X6-RX

V 1.3 4/16/11

PMC/XMC Module with Four 160 MSPS A/Ds, ASIC downconverter, Virtex6 FPGA, 4 GB Memory and PCI/PCIe

FEATURES

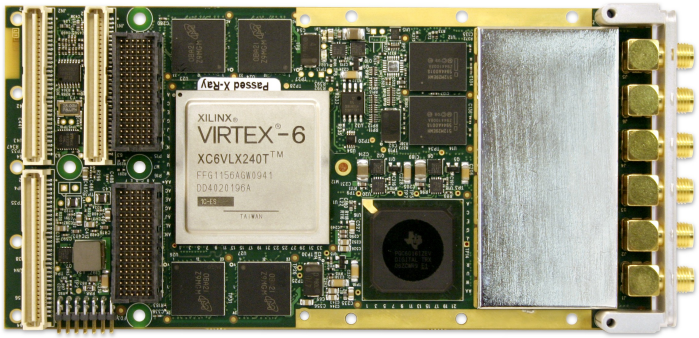
- Four 160 MSPS, 16-bit A/D channels
- Down-Converter ASIC supporting up to 48 Narrowband or 8 Wideband Channels
- +/-1V, AC-Coupled, 50 ohm, SMA inputs
- Xilinx Virtex6 SX315T/SX475T or LX240T
- 4 Banks of 1GB DRAM (4 GB total)
- Ultra-low jitter programmable clock
- Gen2 x8 PCI Express providing 2 GB/s sustained transfer rates
- PCI 32-bit, 66 MHz with P4 to Host card
- PMC/XMC Module (75x150 mm)
- 15-22W typical
- Conduction Cooling per VITA 20
- Ruggedization Levels for Wide Temperature Operation
- Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

APPLICATIONS

- Wireless Receiver
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux/VxWorks Drivers
- C++ Host Tools



DESCRIPTION

The X6-RX is a flexible IF receiver that integrates IF digitizing with signal processing on a PMC/XMC IO module. The module provides up to 48 configurable receiver channels with a powerful Xilinx Virtex 6 FPGA signal processing core, and high performance PCI Express/PCI host interface. With the X6-RX, IF recorders can log both the digitized raw data and channels real-time sustaining rates over 2 GB/s.

The X6-RX features four, 16-bit 160 MSPS A/Ds plus an on-board digital down-converter (DDC) ASIC. IF frequencies of up to 400 MHz are supported. The sample clock is from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling and down-conversion.

A Xilinx Virtex6 SX315T (LX240T and SX475T options) with 4 banks of 1GB DRAM provide a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at extremely high rates.

The digital down-converter (DDC) device, connected directly to the FPGA, provides up to 48 narrow-band or 8 wide-band channels, with input from two A/D channels. The DDC perform complex or real down-conversion, with flexible controls for mixing, filtering, decimation, output formats and data rates. Channels can be synchronized to support beam forming or frequency hopped systems.

The X6-RX power consumption is 15W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

The FPGA logic can be fully customized using VHDL and MATLAB using the Frame Work Logic tool set. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator. IP cores for many wireless and DSP functions such as DDC, PSK/FSK demod, OFDM receiver, correlators and large FFT are available.

Software tools for host development include C++ libraries and drivers for Windows, Linux and VxWorks. Application examples demonstrating the module features are provided.

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04/16/11

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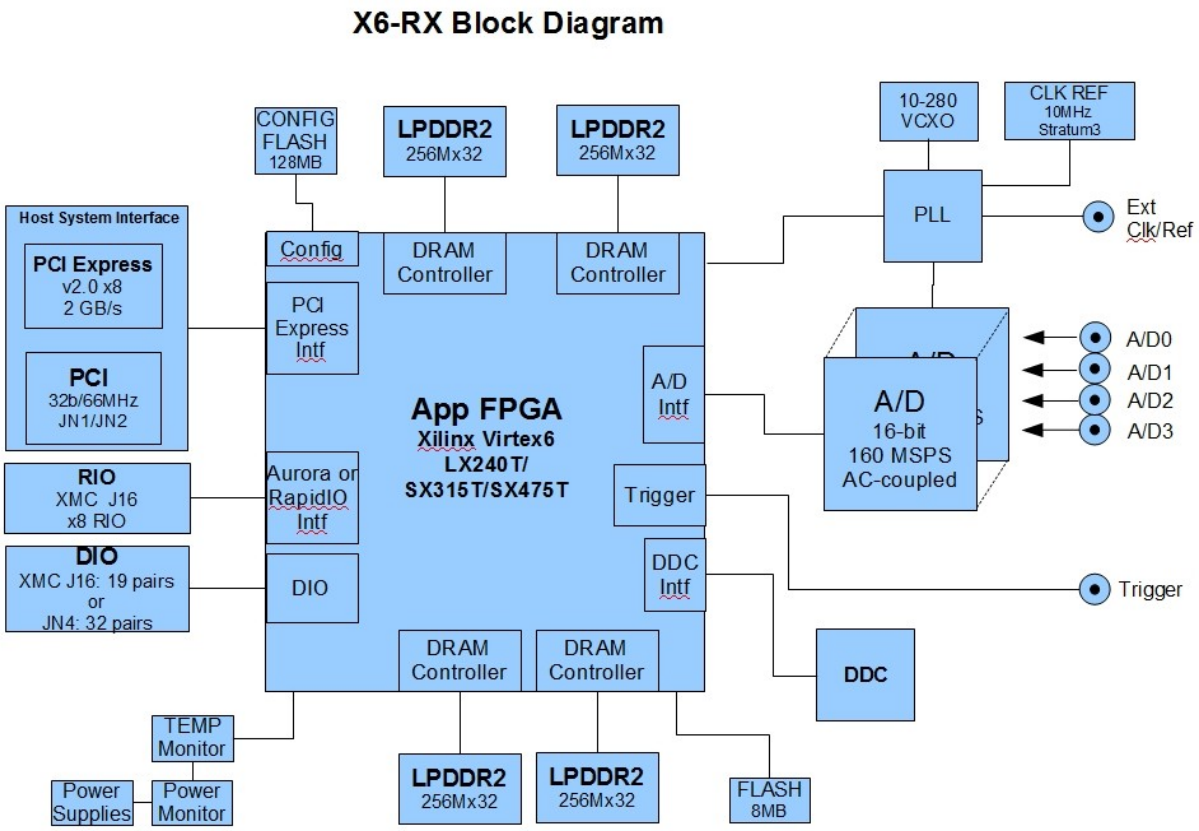
X6-RX

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X6-RX	80245-0-<ER>	PMC/XMC module with four 160 MSPS A/Ds, Virtex6 LX240T FPGA, 1GB DRAM, downconverter ASIC. <ER> is environmental rating.
Logic Development Package		
X6-RX FrameWork Logic	55030	X6-RX FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCIe Adapter	80172-0	PCI Express carrier card for XMC PCI Express modules, x1 lanes
XMC-PCI Adapter	80167-0	PCI carrier card for XMC PCI Express modules, 64-bit PCI
XMC-PCIe Adapter	80173-0	PCI Express carrier card for XMC PCI Express modules, x8 lanes
XMC-compact PCI/PXI Adapter	80207	3U compact PCI carrier card for XMC PCI Express modules, 64-bit PCI. Support for PXI clock and trigger features (logic dependent).
XMC- Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
PMC-PCIe Adapter	80156	PMC to PCI Adapter Board
PMC-PCI Adapter	80166	PMC to PCI Adapter Board
VPX Adapter	80262	3U VPX adapter for X6. Air-cooled or conduction-cooled versions. REDI covers available.
Embedded PC Host		
eInstrumentPC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Intel i5 or i7 CPU; Windows, Linux or VxWorks
eInstrumentPC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or i7 CPU; Windows, Linux or VxWorks
VPXI-ePC: 3U VPX PC with 4 expansion slots	90271	3U VPX embedded PC with 4 expansion slots, integrated timing and data plane; Intel i7 CPU; Windows, Linux or VxWorks

X6-RX


X6-RX Block Diagram
CONFIG FLASH 128MB
LPDDR2 256Mx32
LPDDR2 256Mx32
10-280 VCXO
CLK REF 10MHz Stratum3
PLL
Ext Clk/Ref
Host System Interface
PCI Express v2.0 x8 2 GB/s
PCI 32b/66MHz JN1/JN2
RIO XMC J16 x8 RIO
DIO XMC J16: 19 pairs or JN4: 32 pairs
Config
DRAM Controller
DRAM Controller
PCI Express Intf
Aurora or RapidIO Intf
DIO
App FPGA
Xilinx Virtex6
LX240T/
SX315T/SX475T
A/D Intf
Trigger
DDC Intf
DRAM Controller
DRAM Controller
A/D
16-bit
160 MSPS
AC-coupled
A/D0
A/D1
A/D2
A/D3
Trigger
DDC
TEMP Monitor
Power Supplies
Power Monitor
LPDDR2 256Mx32
LPDDR2 256Mx32
FLASH 8MB

X6-RX

Operating Environment Ratings

X6 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

X6-RX

Standard Features

Analog	
Inputs	4
Input Range	2.4Vpp
Input Type	Single ended, AC or DC coupled
Input Impedance	50 ohm
A/D Device	National Semiconductor ADC16DV160
A/D Resolution	16-bit
A/D Sample Rate	1 MHz to 160 MHz
Input Bandwidth	200 MHz (-3dB)

FPGA	
Device	Xilinx Virtex6
Speed Grade	-1
Size	SX315T : ~31M gate equivalent
Flip-Flops	SX315T: 393K
Multipliers	SX315T: 1344
Slice	SX315T: 49,200
Block RAMs	SX315T: 1408 (25344 Kbits)
Rocket IO	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Digital Down Converter Option	
Channels	4 to 24 Channels of digital receiver; Synchronization supported
Signal Types	Accepts real or complex signals
Decimation	1 to 4096
Gain	User selectable
Word Size	Up to 20-bit output; Real or complex
Filter	Adjustable interpolation and filter
Mixer	Adjustable Freq/Phase Offset

Memories	
DRAM Size	4 GB; 4 banks of 1GB each
DRAM Type	LPDDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	Up to 5.2 GB/s sustained transfer rate per bank (333 MHz clock)

X6-RX

Host Interface	
PCI	32-bit, 33/66 MHz (auto detected) PCI 1.0a
PCI Sustained Data Rate	>200 MB/s @32/66 >80 MB/s @32/33
PCI Express	x8 Lanes, VITA 42.3 PCI Express Gen 2 (x4 for -1 speed FPGA) PCI Express Gen 1 (x8)
PCI Express Sustained Rate	2 GB/s

Clocks and Triggering	
Clock Sources	PLL or External
	0.3125 to 160 MHz
PLL Reference	External or 10MHz on-card 10MH ref is +/-250ppb -40to 85C
PLL Resolution	100 kHz Tuning Resolution
Phase Noise	-130 dBc @ 100 kHz
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	5 ns resolution, 32-bit counter

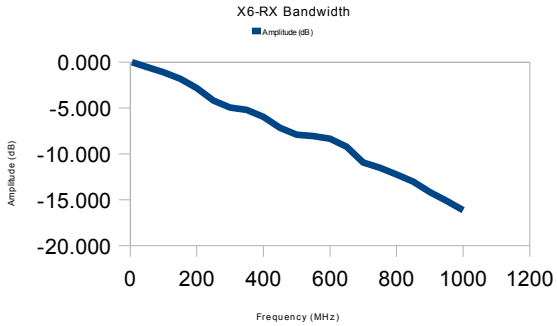
Application IO (J4/J16)	
Rocket IO Channels	8 (J16)
Rocket IO data rate	5 Gbps/lane (4 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	32 (J16/J4)
Signal Standard	LVTTL (2.5V) – NOT 3.3 compatible
Drive	+/-12 mA
Connectors	PMC J4/ XMC J16

Power	
Consumption	15.4W (VPWR = 5V, 1 DDR bank and no Aurora ports instantiated, 4 lane PCIe) 23W (VPWR = 12V, 4 DDR banks, all Aurora ports, 4 lane PCIe)
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)
Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g
Hazardous Materials	Lead-free and RoHS compliant

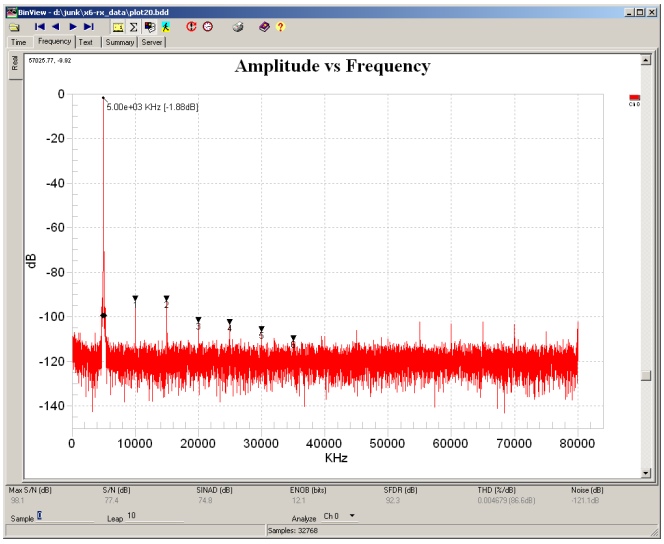
ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

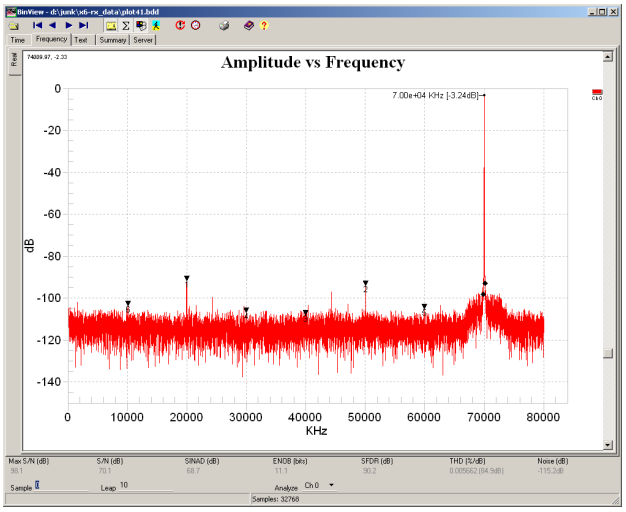
Parameter	Typ	Units	Notes
Analog Input Bandwidth	200	MHz	-3dB, 22 pF filter cap at A/D device inputs
SFDR	86	dB	70 MHz sine input, 85%FS, Fs = 160 MSPS
S/N	68	dB	70 MHz sine input, 85%FS, Fs = 160 MSPS
THD	0.01	%	70 MHz sine input, 85%FS, Fs = 160 MSPS
ENOB	11	bits	70 MHz sine input, 85%FS, Fs = 160 MSPS
Channel Crosstalk	<80	dB	70 MHz, 2Vp-p on adjacent channels
Noise Floor	-110	dB	Input Grounded, Fs = 160 MSPS, 32K sample FFT, non-averaged
Gain Error	<0.2	% of FS	Calibrated
Offset Error	<500	µV	Calibrated



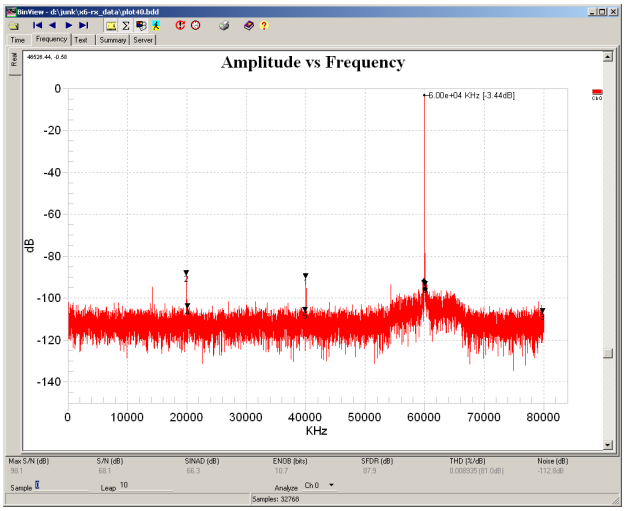
X6-RX Input Bandwidth (22 pF parallel cap at A/D device input)



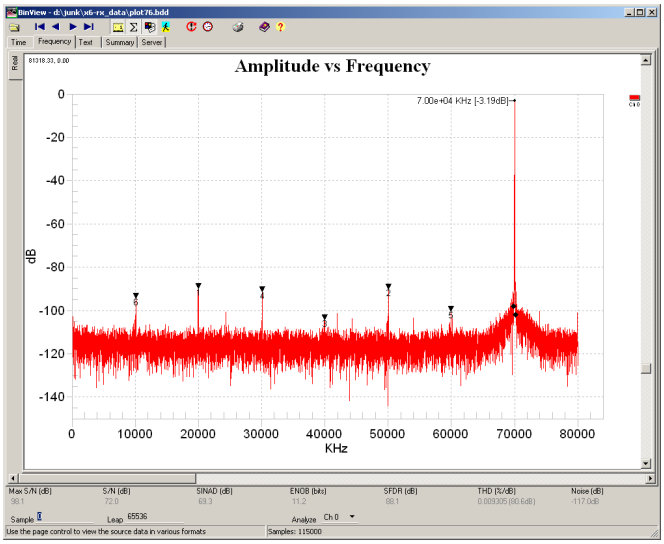
Signal quality, Fin = 5 MHz, Fs = 160 MHz onboard PLL. Channel 0, 22 pF parallel cap at A/D device inputs



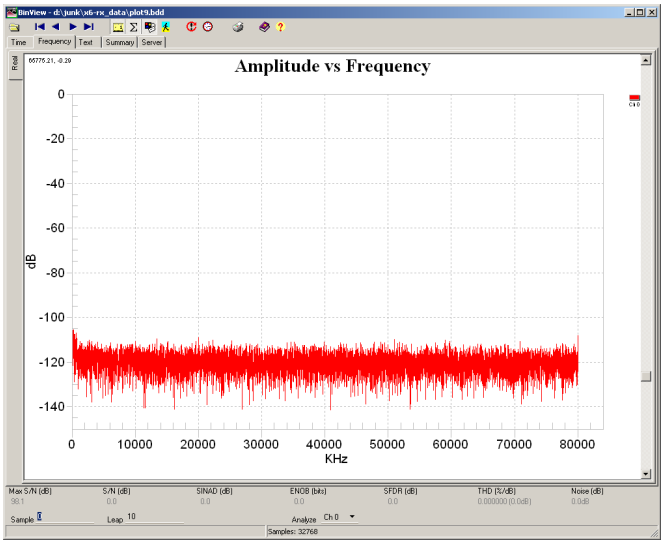
Signal quality, Fin = 70 MHz, Fs = 160 MHz onboard PLL. Channel 0, 22 pF parallel cap at A/D device inputs



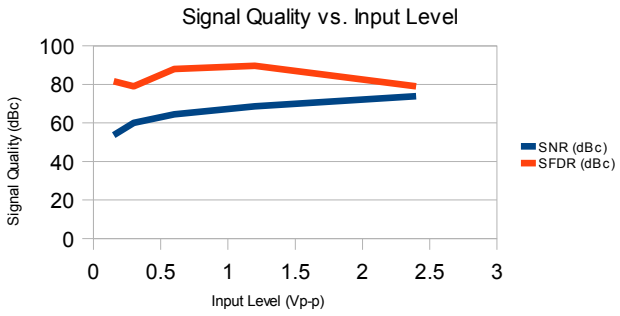
Signal quality, Fin = 70 MHz, Fs = 160 MHz onboard PLL. Channel 0, 22 pF parallel cap at A/D device inputs

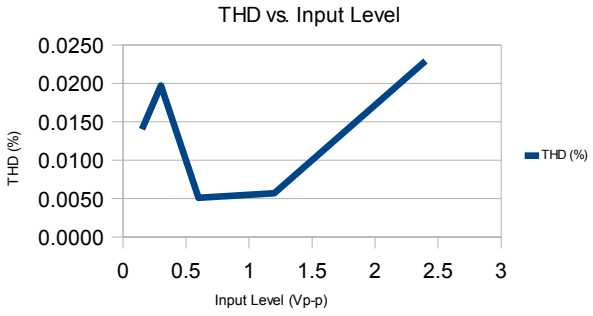


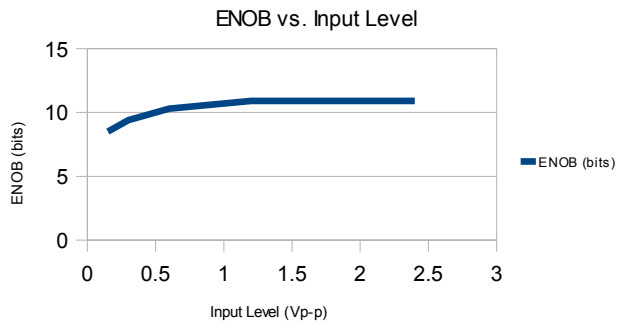
Signal quality, Fin = 70 MHz, Fs = 160 MHz onboard PLL. Channel 1, 70 MHz tank circuit at A/D device inputs, 160 MHz BPF at A/D device clock inputs



Signal quality, open input, Fs = 160 MHz external clock.



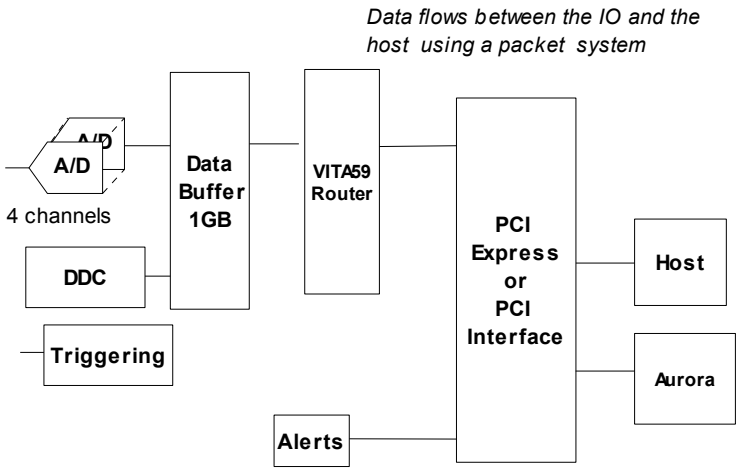




X6-RX

Architecture and Features

The X6-RX module architecture integrates analog IO with an FPGA computing core, memories and PCI host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding applications in wireless, RADAR and medical imaging applications.



X6 Architecture

Analog IO

The analog front end of the X6-RX module has four simultaneously sampling channels of 16-bit, 160 MSPS A/D input. The A/D inputs have an analog input bandwidth of 400 MHz for wideband and direct sampling applications. The A/Ds are directly connected to the FPGA for minimum data latency. In the standard logic, the A/Ds have an interface component that receives the data, provides digital error correction, and a FIFO memory for buffering. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.

The A/D channels operate synchronously for simultaneously sampling systems using the external clock input. Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized in the logic to accommodate a variety of triggering requirements.

FPGA Core

The X6 Module family has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 FPGA is capable of over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to four banks of 1GB DRAM. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The X6 module family uses the Virtex6 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X6 module functionality. Logic utilization is typically <10% of the device.

PCI Express Host Interface

The X6 architecture delivers over 2 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is

transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex6 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 40 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 400 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

PCI Host Interface

The X6 family can be optionally configured with a PCI interface capable of over 200 MB/s sustained rates. The Velocia architecture is the same as the PCI Express system, supporting the packet system with DMA.

System Data Plane Ports and Digital IO

The X6 module family has eight high speed serial data links on J16 for system interconnect, operating at up to 5 Gbps per link, full duplex. These links enable the X6 modules to integrate into switched fabric systems such as VPX to create powerful computing and signal processing architectures. The standard logic uses these lanes as two Aurora ports of 4 lanes each. Other protocols such as SRIO and SFPDP may be implemented in the FPGA.

J4 connector has 32 digital lines that connect to the FPGA. These digital IO lines are direct connections to the FPGA.

Module Management

The X6 family has independent temperature monitoring for the FPGA die. The temperature sensor is set so that power shuts when a critical temperature is exceeded. This function is independent of the FPGA.

The data acquisition process can be monitored using the module alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the card easier to integrate into larger systems.

FPGA Configuration

The modules uses a FLASH memory for the Virtex 6 FPGA image. This FLASH can be programmed in-system using a software applet. There are two images in the FLASH: an application image and a “golden” image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable.

Software Tools

Software development tools for the module provides comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

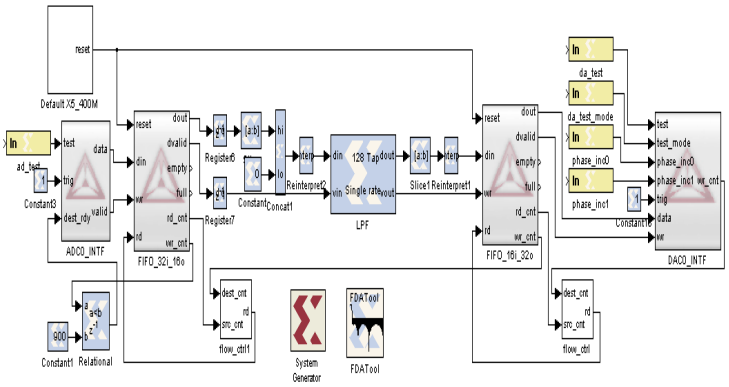
Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or

to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include Windows, Linux and VxWorks. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

IP for X6 Modules

Innovative provides a range of down-conversion channelizer logic cores for wideband and narrowband receiver applications for the X6 family. When fitted with these cores, the X6 modules provide powerful receiver functionality integrated for IF processing.

The DDC channelizers are offered in channel densities from 4 to 128. The four channel DDC offers complete flexibility and independence in the channels, while the 128 channel core offers higher density for uniform channel width applications. The DDC cores are highly configurable and include programmable channel filters, decimation rates, tuning and gain controls. An integrated power meter allows the DDC to measure any channel power for AGC controls. Multiple cores can be used for higher channel counts.

Each IP core is provided with a MATLAB simulation model that shows bit-true, cycle-true functionality. Signal processing designers can then use this model for channel design and performance studies. Filter coefficients and other parameters from the MATLAB simulation can be directly loaded to the hardware for verification.

X6-RX

Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58014	IP-MDDC4	4	Fs/2^32	16 to 32768	Fs/16	Programmable 100 tap filter
58015	IP-MDDC128	128	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter

Additional IP cores are offered for IF processing and baseband demodulation.

Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision. Data rate to 160 Mbps.
58018	PSK Modulator	N=2,4,8,PI/4. Data rates up to 160 Mbps.
58002	FSK Demodulation	Coherent demodulation with carrier recovery,
58019	FSK Modulator	FSK modulation/
58020	QAM Modulator	Quadrature Amplitude Modulator.
58003	TinyDDS	Tiny DDS, 1/3 to ½ size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions.
58012	Windowing	IP core for Hann, Blackman and uniform data windowing functions.
58013	CORDIC	IP core for sine/cosine generation using CORDIC method, resulting in 1/3 logic size of standard DDS cores.
58030	MDUC128	128-channel digital upconverter.

OFDM and LTE Cores

58029	OFDM Transmitter	OFDM transmit with IFFT, Windowing, Filtering, Cyclic Prefix and Upsample.
58031	OFDM Receiver	OFDM receiver with synchronization, downconversion and channel filtering.
58032	LTE Dowlink Transmitter	LTE downlink transmitter core for FDD mode.
58033	LTE Uplink Receiver	LTE uplink receiver core for FDD mode includes 2K FFT, timing and frame synchronization using ML estimation method, decoding of SSS and PSS signals for cell ID and frame sync.

Applications Information

Cables

The X6-RX module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.

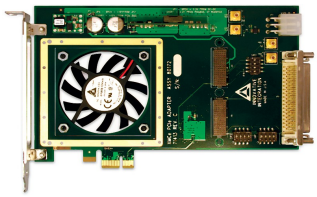
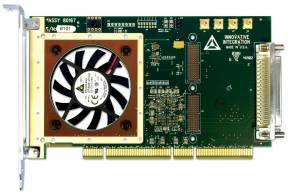
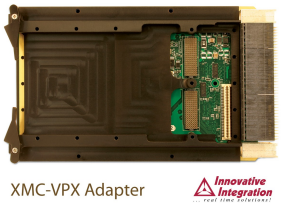
XMC Adapter Cards

X6-RX

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X6 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with digital IO signals provide support for data transfer rates up to 2.0 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80173 is suitable for high speed P16 applications.

PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs 	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC P16 x8 RIO ports to SATA2 connectors DIO to MDR68 	**PCIe-XMC Adapter x8 lane (80259)** x8 PCIe to XMC P16 x8 RIO ports to SATA connectors DIO to MDR68 Preferred for X6 Modules 	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC 
VPX-XMC Adapter (80262-6) 3U conduction-cooled VPX adapter Configurable port A-D mapping Optional REDI covers 	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support 		

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X6 modules.

X6-RX

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201)

Windows/Linux embedded PC
Intel Core2Duo or low power Atom available
8x USB, GbE, cable PCIe, VGA
High speed x8 interconnect between modules
GPS disciplined, programmable sample clocks and triggers to XMCs
100 MB/s, 400 GB datalogger
9-18VDC operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion
Up to 7 meter cable
electrically isolated from host computer
software transparent
Supports standalone operation for X6 modules

3U VPX PC with Four Expansion Slots and Integrated Timing (90271)

3U VPX, air-cooled chassis with backplane
Rns Windows, Linux, VxWorks
Intel Dual Core i5 or i7, 8GB, 256MB SSD
4x USB, GbE, x8 cable PCIe, Displayport, T
Integrated timing clocks and triggers with GPS option
400 MB/s, 1TB datalogger
AC or DC operation

X6-RX

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