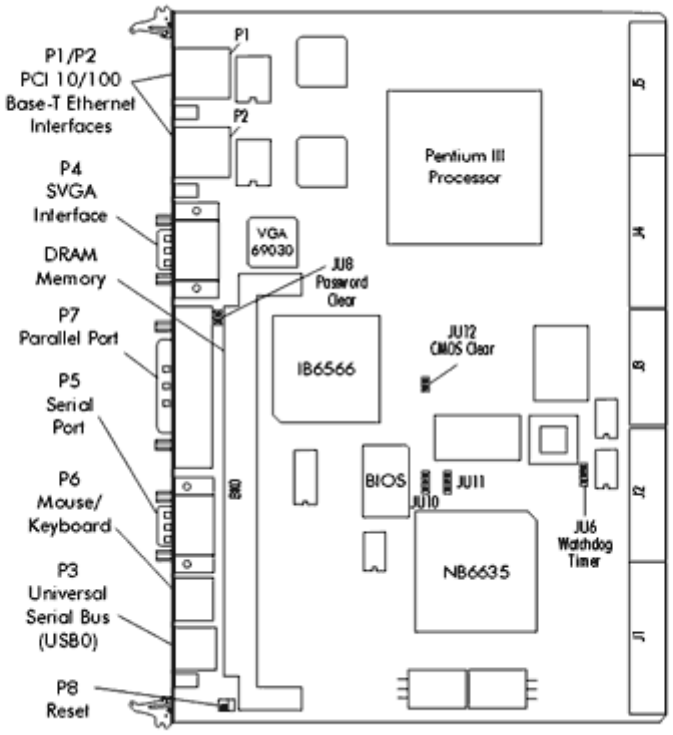
Technical Information – Jumpers, Connectors and Memory
CPLE (5932-xxx) System Host Board

Layout Diagram



Jumpers & LEDs

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "TOP" and "BOTTOM" are defined with the bracket end of the board to the left.

JU6 Watchdog Timer

Install on the TOP for normal reset operation. *
Install on the BOTTOM to enable watchdog timer operation.

JU8 Password Clear

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU10/11 SYSTEM FLASH ROM OPERATIONAL MODES

The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU10	JU11
Program All (Boot and Main)	Top	Top
Normal PnP (Program Main Block)	Top *	Bottom *

Write Protect		Bottom	Bottom

JU12 CMOS Clear

INSTALL = Clear CMOS
REMOVE = Operate *

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. CMOS is cleared during the POST routines. Wait for AMIBIOS to display a "CMOS Checksum Bad" message; then power down the system again and remove the jumper before the next power-up.

Connectors

NOTE:
Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - PCI 10/100BASE-T ETHERNET CONNECTOR

8 pin shielded RJ-45 connector, Molex #43202-8110

PIN	SIGNAL
1	TD+
2	TD-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC

P2 - PCI 10/100BASE-T ETHERNET CONNECTOR

8 pin shielded RJ-45 connector, Molex #43202-8110

PIN	SIGNAL
1	TD+
2	TD-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC

P3 - UNIVERSAL SERIAL BUS (USB0) CONNECTOR

Right angle single port, Amp #787616-1
(+5V fused with self-resetting fuses)

PIN	SIGNAL
1	+5V - USB0
2	USB0-
3	USB0+
4	Gnd - USB0

P5 - SERIAL PORT CONNECTOR

Right angle 9 pin D, Amp #869436-1

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-0	8	Clear to Send-I
4	Data Terminal Ready-0	9	Ring Indicator-I
5	Signal Gnd		

P6 - PS/2 MOUSE AND KEYBOARD CONNECTOR

6 pin mini DIN, Kycon #KMDG-6S-BS-PS

PIN	SIGNAL
1	Ms Data
2	Kbd Data
3	Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P7 - PARALLEL PORT CONNECTOR

25 pin D, Amp #747846-4

PIN	SIGNAL	PIN	SIGNAL
1	Strobe	14	Auto Feed XT
2	Data Bit 0	15	Error
3	Data Bit 1	16	Init
4	Data Bit 2	17	Slct In
5	Data Bit 3	18	Gnd
6	Data Bit 4	19	Gnd
7	Data Bit 5	20	Gnd
8	Data Bit 6	21	Gnd
9	Data Bit 7	22	Gnd
10	ACK	23	Gnd
11	Busy	24	Gnd
12	Paper End	25	Gnd

Connectors (Continued)

P4 - PCI SVGA VIDEO INTERFACE CONNECTOR

15 pin VGA connector, Amp #748390-5

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	Red	6	Gnd	11	NC
2	Green	7	Gnd	12	EEDI
3	Blue	8	Gnd	13	HSYNC
4	NC	9	+5V	14	VSYNC
5	Gnd	10	Gnd	15	EECS

P8 - EXTERNAL RESET CONNECTOR

2 pin header, Amp #640456-2

PIN	SIGNAL
1	External Reset In (Low Active)
2	Gnd

Memory

The DRAM interface consists of one dual in-line memory module (DIMM) socket and supports auto detection of memory up to 1GB of Synchronous DRAM (SDRAM). The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 72-bit wide gold finger DIMM DRAM in a 168-pin DIMM socket.

NOTE: EDO DIMMs and unbuffered SDRAM DIMMs are not supported. All DIMMs must have gold contacts.

The SBC supports DIMM memory modules which are PC-133 compliant and have the following features:

- 168-pin DIMMs with gold-plated contacts
- 133MHz SDRAM
- ECC (72-bit) memory
- 3.3 volt
- Registered configuration

The following DIMM sizes are supported:

DIMM Size	DIMM Type	ECC
64 MB	Registered	8M x 72
128 MB	Registered	16M x 72
256 MB	Registered	32M x 72
512 MB	Registered	64M x 72
1 GB	Registered	128M x 72

NOTE: DIMM modules must not exceed 1.7" in height.

All memory components and DIMMs used with the SBC must be PC-133 compliant, which means that they comply with IBM's PC133 SDRAM Registered DIMM Design Specification.