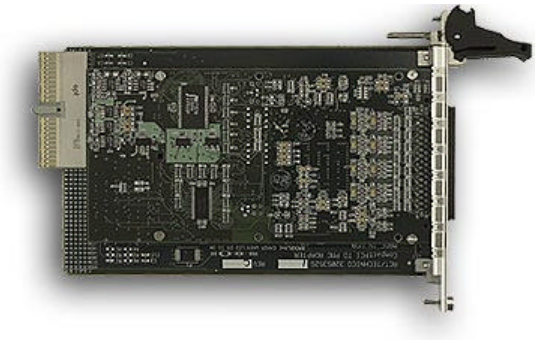
General Standards Corporation

High Performance Bus Interface Solutions

CPCI-12AI64

64-Channel, 12-Bit Analog Input CPCI Board

With 1,500 KSPS Input Conversion Rate



Features Include:

- 64 Single-ended or 32 Differential 12-Bit Scanned Analog Input Channels
- Sample Rates to 1,500 KSPS per Second in Single-Channel Mode; 1,000 KSPS in Scanning Mode
- Input Ranges Selectable as ±10V, ±5V or ±2.5V
- 64-Ksample FIFO Data Buffer
- Continuous and Burst (One-Shot) Input Modes
- Sync Input and Output (Alternate Function for Channels 62,63)
- Internal Rate Generator Implements a 32-Bit Divider
- Scan Sizes from 2 to 64 Channels-per-Scan
- can Rates Adjustable from 0.01 to 500K Scans-per-Second (2-channel scan)
- Internal Autocalibration; No Host Involvement
- DMA Engine Minimizes Host I/O Overhead
- Dynamic Node Control Minimizes Crosstalk and Input Bias Current
- Completely Software-Configurable; No Field Jumpers
- Single-width CPCI Form Factor

Applications Include:

- ✓ Data Acquisition Systems
- ✓ Voltage Measurement
- ✓ Industrial Robotics
- ✓ Automatic Test Equipment
- ✓ Transient Analysis
- ✓ Research Instrumentation

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Overview:

The CPCI-12AI64 board provides cost effective 1,500,000 samples-per-second 12-bit analog input capability in a single-width CPCI format. The inputs are configurable either as 64 single-ended channels or as 32 differential channels, and the input range is software-selectable as ±10V, ±5V or ±2.5V. Scan rates can be controlled from (a) an internal rate generator, (b) through an external digital input, or (c) by direct software commands. Multiple CPCI-12AI64 boards can be connected together for synchronous scanning. Data is buffered through a 64K-sample FIFO. Internal autocalibration networks permit calibration to be performed without removing the board from the system.

Functional Description:

The CPCI-12AI64 board is a scanning analog digitizer that performs high-speed sampling and 12-bit A/D conversion of as many as 64 single-ended or 32 differential analog input channels. The resulting 12-bit sampled data is available to the PCI bus through a data buffer that is configured as a 64K-Sample FIFO. All operational parameters are software configurable.

The analog inputs can be sampled in scans of 2, 4, 8, 16, 32 or 64 single-ended channels, or in scans of 2, 4, 8, 16 or 32 differential channels. The scan rate can be controlled internally up to 500,000 scans per second for 2-channel scans. Sync input and output signals permit multiple boards to perform synchronous scanning. Input buffer amplifiers on all channels eliminate the high input currents that are produced by nonbuffered multiplexers running at high scan rates.

An internal autocalibration utility uses hardware D/A converters to correct for offset and gain errors in the input signal path, and eliminates the missing codes that are inevitably introduced when software correction methods are used. A selftest switching network routes calibration signals through the input multiplexer to the A/D converter to support internal autocalibration, and permits board integrity to be tested by the host. Autocalibration is performed automatically after reset or upon demand from the PCI bus, and calibrates the offset and gain of the converter to a precision internal reference voltage.

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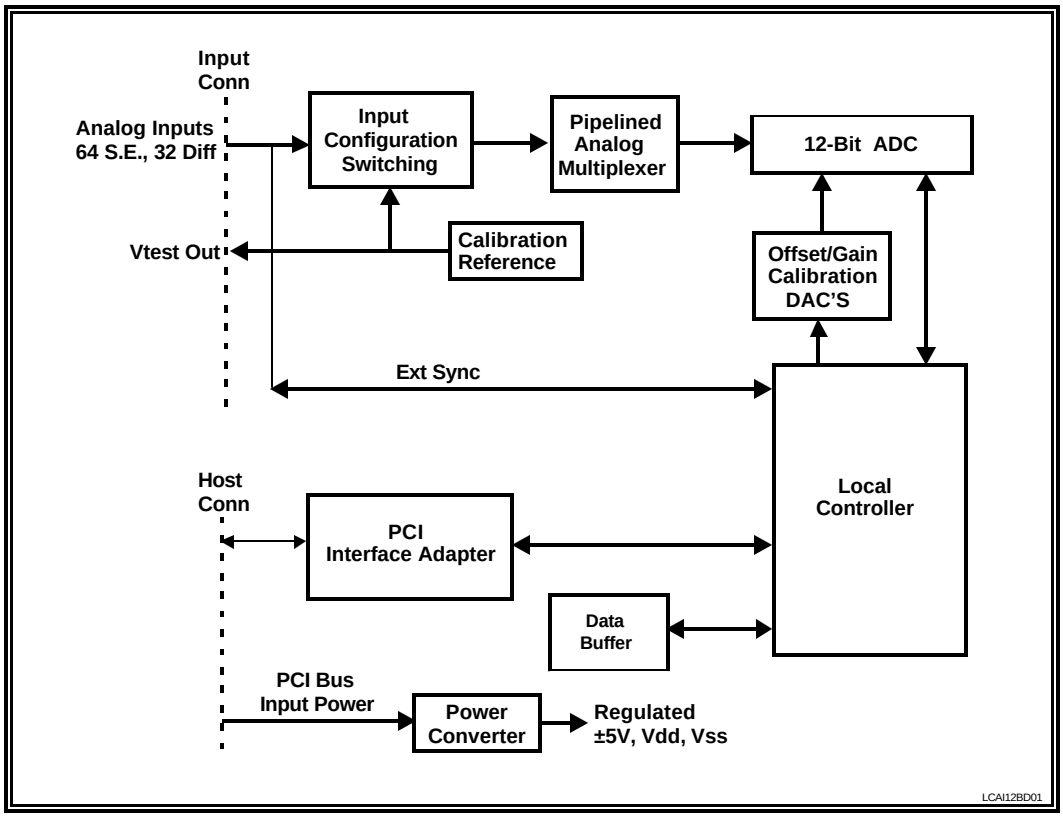

Figure 1. CPCI-12AI64; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.1, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density 68-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

❑ Input Characteristics:

Configuration:	64 single-ended or 32 differential analog input channels
Voltage Ranges:	Software configurable as ±10 Volts, ±5 Volts or ±2.5 Volts
Input Impedance:	1.0 Megohm, independent of scan rate
Common Mode Rejection:	60 dB typical, DC-60 Hz (Differential inputs)
Common Mode Range:	±10 Volts; differential input configuration
Offset Voltage:	±3.0 millivolts, maximum
Bias Current:	Less than 80 nanoamps.
Noise:	2.0 LSB-RMS typical
Crosstalk Rejection:	75dB typical, DC-10kHz
Overvoltage Protection:	±30 Volts with power applied*; ±15 Volts with power removed.

* Inputs 62,63 (Alternate function TTL Sync I/O) limited to -0.5 to +7.0 Volts

❑ Transfer Characteristics:

Resolution:	12 Bits (0.0244 percent of FSR)
Maximum Sample Rate:	1,500 KSPS in single-channel mode; 1,000 KSPS (aggregate) in scanning mode
Scan Rate:	Adjustable internally from 0.01 to 500K scans per second.
Channels per scan:	2, 4, 8, 16, 32 or 64 Single-ended channels; 2, 4, 8, 16 or 32 differential channels. One channel in single-channel mode.

DC Accuracy: (Maximum composite error after autocalibration)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	± 10mv	±12mv
±5V	± 5mv	± 7mv
±2.5V	± 3mv	± 5mv

Integral Nonlinearity:	±0.04 percent of FSR, typical
Differential Nonlinearity:	±0.024 percent of FSR, maximum

❑ Analog Input Operating Modes and Controls

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Input Data Buffer:	64K-sample FIFO, with status flags and interrupt.	
Analog Input Modes:	Continuous Scan:	Analog inputs are scanned continuously
	Burst Scan:	Each scan is initiated either by the internal rate generator, or by a hardware TTL input or a software sync input.
	Single Channel:	Any single selected channel is sampled continuously
	Selftest:	Autocalibration and Selftest modes
Rate Generator:	Programmable from 0.01 - 500,000 scans per second in scanning mode, 0.01 to 1,500,000 samples per second in single-channel mode.	
Input Data Format:	Selectable as offset binary or as two's complement	

AUTOCALIBRATION

A single bit in the board control register initiates Autocalibration. During autocalibration, all analog channels are calibrated to a single precision internal voltage reference. Autocalibration has a typical duration of less than one second.

PCI INTERFACE

❑ **Compatibility:** Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5VDC ±0.2 VDC at 1.5 Amp, maximum

Maximum Power Dissipation:	6.0 Watts,	Side 1
	1.0 Watt,	Side 2

❑ Physical Characteristics

Height:	100 mm
Depth:	15.05 mm
Width:	160 mm
Shield:	Side 1 can be protected by an optional EMI shield.

❑ Environmental Specifications

Ambient Temperature Range:	Operating:	0 to +55 degrees Celsius
	Storage:	-40 to +85 degrees Celsius
Relative Humidity:	Operating:	0 to 80%, non-condensing
	Storage:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.	
Cooling:	Conventional convection cooling	

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ORDERING INFORMATION

Specify the basic product model number CPCI-12AI64.

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SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

P2 ROW-A		
PIN	SIGNAL	
	S.E. MODE	DIFF MODE
1	INP00	INP00 HI
2	INP01	INP00 LO
3	INP02	INP01 HI
4	INP03	INP01 LO
5	INP04	INP02 HI
6	INP05	INP02 LO
7	INP06	INP03 HI
8	INP07	INP03 LO
9	INP08	INP04 HI
10	INP09	INP04 LO
11	INP10	INP05 HI
12	INP11	INP05 LO
13	INP12	INP06 HI
14	INP13	INP06 LO
15	INP14	INP07 HI
16	INP15	INP07 LO
17	AGND	AGND
18	AGND	AGND
19	INP16	INP08 HI
20	INP17	INP08 LO
21	INP18	INP09 HI
22	INP19	INP09 LO
23	INP20	INP10 HI
24	INP21	INP10 LO
25	INP22	INP11 HI
26	INP23	INP11 LO
27	INP24	INP12 HI
28	INP25	INP12 LO
29	INP26	INP13 HI
30	INP27	INP13 LO
31	INP28	INP14 HI
32	INP29	INP14 LO
33	INP30	INP15 HI
34	INP31	INP15 LO

P2 ROW-B		
PIN	SIGNAL	
	S.E. MODE	DIFF MODE
1	INP32	INP16 HI
2	INP33	INP16 LO
3	INP34	INP17 HI
4	INP35	INP17 LO
5	INP36	INP18 HI
6	INP37	INP18 LO
7	INP38	INP19 HI
8	INP39	INP19 LO
9	INP40	INP20 HI
10	INP41	INP20 LO
11	INP42	INP21 HI
12	INP43	INP21 LO
13	INP44	INP22 HI
14	INP45	INP22 LO
15	INP46	INP23 HI
16	INP47	INP23 LO
17	AGND	AGND
18	AGND	AGND
19	INP48	INP24 HI
20	INP49	INP24 LO
21	INP50	INP25 HI
22	INP51	INP25 LO
23	INP52	INP26 HI
24	INP53	INP26 LO
25	INP54	INP27 HI
26	INP55	INP27 LO
27	INP56	INP28 HI
28	INP57	INP28 LO
29	INP58	INP29 HI
30	INP59	INP29 LO
31	INP60	INP30 HI
32	INP61	INP30 LO
33	INP62/ SYNC HI *	INP31 HI/ SYNC HI*
34	INP63/ SYNC LO*	INP31 LO/ SYNC LO*

* Software-selected.

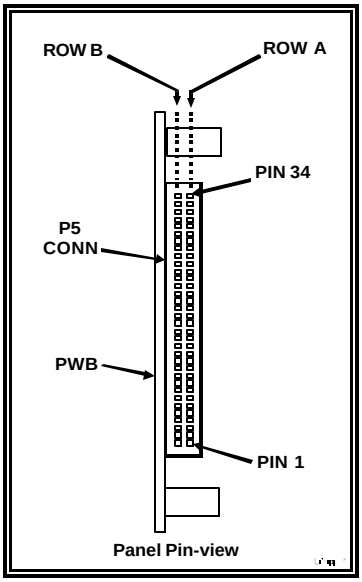

Figure 2. System Input Connector

System Mating Connector:

68-Pin 2-row 0.050" dual-ribbon cable socket connector: Robinson Nugent #P50E-068-S-TG, or equivalent.