1000BASE-T Copper SFP Transceiver

(For 100m reach over Cat 5 UTP cable)

Members of Flexon^{TM} Family

Standard

- ◆ Compatible with SFP MSA
- ◆ Compatible with IEEE Std 802.3^{TM}-2002
- ◆ Compatible with FCC 47 CFR Part 15, Class B
- ◆ RoHS compliance

Description

Fiberxon FTM-C012R-LMG 1000BASE-T copper SFP transceiver is high performance, cost effective module compatible with the Gigabit Ethernet and 1000BASE-T standards as specified in IEEE 802.3-2002 and IEEE 802.3ab, which supporting 1000Mbps data- rate up to 100 meters reach over unshielded twisted-pair category-5 cable.

The FTM-C012R-LMG supports 1000Mbps full duplex data-links with 5-level Pulse Amplitude Modulation (PAM) signals. All four pairs in the cable are used with symbol rate at 250Mbps on each pair.

The FTM-C012R-LMG provides standard serial ID information compatible with SFP MSA, which can be accessed with address of A0h via the 2-wire serial CMOS EEPROM protocol. The physical IC can also be accessed via 2-wire serial bus at address ACh.

The FTM-C012R-LMG is compliant with RoHS

Features

- ◆ Up to 1.25Gbps bi-direction data links
- ◆ 100m transmission over unshielded twisted-pair (UTP) Category 5 Cable
- ◆ 1000BASE-T operation in host systems with Serdes interface default
- ◆ Hot-pluggable capability
- ◆ SFP form with compact RJ-45 connector
- ◆ With spring latch for high density application
- ◆ Very low EMI and excellent ESD protection
- ◆ +3.3V single power supply
- ◆ Low power dissipation
- ◆ Operating case temperature: -5 to +70°C
- ◆ Detailed product information in EEPROM
- ◆ Physical layer IC can be accessed via 2-wire serial bus

Applications

- ◆ LAN 1000Base-T
- ◆ Switch to Switch interface
- ◆ Switched backplane applications
- ◆ Router/Server interface

Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Fiberxon regulatory specification and safety guidelines, or contact Fiberxon, Inc. America sales office listed at the end of the documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 2(>2000 V)
Electrostatic Discharge (ESD) to the RJ-45 Receptacle	IEC 61000-4-2 GR-1089-CORE	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compatible with standards
Immunity	IEC 61000-4-3	Compatible with standards
Component Recognition	UL and CSA	Compatible with standards
RoHS	2002/95/EC 4.1&4.2	Compliant with standards

Absolute Maximum Ratings

Stress in excess of the maximum absolute ratings can cause permanent damage to the module.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Operating Relative Humidity	-	5	95	%

Recommended Operating Conditions

Table 3- Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	-5		70	°C	
Power Supply Voltage	V_{CC}	3.13	3.30	3.47	V	
Power Supply Current	I_{CC}		315	370	mA	
Data Rate				1000	Mbps	

Host Side Electrical Interface

Table 4 - Electrical Characteristics

Parameter		Symbol	Min.	Typical	Max.	Unit	Notes
Data Input Swing Differential		V_{IN}	250		1200	mV	1
Input Differential Impedance		Z_{IN}		100		Ω	
TX Disable	Disable			2.0		Vcc	V	
	Enable			Vee		Vee+0.8	V	
Data Output Swing Differential		V_{OUT}	350		800	mV	2
Output Differential Impedance		Z_{OUT}		100		Ω	
Output Data Rise/Fall Time		Tr/Tf		175		ps	

Notes:

1.   Internally AC coupled and terminated.

2.   Internally AC coupled.

Line Side Electrical Interface

Table 5 - Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Line Baud Rate			125		MHz	1
Bit Error Rate	BER			10^{-12}		2
Line Rx Intput Impedance	Z_{IN}		100		Ω	
Line Tx Output Impedance	Z_{OUT}		100		Ω	

Notes:

1.   Use 5-level PAM encoding.

2.   Measured over 100m Cat-5 UTP cable.

EEPROM Information

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard interfaces, manufacturer, and other information, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h). See Table 6 for the memory contents. The physical IC can also be accessed via 2-wire serial bus at address ACh, please refer to the related document of *Fiberxon 1000BASE-T Copper SFP Application Note* for more information.

Table 6 - EEPROM Serial ID Memory Contents (A0h)

Addr.	Field Size (Bytes)	Name of Field	Hex	Description
0	1	Identifier	03	SFP
1	1	Ext. Identifier	04	MOD4
2	1	Connector	00	
3—10	8	Transceiver	00 00 00 08 00 00 00 00	1000BASE-T
11	1	Encoding	01	8B10B
12	1	BR, nominal	0D	1.25G
13	1	Reserved	00	
14	1	Length (9um)-km	00	
15	1	Length (9um)	00	
16	1	Length (50um)	00	
17	1	Length (62.5um)	00	
18	1	Length (copper)	64	100m
19	1	Reserved	00	
20—35	16	Vendor name	46 49 42 45 52 58 4F 4E 20 49 4E 43 2E 20 20 20	"FIBERXON INC. "(ASCⅡ)
36	1	Reserved	00	
37—39	3	Vendor OUI	00 00 00	
40—55	16	Vendor PN	46 54 4D 2D 43 30 31 32 52 2D 4C 4D 47 20 20 20	"FTM-C012R-LMG " (ASCⅡ)
56—59	4	Vendor rev	xx xx xx xx	ASCⅡ ("31 30 20 20" means 1.0 revision)
60-61	2	Wavelength	00 00	
62	1	Reserved	00	
63	1	CC BASE	xx	Check sum of bytes 0 - 62
64—65	2	Options	00 10	TX_DISABLE
66	1	BR, max	00	
67	1	BR, min	00	
68—83	16	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx	ASCⅡ
84—91	8	Vendor date code	xx xx xx xx xx xx 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes)
92—94	3	Reserved	00 00 00	
95	1	CC EXT	xx	Check sum of bytes 64 - 94
96—255	160	Vendor specific		

Note: The "xx" byte should be filled in according to practical case. For more information, please refer to the related document of SFP MSA.

Recommended Host Board Power Supply Circuit

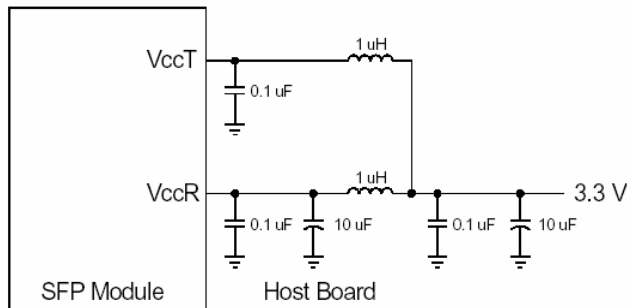Figure 1 shows the recommended host board power supply circuit.

Figure 1, Recommended Host Board Power Supply Circuit

Recommended Interface Circuit

Figure 2 shows the recommended interface circuit.
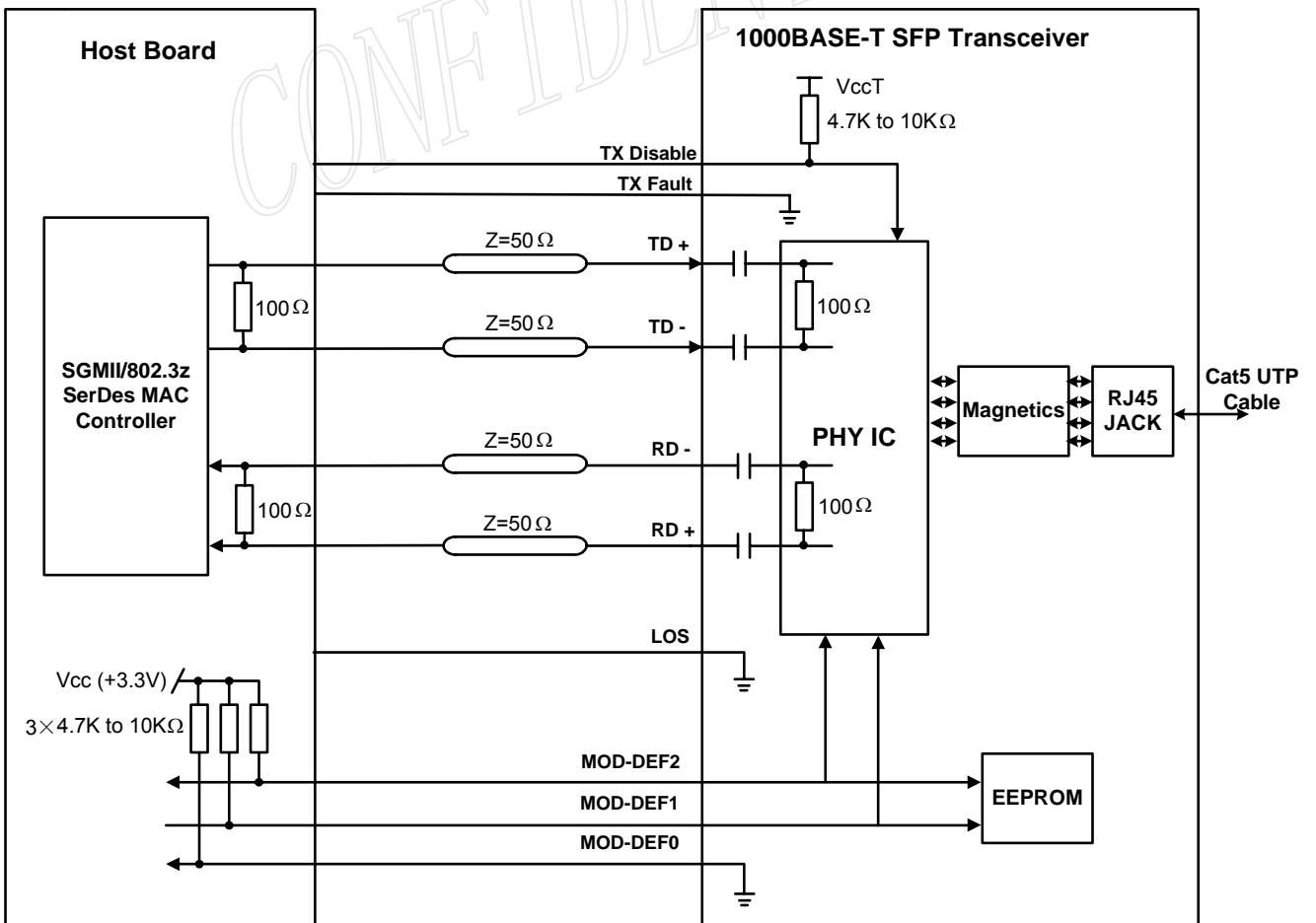

Figure 2, Recommended Interface Circuit

20-Pin Definitions

Figure 3 below shows the 20-pin numbering of SFP to Host electrical interface. The pin functions are described in Table 7 with some accompanying notes.
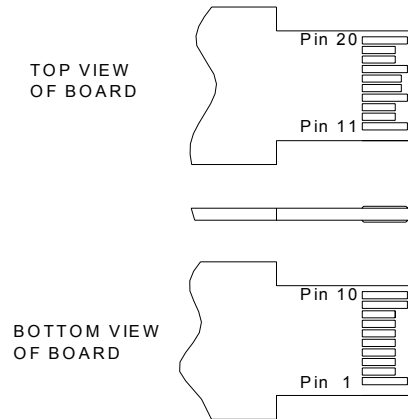

TOP VIEW OF BOARD

Pin 20

Pin 11

BOTTOM VIEW OF BOARD

Pin 10

Pin 1

Figure 3, Pin View

Table 7– Pin Function Definitions

Pin No.	Name	Function	Plug Seq.	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2
4	MOD-DEF2	Module Definition 2	3	Note 3
5	MOD-DEF1	Module Definition 1	3	Note 3
6	MOD-DEF0	Module Definition 0	3	Note 3
7	Rate Select	Not Connected	3	
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inv. Received Data Out	3	Note 5
13	RD+	Received Data Out	3	Note 5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 6
19	TD-	Inv. Transmit Data In	3	Note 6
20	VeeT	Transmitter Ground	1	
20	VeeT	Transmitter Ground	1	

Notes:

1. TX Fault is not used and tied to ground within the module.

2. TX Disable is used to reset the physical IC within the module. It is pulled up within the module with a

4.7k~10kΩ resistor. Its states are:

Low (0~0.8V):   PHY IC on

(>0.8V, <2.0V):   Undefined

High (2.0~3.465V):   PHY IC Reset

Open: PHY IC Reset

3. MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a 4.7k~10kΩ resistor on the host board. The pull-up voltage shall be VccT or VccR.

   MOD-DEF 0 is tied to ground within the module.

   MOD-DEF 1 is the clock line of two wire serial interface for serial ID

   MOD-DEF 2 is the data line of two wire serial interface for serial ID

4. LOS is not used and tied to ground within the module.

5. These are the differential receiver output. They are internally AC-coupled 100Ω differential lines which should be terminated with 100Ω (differential) at the user SERDES.

6. These are the differential transmitter inputs. They are AC-coupled, differential lines with 100Ω differential termination inside the module.

Mechanical Design Diagram
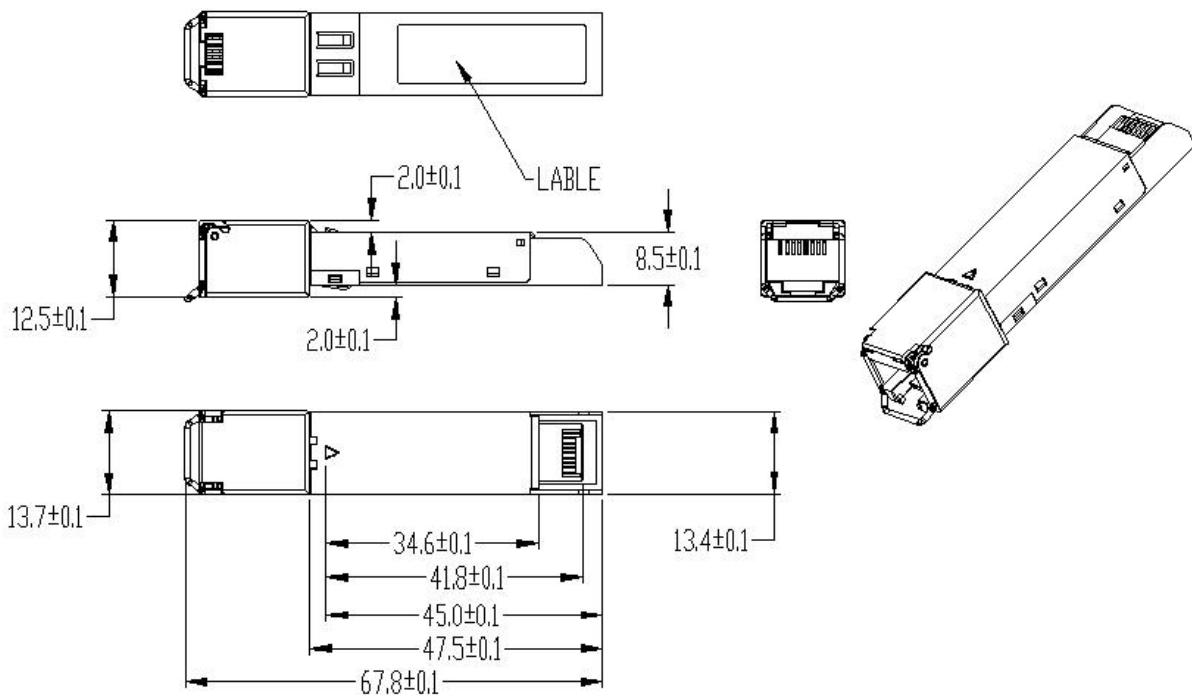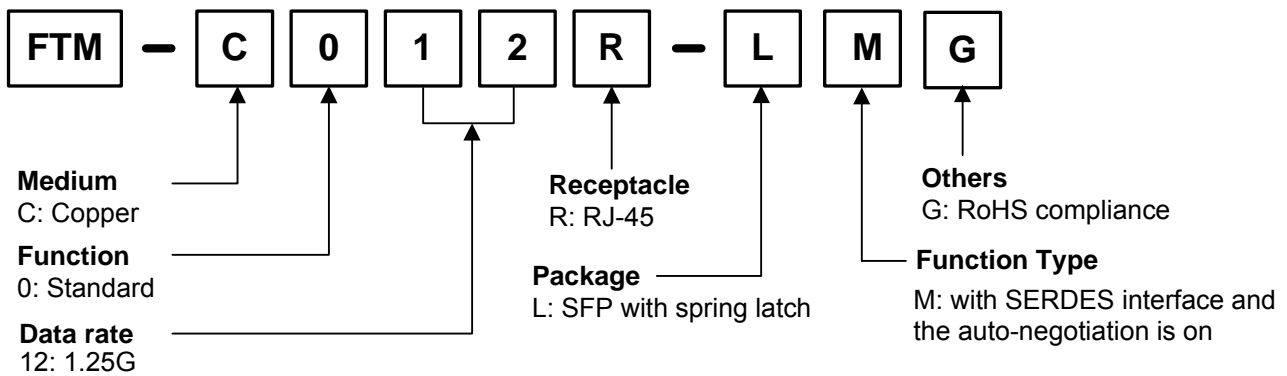
The mechanical design diagram is shown in Figure 4.

Figure 4, Mechanical Design Diagram

Ordering information

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FTM  —  C  0  1  2  R  —  L  M  G
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Medium
C: Copper

Function
0: Standard

Data rate
12: 1.25G

Receptacle
R: RJ-45

Package
L: SFP with spring latch

Others
G: RoHS compliance

Function Type
M: with SERDES interface and the auto-negotiation is on

Part No.	Product Description
FTM-C012R-LMG	1000BASE-T, with SERDES interface, enable the auto-negotiation default, RoHS compliance, Copper SFP with spring latch, -5°C~+70°C Case Temperature

Related Documents

For further information, please refer to the following documents:

- *Fiberxon SFP Application Notes*
- *Fiberxon 1000BASE-T Copper SFP Application Note*
- *SFP Multi-Source Agreement (MSA)*

Obtaining Document

You can visit our website:

http://www.fiberxon.com

Or contact Fiberxon, Inc. America Sales Office listed at the end of documentation to get the latest documents.

Revision History

Revision	Initiate	Review	Approve	Subject	Release Date
Rev. 1a	Unvier.Yang	Funstone.He	Walker.Wei	Initial datasheet	Feb 27. 2006

result in injury or death to persons.

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Contact

U.S.A. Headquarter:

5201 Great America Parkway, Suite 340

Santa Clara, CA 95054

U. S. A.

Tel: 408-562-6288

Fax: 408-562-6289

Or visit our website: http://www.fiberxon.com