VMIVME-7487
486 PC/AT VMEbus CPU
Dual-Port Memory

- 100 percent PC/AT-compatible processor board on VMEbus
- High performance
  - — Available in 66 or 100 MHz CPU clock speeds
- Single slot 6U size
- Coprocessor and 8 Kbyte four-way set associative cache-on-chip (16 Kbyte on DX4 option)
- Up to 16 Mbyte dual-ported DRAM
- Super VGA 1,024 x 768 noninterlaced resolution with 1 Mbyte video DRAM on-board
- One parallel centronics port
- Two serial RS-232C ports
- PC/AT keyboard interface
- Real-time clock with on-board battery
- Floppy and IDE controllers on-board
- Front panel reset button and small speaker included
- Industry-standard gate array technology offers full VMEbus functionality
- Interrupt handler, interrupter, and system controller
- Access all VMEbus memory in real or protected modes
- Three-way byte-swapping hardware for little-endian and big-endian type interfacing in both master and slave modes
- Software drivers for DOS and real-time UNIX
- Diskless operation with optional flash mezzanine board
- Ethernet adapter available

MICROPROCESSOR — High performance is achieved by the use of Intel's industry-standard 80486DX2 66 MHz 32-bit CPU. For even higher performance, the VMIVME-7487 can also be ordered with the 80486DX4 (100 MHz) CPU. The on-chip cache ensures true zero-wait-state operation with hit ratios exceeding 90 percent. For intensive mathematical calculations, the 80486DX models incorporate a high-performance math coprocessor on-chip. Complete software compatibility is ensured with all PC/AT software which supports Intel's family of math chips.

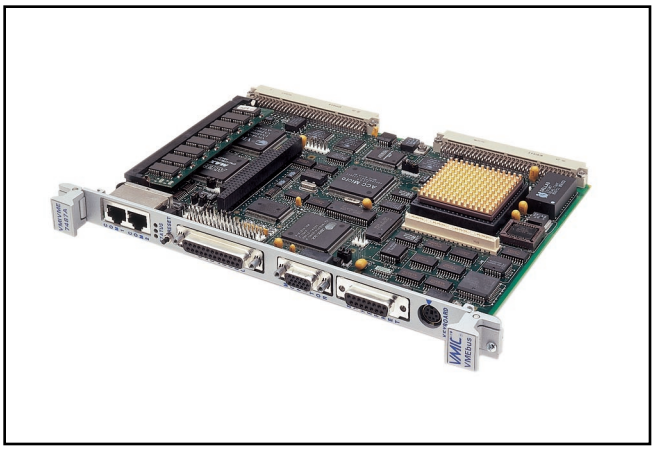
MEMORY — The VMIVME-7487 accepts one bank of 32-bit wide DRAMs with a total maximum capacity of 16 Mbyte. Page mode offers nearly zero-wait-state system performance during burst cache refill mode.

Memory above 640 Kbyte can be configured as Extended, Expanded LIM 4.0, and System and Video BIOS Shadow for improved performance.

The on-board DRAM is dual-ported to the VMEbus. A set of registers enable the dual-port feature of the board as well as the VMEbus base address (A32 or A24), and the size of the memory "window" accessible from the VMEbus, (64 Kbyte increments up to 16 Mbyte).

EPROM — There is a total of 128 Kbyte of EPROM space on the board for the BIOS. Nonvolatile memory expansion is supported by the Flash Mezzanine Option.

SUPER VGA CONTROLLER — The Video interface controller of the VMIVME-7487 is included on the main board with 1 Mbyte DRAM standard. No additional mezzanine boards or VMEbus slots are required.



Resolutions of 800 x 600 256-color and 1,024 x 768 16-color in interlaced and noninterlaced modes are supported.

FLOPPY AND IDE CONTROLLERS — The VMIVME-7487 incorporates both Floppy and IDE Controllers on-board supporting all standard PC/AT drives and formats.

The VMIVME-7487 provides industry-standard interfaces to the VMIVME-7450 which is a dual-slot board containing one 3.5-in floppy and one 3.5-in hard drive. The VMIVME-7450 does not contain any electronics and draws power only from P1.

Ordering Options

Jan. 3, 1996 800-007487-000 C	A	B	C	–	D	E	F
VMIVME-7487 –				–			

A = Memory Size
- 0 = 1 Mbyte
- 1 = 4 Mbyte
- 2 = 16 Mbyte
- 5 = 1 Mbyte with VME64
- 6 = 4 Mbyte with VME64
- 7 = 16 Mbyte with VME64

B = Mezzanine Options
- 0 = None
- 2 = Ethernet
- 3 = Flash Disk

C = CPU Selection
- 0 = Reserved
- 1 = Reserved
- 2 = 66 MHz 486DX2
- 3 = Reserved
- 4 = Reserved
- 5 = 100 MHz 486DX4

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

Ethernet CONTROLLER — The Ethernet Adapter is a small plug-in board compatible with the Novell NE-2000. The 10BASE-T and Thinnet Transceivers are sold separately.

FLASH MEZZANINE — The Flash Mezzanine is a small plug-in board containing 2 Mbyte of flash memory. The user may erase and program the flash disk with MS-DOS® and embedded software. With the custom BIOS supplied with the Flash Mezzanine Option, the VMIVME-7487 may be configured for diskless operation.

SERIAL AND PARALLEL PORTS — Two serial and one Centronics ports are available and accessible through the front panel. Both serial ports support an asynchronous RS-232C interface.

KEYBOARD CONTROLLER AND REAL-TIME CLOCK — The VMIVME-7487 has an on-board PS/2 Keyboard Controller and a compatible connector accessible from the front panel. The on-board real-time clock is fully PC/AT compatible.

RESET SWITCH AND ANNUNCIATORS — A small push-button switch on the front panel will reset the VMIVME-7487. If the System Controller is also enabled, a SYSRESET* will also be generated on the VMEbus.

Three LEDs are also visible on the front panel. A green LED is tied to the +5 V power, a red LED indicates the status of user software, and a yellow LED is illuminated during hard disk accesses.

A small speaker is also included on the VMIVME-7487 to provide compatibility with the PC/AT internal speaker function.

VMEbus MASTER INTERFACE —
MA32:MBLT32:MBLT64 (Option)
(A32:A24:A16:D32:D16:D8 (EO):BLT32)
(BLT64 when VME64 option is ordered)

When the 80486 microprocessor is in protected mode, the VMEbus is accessed using a 16 Mbyte window. VMEbus address A31 to A24 are driven from the extended address 8-bit page register. 80486 address signals A31 to A24 are decoded to provide 16 unique 16 Mbyte regions. Each region generates a unique address modifier code for the desired address width (A32/A24/A16) and access type (supervisory or nonprivileged, code or data). The 80486 address decode also allows user-defined address modifier codes to be output when accessing a specific 16 Mbyte region.

When the 80486 microprocessor is operating in real mode, the VMEbus is accessed using a 64 Kbyte window at E0000H. VMEbus A31 to A24 are driven from the extended address page register. VMEbus A23 to A16 are driven from the standard address page register which is only activated when in real mode.

VMEbus SLAVE INTERFACE —
Memory Access
SAD032:SD32:SBLT32:SBLT64 (Option)
A32:A24:A16:D32:D16:08 (EO): BLT32)
(BLT64 when VME64 option is ordered)
The VMIVME-7487 slave interface provides access to the on-board DRAM as well as to mailbox registers which are used for communication between VMEbus and the 80486 microprocessor.

The interface allows access to the on-board DRAM. The amount (window size) of DRAM accessible from the VMEbus is programmable in increments of 64 Kbyte up to 16 Mbyte.

MAILBOX ACCESS — Access to mailbox registers is provided using A16/D8(O) VMEbus accesses only.

MAILBOXES — The VMIVME-7487 provides four mailboxes which are accessible from both the 80486 and the VMEbus providing interprocessor communication. The mailboxes have the ability to interrupt the 80486 when accessed by VMEbus.

VMEbus REQUESTER — The VMIVME-7487 allows the 80486 to request and gain control of the bus using any of the VMEbus request lines, (BR3*-BR0*), under software control. The requester can be programmed to operate in any of the following modes:

Release-On-Request (ROR)
Release-When-Done (RWD)
Release-On-Clear (ROC)
VMEbus Capture and Hold (BCAP)

INTERRUPT HANDLER — The VMIVME-7487 incorporates an Interrupt Handler which monitors all VMEbus IRQ* lines. The handler can be programmed to respond to interrupts on any or all of the IRQ* inputs.

All normal-process VMEbus-related interrupts are connected to the IRQ11 and IRQ12 PC/AT interrupt. These include:

Mailbox interrupts
VMEbus interrupts
VMEbus interrupter IACK cycle (acknowledgment of VMIVME-7487 VMEbus-issued interrupts)

All error processing VMEbus-related interrupts are connected to the PC/AT NMI interrupt. These include:

ACFAIL* interrupt
BERR* interrupt
SYSFAIL* interrupt
Software NMI

Each interrupt source can be programmed with a unique vector. This allows both the non-NMI and NMI interrupt service routine to simply read an interrupt acknowledge register. The returned ID will correspond to the highest priority interrupt pending.

INTERRUPTER — The VMIVME-7487 can issue interrupts on any or all of the seven VMEbus interrupt lines (IRQ7* to IRQ1*) under program control. An ID Register is associated with each interrupt line. During the interrupt acknowledge cycle, the interrupter issues the ID associated with the IRQ* being acknowledged.

The interrupter also provides an interrupt acknowledge ID Register that can be programmed with a unique ID to allow interrupt processing software to know when a specific interrupt has been acknowledged by the VMEbus interrupt handler.

SYSTEM CONTROLLER — The on-board VMEbus System Controller allows the board to work at slot 1, or it may be disabled when another board is acting as the system controller.

The System Controller can be programmed under software control to provide the following modes of arbitration:

Round Robin (RRS)
Single Level (SGL)
Priority (PRI)

The System Controller provides a SYSCLK driver, IACK* Daisy-Chain Driver, and a VMEbus Access Time-Out Timer. The SYSTEM controller also provides an arbitration time-out if BBSY* is not seen within 10 ms after a BGOUT* signal is issued.

BYTE SWAPPING — The Intel 80x86 family of processors use little-endian format. To accommodate other VMEbus modules which transfer data in big-endian format, such as the 680x0 processor family, the VMIVME-7487 incorporates Byte Swapping hardware.

The byte swapping hardware provides independent byte swapping for both the Master and Slave interface. Both Master and Slave interface byte swapping is programmed under 80486 software control.

SOFTWARE — The VMIVME-7487 is 100 percent PC/AT compatible and in addition to MS-DOS it can run Microsoft Windows in Enhanced mode, DR-DOS, OS/2, O/S 9000, SCO Xenix, UNIX, and other operating systems.

VMIC's **VMEaccess™** and **IOWorks Access™** software are sets of development tools and run-time software which support the management of VMEbus functions in applications containing any of VMIC's CPU modules.

SPECIFICATIONS

6U double Eurocard format, single slot

Height	9.2 in (233.4 mm)
Depth	6.3 in (160 mm)
Thickness	0.8 in (20.3 mm)

Power Requirements:
+5 VDC (±5 percent), 3.0 A (typical), 4 A maximum

+12 VDC (±5 percent), 25 mA (typical), 50 mA maximum

-12 VDC (±5 percent), 25 mA (typical), 50 mA maximum
Note: The currents at +12 and -12 VDC are specified with the serial connectors open.

Operating Temperature:
0 to 55 °C Forced air cooling required

Relative Humidity: 10 to 90 percent, noncondensing

VMEbus Interface:

DTB Master:	BLT32 (BLT 64 with VME64 option) A32/D32, A24/D32, A16/D32
DTB Slave:	BLT32 (BLT 64 with VME64 option) A32/D32, A24/D32 DRAM access
DTB Slave:	A16/D8(O) Interprocessor communication
Requester:	Programmable, BR(3-0), ROR, RWD, BCAP, ROC
Interrupt Handler:	IH(1 to 7) D8(O)
Interrupter:	Programmable, IRQ7* to IRQ1*

Arbiter:	SGL, PRI, RRS
BTO:	10 µs
Compliance:	Rev. C.1

TRADEMARKS