General Standards Corporation

High Performance Bus Interface Solutions

PC104P-16AO12

12-Channel 16-Bit High-Speed Analog Output PC104 Plus Board

With 400,000 Samples per Second per Channel, and Simultaneous Clocking

Features Include:

- 12 Precision High-Speed Analog Output Channels;
- 16-Bit Resolution; D/A Converter per Channel
- Data Rates to 400K Samples per Second per Channel; 4.8 MSPS Aggregate Rate
- Output Ranges of ±10V, ±5V or ±2.5V
- Output Clocking Mode Selectable as Simultaneous or Sequential
- 32, 64 or 128K-Sample Analog Output FIFO Buffer is Configurable as Open or Circular
- Continuous and Burst (One-Shot) Output Modes Support Seamless Waveform Sequencing
- Data Rate Controlled by Adjustable Internal Clock, or by Externally Supplied Clock
- Supports Multiboard Synchronization;
- Optional Differential Clock output Available for Synchronizing Sigma-Delta A/D Boards
- Internal Autocalibration of all Channels
- Remote Ground Sensing
- Output Data Buffer Size Adjustable up to 32K, 64K or 128K Channel Samples
- High Accuracy; 0.017% FSR max error on ±10V Range, INL = 0.007%
- Fast Settling; 5 us to 0.1%; 8 us to 0.01%;with No-filter Option
- VxWorks™ and NT Drivers™ can be provided.

Applications Include:

- ✓ Precision Voltage Source
- ✓ Industrial Robotics
- ✓ Audio Synthesis
- ✓ Acoustic Research
- ✓ Process Monitoring
- ✓ Waveform Synthesis
- ✓ Acoustic Research

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Overview:

The 12-channel PC104P-16AO12 analog I/O board provides precision high-speed 16-bit analog output capability. Twelve analog output channels are updated simultaneously from an internal buffer, either at a software-determined rate, or by an externally supplied clock. Flexible operating modes include continuous, periodic and triggered-burst functions, as well as the seamless, dynamic concatenation of waveforms in real-time. Output ranges are supplied as ±10V, ±5V or ±2.5V.

Internal auto calibration networks permit periodic calibration to be performed without removing the board or host from the system. This feature produces the optimum calibration situation, in which the board is calibrated in its actual operating environment.

Functional Description:

The PC104P-16AO12 board contains twelve 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed analog output capability. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.1, and supports the "plug-n-play" initialization concept. Unique FIFO buffer controls support the seamless sequencing of successive waveforms. In less demanding applications, the outputs can be updated individually. An optional clock output for synchronizing Sigma-Delta ADC boards is available.

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 16-bit local bus (Figure 1). Twelve analog output channels are controlled through an analog output FIFO buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator, or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including auto calibration. Analog output levels are initialized to zero (midrange). Multiboard synchronization is supported.

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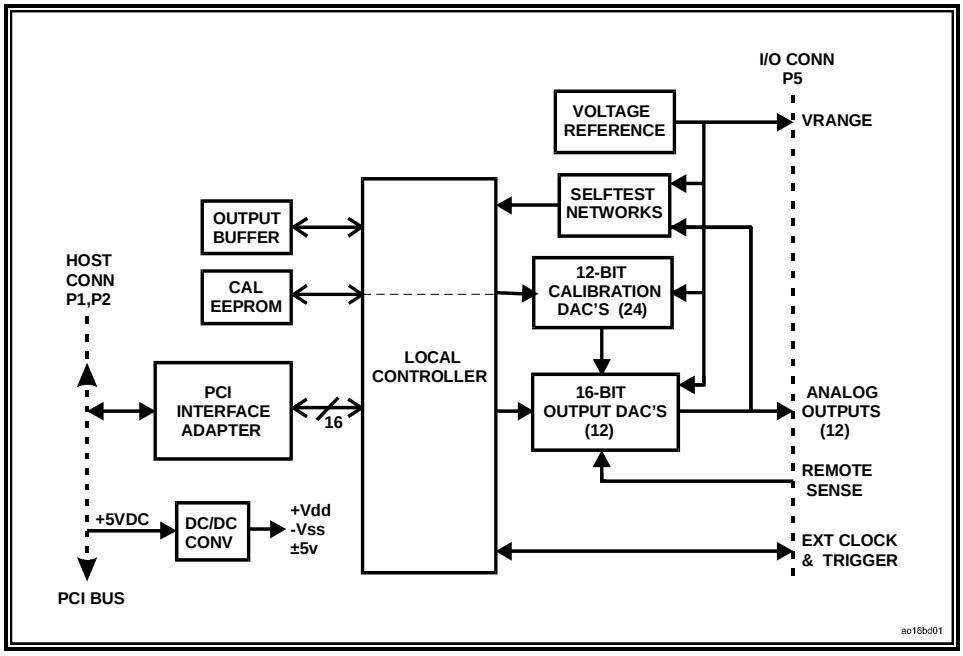

Figure 1. PC104P-16AO12 Board; Functional Organization

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 50-pin, dual-ribbon front-access I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Selftest networks permit all channels to be calibrated automatically to a single internal voltage reference. Offset and gain trimming of the output channels is performed by calibration DAC's that are loaded with channel correction values during initialization. The correction values are determined during auto calibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's. Either auto calibration or initialization can be invoked at any time by asserting a single control bit in the board control register.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

ANALOG OUTPUT CHANNELS

❑ Output Characteristics:

Configuration:	Twelve single-ended analog output channels, with dedicated 16-Bit DAC per channel; Optional 4-channel and 8-Channel configurations available.
Voltage Ranges:	Factory configured as ±10 Volts, ±5 Volts or ±2.5 Volts
Output Resistance:	1.0 Ohm maximum
Output protection:	Withstands sustained short-circuiting to ground without damage
Load Current:	±5 ma maximum; ±2 ma recommended for minimum crosstalk and line loss
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Settling Time:	No Filter : 5 us to 0.1%, 8 us to 0.01% 10 kHz Filter: 130 us to 0.1%, 160 us to 0.01%
Noise:	No Filter: 4 mVRMS, 10Hz-10KHz 10 kHz Filter: 2 mVRMS, 10Hz-10KHz
Glitch Impulse:	±2.5V Range: 3 nV-Sec max. ±5V Range: 5 nV-Sec ±10V Range: 8 nV-Sec
Remote Sensing:	Single input pin compensates for ground potential at load. Maximum range ±1.0 Volt. Correction ±1 percent. Enabled or disabled by control software.

❑ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Clocking Rate:	Internal Rate Clock: 460 to 400,000 samples per second per channel External Rate Clock: 0 to 400,000 samples per second per channel

DC Accuracy:
(Max error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±2.4mv	±3.3mv
±5V	±1.7mv	±2.2mv
±2.5V	±1.4mv	±1.6mv

Bandwidth: (Single-pole lowpass)	No output filter option: 300 kHz typical 10 kHz filter option: 10 kHz typical
Crosstalk Rejection:	80 dB minimum, DC-10 kHz
Integral Nonlinearity:	±0.007 percent of FSR, maximum

Differential Nonlinearity: ±0.003 percent of FSR, maximum

❑ Operating Modes and Controls

Sample Clock Source:	Internal rate generator, external TTL hardware clock input, or software clock. An external TTL clock output can be used for synchronization of multiple PC104P-16AO12 boards together. An optional differential clock output is available for synchronizing sigma-delta A/D boards to a PC104P-16AO12 board. The optional clock output frequency is adjustable from 16MHz to 32MHz with 0.2 percent resolution, and is derived from the local crystal-controlled master clock. An internal divider in the PC104P-16AO12 permits the adjustable clock output and the local output sampling clock to be phase-locked in integer frequency ratios from a common clock. This option is referred to in the ordering and pin out information and as Differential Sync I/O, and provides a differential interface for all digital signals at the I/O connector.
Burst Trigger:	Software control bit, or external TTL trigger input (Optional differential LVDS). Burst triggering also can be obtained from an external source.
Update Mode:	Simultaneous or channel-sequential output updating
Active Buffer Size:	From 4 output values to 32K, 64K, or 128K-values, in 2:1 steps.
Buffer Mode:	Selected as Circular for periodic waveforms, or as Open for one-shot functions
Data Format:	Software selected as offset binary or Two's complement

AUTOCALIBRATION

During auto calibration, all analog channels are calibrated to a single precision internal voltage reference that is adjustable with a single trimmer. Correction values determined during auto calibration are retained in nonvolatile EEprom, and are restored automatically during initialization. Auto calibration has a typical duration of 3-5 seconds, and can be invoked at any time after initialization by asserting a single control bit

PCI INTERFACE

❑ **Compatibility:** Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers as bus master.

❑ **Board Control and Data Registers** (All registers except the output buffer are 16 Bits)**:**

Board Control Register:	Determines the principal operating mode
Channel Selection:	Selects active analog output channels
Sample Rate Control:	Controls the internal sample-rate generator
Buffer Operations:	Controls buffer size and mode; provides buffer status flags
Output Data Buffer:	Analog output buffer (17 bits, including end-of-frame (EOF) flag).

A single interrupt request can be programmed to occur in response to specific internal conditions.

❑ **Analog Output Buffer**

Analog output data is written to the board through a single 16-bit register that serves as a FIFO buffer port. The buffer is 17 bits wide, has a software-controlled capacity of from 4 values to 32K output values (or optional 64K or 128K), and is right justified to the LSB in the D32 PCI data path. Output data is a 16-bit field that is software-configurable in either Two's complement or offset binary format. The 17th bit is used as an end-of-frame (EOF) flag for tracking functions through the buffer.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ **Power Requirements**

+5VDC ±0.2 VDC at 1.0 Amps, maximum, 1.1 Amps typical
Power Dissipation: 7.0 Watts maximum; 5.5 Watts typical

❑ **Physical Characteristics** (Overall, excluding spacers)**:**

Height:	23.3 mm (0.92 in)
Width:	94.0 mm (3.78 in)
Depth:	95.9 mm (3.70 in)

❑ **Environmental Specifications**

Ambient Temperature Range:	Operating: 0 to +70 degrees Celsius * Storage: -40 to +85 degrees Celsius *Temperature of inlet cooling air.
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling

❑ **Cooling Requirements**

Conventional air cooling; 200 LPFM (typical mezzanine environment).

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ORDERING INFORMATION

Specify the basic product model number (PC104P-16AO12), followed by an option suffix "-ABCDE", as indicated below. For example, model number PC104P-16AO12-10201 describes a board with a ±5 Volt output range, no output filter, 12 output channels, a 32K-Sample buffer, and single-ended sync I/O.

Optional Parameter	Value	Specify Option As:
Output Range:	±2.5 Volts	A = 0
	±5 Volts	A = 1
	±10 Volts	A = 2
Output Lowpass Filter:	No output Filter	B = 0
	10 kHz Output Filter	B = 1
	100 kHz Output Filter	B = 2
Number of Output Channels:	4 Channels	C = 0
	8 Channels	C = 1
	12 Channels	C = 2
Output Buffer Size:	32K Samples	D = 0
	64K Samples	D = 1
	128K Samples *	D = 2
Sync I/O Configuration	Non-differential I/O (TTL)	E = 1
	Differential I/O (LVDS), R402 Termination Installed	E = 2
	Differential I/O (LVDS), R402 Termination Omitted	E = 3
	Differential External Rate Generator I/O (LVDS)**	E = 4
	Non-differential External Rate Generator I/O (TTL)**	E = 5

* Contact factory for availability.

** This option is needed for synchronizing multiple PMC-16AO12 boards with other GSC products.

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SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

P5A		P5B	
PIN	SIGNAL	PIN	SIGNAL
1	OUTPUT RETURN	1	OUTPUT RETURN
2	OUTPUT CHANNEL 00	2	REMOTE GROUND SENSE
3	OUTPUT RETURN	3	OUTPUT RETURN
4	OUTPUT CHANNEL 01	4	OUTPUT RETURN
5	OUTPUT RETURN	5	VRANGE RETURN
6	OUTPUT CHANNEL 02	6	VRANGE OUTPUT
7	OUTPUT RETURN	7	VRANGE RETURN
8	OUTPUT CHANNEL 03	8	OUTPUT RETURN
9	OUTPUT RETURN	9	OUTPUT RETURN
10	OUTPUT CHANNEL 04	10	OUTPUT RETURN
11	OUTPUT RETURN	11	OUTPUT RETURN
12	OUTPUT CHANNEL 05	12	OUTPUT RETURN
13	OUTPUT RETURN	13	OUTPUT RETURN
14	OUTPUT CHANNEL 06	14	OUTPUT RETURN
15	OUTPUT RETURN	15	OUTPUT RETURN
16	OUTPUT CHANNEL 07	16	OUTPUT RETURN
17	OUTPUT RETURN	17	DIGITAL RETURN
18	OUTPUT CHANNEL 08	18	TRIG INPUT *
19	OUTPUT RETURN	19	TRIG INPUT RETURN *
20	OUTPUT CHANNEL 09	20	TRIG OUTPUT *
21	OUTPUT RETURN	21	TRIG OUTPUT RETURN *
22	OUTPUT CHANNEL 10	22	CLOCK I/O **
23	OUTPUT RETURN	23	CLOCK I/O RETURN **
24	OUTPUT CHANNEL 11	24	CLOCK OUTPUT *
25	OUTPUT RETURN	25	CLOCK OUTPUT RETURN *

* Available optionally as LVDS differential pairs (Differential Sync I/O option).

** Differential pair in the Differential Sync I/O configuration; selectable as either an input or an output clock signal.

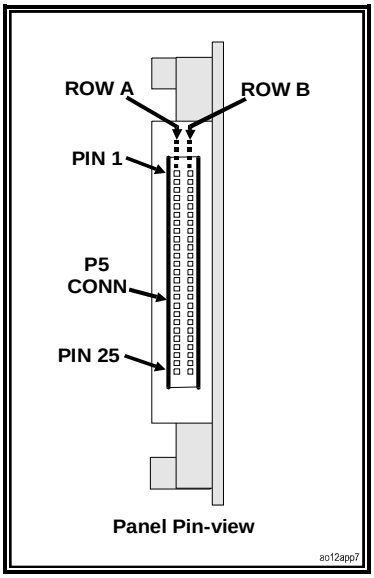

Figure 2. System Input/Output Connector

System Mating Connector:
Standard 50-pin 0.050"
Dual-ribbon socket connector;
Robinson Nugent # P50E-050-S-TG.