# **Industry Pack Modules**



## IP501-x Serial 422/485 Communication

These modules provide an asynchronous serial communication interface for your system. They have four asynchronous, full-duplex RS422B serial ports. Since the transceivers are compatible with the RS485 standard, you can also use a full-duplex RS485 interface for multiple driver support. However, for true half-duplex RS485 operation, use the IP502.

Software-configuration quickly sets the baud rate, character-size, stop bits, and parity.

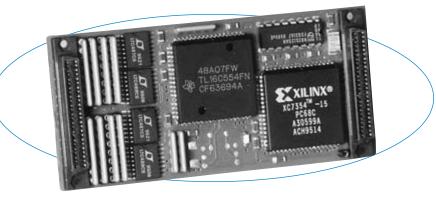
For more efficient data processing, each serial port is equipped with 16, 64 or 128-character FIFO buffers on the transmit and receive lines.

### Features

- Four asynchronous, full-duplex RS422B serial ports (full-duplex RS485)
- 16,64, or 128-byte FIFO buffers
- Programmable baud rate (up to 512Kbps) (Consult factory for custom rates up to 1Mbps)
- Individually controlled interrupts (unique vectors for each port)
- Handshake control signals (RTS, CTS) for each channel
- Extended temperature option (-40 to 85°C)
- Industry-standard 16C550 family UART includes software-compatible 16C450 mode

## **Benefits**

- Failsafe receivers guarantee a high output state when the inputs are left open or floating.
- Internal diagnostics help detect faults.
- FIFO buffers minimize CPU interaction for improved system performance.



Large, 128-byte FIFO buffers reduce the processing burden on the CPU to increase the overall system performance.

## **Specifications**

### **RS422B Serial Ports**

- Configuration: Four independent, non-isolated RS422B serial ports with a common single return connection.
- Data rate: Programmable up to 512K bits/second using internal baud rate generator. Consult factory for custom baud rates up to 1M baud.

Interface: Asynchronous serial only.

- Character size: 5 to 8 bits, software-programmable.
- Parity: Odd, even, or no parity; software-programmable.
- Stop bits: 1, 1-1/2, or 2 bits; software-programmable.
- Interrupts: Receiver line status (overrun error, parity error, framing error, or break interrupt); received data available (FIFO level reached) or character time-out; transmitter holding register empty; or modem status (CTS). Multiple ports share the IntReq0 line according to a shifting priority scheme based on the last interrupting port serviced.

#### UART

IP501-16: Texas Inst. TL16C554FN or equivalent. IP501-64: Startech ST16C654CJ68. IP501-128: Exar/Startech XR16C854

### IP Compliance (ANSI/VITA 4)

Meets IP specifications per ANSI/VITA 4-1995. IP data transfer cycle types supported:

Input/output (IOSel\*), ID read (IDSel\*).

Access times (8MHz clock): ID PROM read: 1 wait state (375nS cycle). Channel register read/write: 2 wait states (500nS cycle). Interrupt select read: 2 wait states.

### Environmental

Operating temperature: 0 to 70°C (IP501-16/64/128) or -40 to 85°C (IP501-16E/128E).

Storage temperature: -40 to 125°C (all models).

Relative humidity: 5 to 95% non-condensing.

Power:  $\pm$ 5V ( $\pm$ 5%): 650mA maximum.  $\pm$ 12V ( $\pm$ 5%) from P1: 0mA (not used). MTBF: Consult factory.

## **Ordering Information**

#### Industry Pack Modules IP501-16

Four serial ports with 16-byte FIFOs.

### IP501-16E

Same as IP501-16 plus extended temperature range

IP501-64 Four serial ports with 64-byte FIFOs

### IP501-128

Four serial ports with 128-byte FIFOs

### IP501-128E

Same as IP501–128 plus extended temperature range For Industry Pack Carrier Cards, see Page 5.

#### Customized Industry Pack Modules †4861-x

Modified IP501-16 with user specified crystal/baud rate.

### <sup>+</sup>4988-x

Modified IP501-64 with user specified crystal/baud rate.

†5024-x

Modified IP501-128 with user specified crystal/baud rate.

*†* Specify x = crystal frequency when ordering. Minimum quantity per order is two units.

For Industry Pack Carrier Cards, see Page 5.

Software (see Page 81) IPSW-API-VXW

VxWorks<sup>®</sup> software support package

IPSW-API-QNX QNX<sup>®</sup> software support package

### IPSW-ATX-PCI

ActiveX"/OLE Controls 2.0 software package For accessories information, see Page 87.