EPC® - 7

Hardware Reference

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1. Product Description

This manual contains all the information needed to install and use the EPC-7 VXIbus embedded computer. Additional user and programmer manuals discuss the use of the EPConnect software package designed to work with the EPC-7.

The EPC-7 is a C-size VXIbus embedded computer based on the Intel 486 processor. It can perform 8-, 16-, and 32-bit VXIbus data transfers, both as master and slave, and can be the slot-0 and system controller and resource manager. The EPC-7 can be an interrupter and interrupt handler, and can drive and sample the TTL and ECL trigger lines.

The EPC-7 is compatible with the IBM PC architecture and contains standard front-panel connectors for PC serial and parallel ports. The keyboard port is PS/2 style. In addition, the front panel contains a SCSI-2 port and cable connectors for external clock and trigger signals.

Depending on the model, the EPC-7 contains three or four front-panel expansion slots for EXM modules. Also, the particular model of the EPC-7 will determine such attributes as the speed of the 486 processor, the size of the internal hard disk, the amount of the DRAM memory, and whether a floppy diskette drive is present.

Specifications

The following tables define the power and environmental specifications of the EPC-7. They do not include any EXM modules in the EPC-7.

The following are the environmental specifications of the EPC-7 when it contains no internal disk drives.

Characteristic		Value
Environmentals		
Temperature	operating	0°C - 60°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 10,000 ft (3,000m) 2°C per min max excursion gradient
	storage	-40 - 85°C 5°C per min max excursion gradient
Cooling		For 10°C rise, airflow of 2 liters per second against 0.014mm H_2O backpressure
Humidity	operating	5% - 95% noncondensing
	storage	5% - 95% noncondensing
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 40,000 ft (12,000 m)
Vibration	operating	0.015 inch (0.38 mm) P-P displacement with 2.5 g peak (max) acceleration over 5-2000 Hz
	storage	0.030 inch (0.76 mm) P-P displacement with 5.0 g peak (max) acceleration over 5-2000 Hz
Shock	operating	30 g, 11 ms duration, half-sine shock pulse
	storage	50 g, 11 ms duration, half-sine shock pulse

Table 1. EPC-7 Environmental Specifications With No Internal Disk Drives.

The following are the environmental specifications of the EPC-7 when it contains floppy and hard disk drives.

Characteristic		Value
Temperature	operating	5°C - 45°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 10,000 ft (3000m) 10°C per hour max excursion gradient
	storage	-40°C - 70°C 2°C per hour max excursion gradient
Cooling		For 10°C rise, airflow of 2 liters per second against 0.014mm H_2O backpressure
Humidity	operating	20% - 80% noncondensing 26°C max wet bulb
	storage	5% - 95% noncondensing 48°C max wet bulb
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 40,000 ft (12,000 m)
Vibration	operating	0.015 inch (0.38 mm) P-P displacement with 0.6 g peak (max) acceleration over 5-500 Hz
	storage	0.030 inch (0.76 mm) P-P displacement with 2.0 g peak (max) acceleration over 5-500 Hz
Shock	operating	5 g, 11 ms duration, half-sine shock pulse, no soft errors, 10 g with 1 soft error per block
	storage	10 g, 11 ms duration, half-sine shock pulse

Table 2. EPC-7 Environmental Specifications With Floppy and Hard Drives.

The following table contains additional specifications. Power and current are measured with hard and floppy drives and no EXMs.

Characteristic		Value
Electrical		
Current	+5V	6.0 A typ, 7.0 A max (33 MHz) 7.0 A typ, 8.0 A max (50 MHz) 7.5 A typ, 8.5 A max (100 MHz)
	+12V	1.1 A max for first 10 sec after power on for hard-drive spin up, 0.5 A max thereafter
	-12V	0.1 A max
	-5.2V	0.3 A max
	-2V	0.12 A max
Other		
Weight	without EXMs	5.5 lb (2.6 kg)
VME	master address	A16, A24, A32
	master transfer	D08(EO), D16, D32, RMW
	slave address	A16, A24, A32
	slave transfer	D08(EO), D16, D32, RMW
	interrupter	I(1-7)
	interrupt handler	D08(O),D16 IH(1-7)
	requester	ROR,RONR
	arbiter	RRS,PRI
	system controller	SYSCLK, IACK daisy chain, bus timer
VXI	device type	message based
	protocols	cmdr/master/interrupter
	manufacturer code	4076 - RadiSys Corporation
	model code	239 (if configured for slot 0) 495 (if configured for not slot 0)

Table 3. Additional EPC-7 Specifications.

2. Before Installation

2 2

Before installing the EPC-7, unpack and inspect it for shipping damage.

- **DO NOT REMOVE ANY MODULES FROM THEIR ANTI-STATIC BAGS UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT. THE EPC-7 MODULES, LIKE MOST OTHER ELECTRONIC DEVICES, ARE SUSCEPTIBLE TO ESD DAMAGE. ESD DAMAGE IS NOT ALWAYS IMMEDIATELY OBVIOUS, IN THAT IT CAN CAUSE A PARTIAL BREAKDOWN IN SEMICONDUCTOR DEVICES THAT MIGHT NOT IMMEDIATELY RESULT IN A FAILURE.**

- **THE EPC-7 CONTAINS A HARD DISK. PLEASE HANDLE IT WITH CARE.**

Configuring the EPC-7 Jumpers

Slot 0 and System Controller Configuration

Before installing the EPC-7 in a VXIbus chassis, a decision must be made whether the EPC-7 is to be the slot 0 controller and the VMEbus system controller. Every VXIbus system needs a module that performs the VMEbus system controller functions (generation of the 16 MHz SYSCLK signal, arbitration of the bus, detection of bus timeout conditions, and initiation of the interrupt-acknowledge daisy chain), and the VXIbus slot-0 functions (generation of the 10 MHz ECL CLK10 signals and control of the MODID module identification function).

Typically, the same device is the slot-0 controller and VMEbus system controller.

The EPC-7 is shipped configured as a VXI slot 0 controller. If this is the intended use of the EPC-7 (which will usually be the case), skip the rest of this section.

The EPC-7 has nine jumper positions appearing through its rear panel between the P1 and P2 connectors. See Figure 1 below.

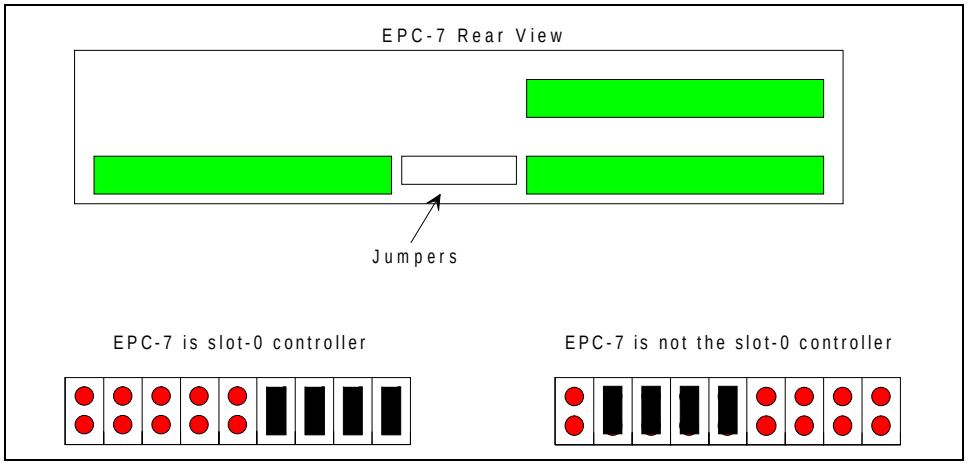


Figure 1. EPC-7 Configuration Jumpers.

There are several readily apparent consequences of incorrectly configuring the EPC-7 configuration jumpers.

- Resource manager reports a system configuration differing widely from the actual configuration
- Power-on selftest reports a VXI failure.
- CLK10+ and CLK10- signals are not being driven or are out of spec on the backplane.
- The system resource manager could not detect the presence of a non-slot-0 EPC-7.
- Power-on selftest reports NO SYSCLK.
- System hangs, typically while running the resource manager.

If any of these conditions occur, check the configuration jumpers on the back of the EPC-7.

Installing the VXIbus Backplane Jumpers

The VXIbus contains several daisy-chained control signals. Most VXIbus backplanes contain jumpers or DIP switches for these control signals to allow systems to operate across empty slots. Failing to install these jumpers properly is a common source of problems when integrating a new VXIbus system. In this manual, these jumpers or DIP switches will be referred to as jumpers.

The VXIbus specification provides 4 bus grant signals (`BG0 - BG3`) and 1 interrupt acknowledge signal (`IACK`) via daisy-chain lines. Per the VXIbus specifications, all boards are required to correctly handle these signals. All slots that do not have a board plugged into the backplane (i.e. empty slots and slots occupied by some multi-slot instruments), need to be jumpered to allow the signals to pass through to other instruments in the system.

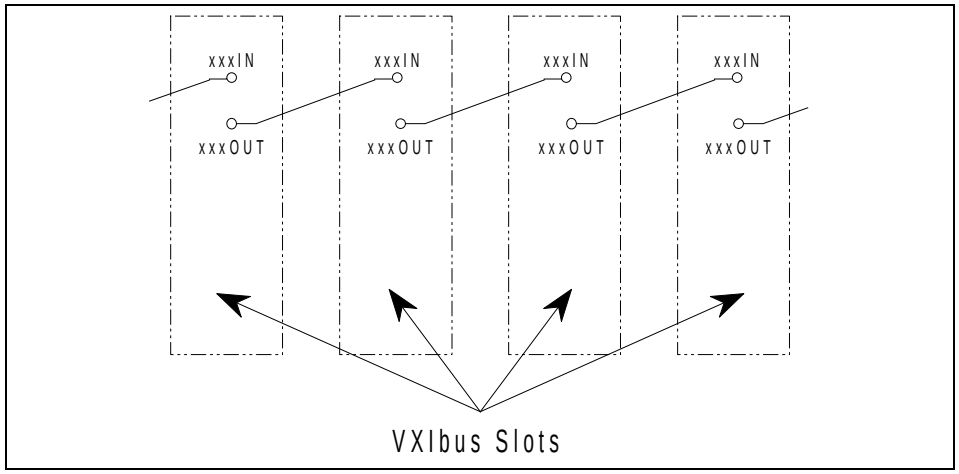
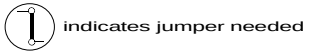


Figure 2. Daisy-Chain Signal Concept.

The Slot-0 controller board initiates each daisy-chain signal. Each VXIbus slot to the right of the Slot-0 controller must pass through each of the daisy-chain signals. For each VXIbus slot, `xxxIn` pin must be connected to its corresponding `xxxOut` pin (e.g. `BG0In` to `BG0Out`, `BG1In` to `BG1Out`,...,`IackIn` to `IackOut`) either through the board in that slot or by jumpers.

Some boards correctly pass all of these signals, some boards handle some of these signals and not others, and some boards (typically "dumb" slave boards) may not

handle any of these signals. Check the manual for each board to be installed to determine if these signals are passed through correctly. If they are not or if the VXIbus slot is empty, all (or some) of these signals must be jumpered. See Figure 3 below.



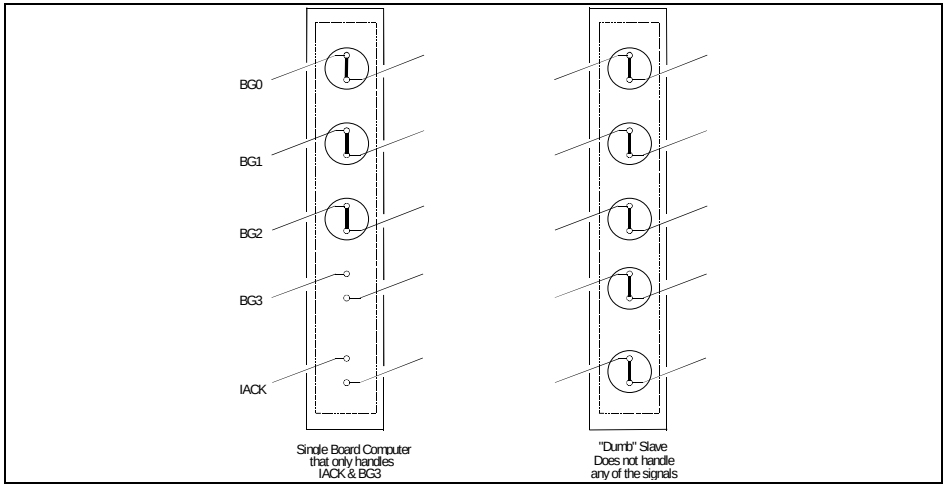


Figure 3. VXIbus Backplane Jumper Examples.

Now that you have determined where the jumpers need to be, you must determine how to jumper your particular backplane. VXIbus chassis provide jumper connections in one of three ways; stake pins, DIP switches, or auto jumpering. If the chassis in use auto-jumpers the daisy-chain signals, proceed to the next chapter.

Different backplane manufacturers handle jumpers and DIP switches in different ways; some provide stake pins on the rear of the backplane while others provide stake pins or DIP switches on the front of the backplane. These stake pins can be located in several different places.

If the stake pins are on the rear of the backplane, the most common place is in the middle of the J1 connector as shown in Figure 5 below. This can be just these pins extended or all pins extended for wirewrapping.

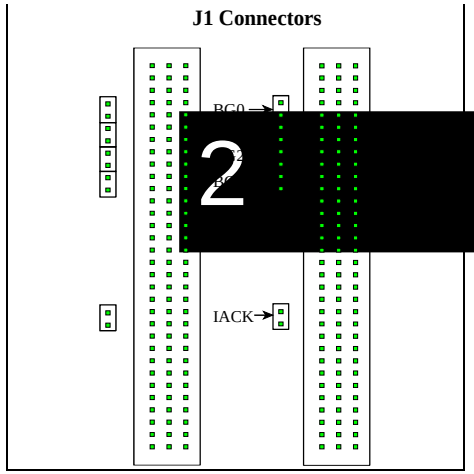


Figure 4. VXIbus Jumpers or DIP Switches on Front of Chassis.

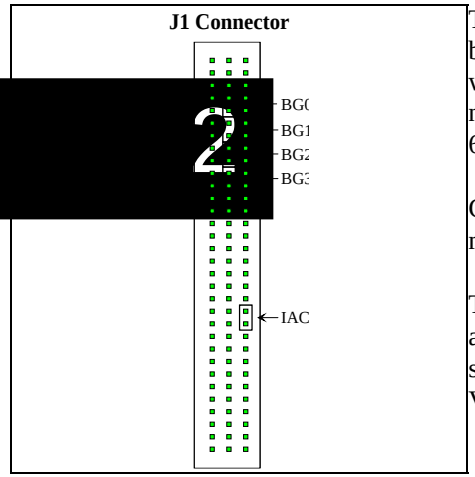


Figure 5. VXIbus Jumpers on Rear Wirewrap Pins.

The stake pins (front or rear) can also be located adjacent to the slot being jumpered as shown in Figure 4 above. Typically, the stake pins will be located between the slot being jumpered and the next lower-numbered slot (e.g. jumpers for Slot 6 would be located adjacent to Slot 6 between Slots 5 and 6).

Consult your VXI chassis reference manual or contact the chassis manufacturer if you are unsure where to jumper your particular system.

The EPC-7 occupies two VXI slots and correctly handles all bus grant and IACK signals for both slots. No jumpers are needed for these two slots. If an EPC-7AM or EPC-7MC is also being used, it occupies a third VXI slot. Jumpers must be installed for this slot.

NOTES

3. Installation

EPC-7 Insertion

The EPC-7 is inserted in a VXIbus card cage in the following way:

1. Make sure that power to the VXI system is off. The modules are not designed to be inserted or removed from live backplanes.
2. Align the EPC-7 to adjacent top and bottom card guides in the VXI chassis.
3. Slide the EPC-7 module into the chassis. Use firm pressure on the handles to mate the module with the backplane connectors.
4. Tighten the screws in the top and bottom of the front panel to ensure proper connector mating and prevent loosening of the module via vibration.

Note that the EPC-7 has a front-panel key adhering to the VXIbus specification that prevents its insertion to the right of certain other types of modules. These keys prevent problems associated with incompatible signal levels on the VXI daisy-chained Local Bus. Although the EPC-7 does not use the Local Bus, its ability to be a slot-0 controller means that it uses what would otherwise be "leftside" Local Bus lines for TTL MODID lines. Therefore the key prevents the EPC-7 from being installed to the immediate right of a module keyed for a "rightside" ECL, analog, or sensor Local Bus.

EXM Module Insertion

Your EPC-7 will typically have several EXM expansion modules for such purposes as a video controller, network interface, and GPIB interface. If an EXM needs to be removed or replaced, loosen the two thumbscrews on the EXM and gently pull it out of its rear connector.

To insert an EXM, slide the EXM into place in the card guides, push firmly on the EXM front panel to seat the rear cardedge connector, and tighten the thumb screws on the EXM's face plate.

- **MAKE SURE THAT POWER TO YOUR VXI SYSTEM IS OFF. EXMS ARE NOT DESIGNED TO BE INSERTED OR REMOVED FROM LIVE SYSTEMS.**

- **WHEN INSERTING AN EXM, AVOID TOUCHING THE CIRCUIT BOARD, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

3 3

Connecting Peripherals to the EPC-7

The final step of installation is connecting peripherals, typically a video display and keyboard, but also perhaps a mouse, modem, printer, etc. Unless otherwise noted, all connectors are compatible with those found on IBM-compatible desktop PCs. Detailed pin assignments are described in Chapter 6.

Monitor

The EPC-7 contains no built-in connection for a monitor. Typically the EPC-7 contains an EXM-13A video controller for connection to an analog VGA monitor. Use of the EXM-13A is summarized below. Consult the EXM-13A reference manual for further details.

Monitors that can be used with the EXM-13A are VGA-compatible monitors (i.e., those compatible with the IBM PS/2 and with PC VGA add-in cards) and multiscan (multifrequency or "multisync") monitors. Refer to the EXM-13A manual for more information. If you cannot mate your monitor to the 15-pin connector on the EXM because you have a cable with a 9-pin connector, either (1) you have a TTL monitor that is not compatible with VGA or (2) you have a multisync monitor (which are usually shipped with 9- and 15-pin cables or adapters) and are using the wrong cable. If using a multiscan monitor, make sure to set the monitor's switch to analog (not TTL).

Keyboard

The front panel contains a keyboard connector compatible with that of the IBM PS/2. An adapter cable is provided so that keyboards with the larger five-pin PC/AT connectors can be used.

If the BIOS produces the message "KEYBOARD ERROR OR NO KEYBOARD PRESENT" at time of power-on or reset, either no keyboard is present, the keyboard cable is not firmly connected, a key was pressed, or the keyboard is not a PC/AT compatible keyboard.

If you wish to operate your system without a keyboard, you must start with a keyboard and invoke the BIOS setup screen to change the *Configuration Errors* field to "ignore keyboard errors."

Serial Port

The front panel contains one DB-9 serial-port connector. It is identical to the serial port labeled COM1 in the PC/AT and compatibles. It may be used for connecting a mouse, modem, serial printer, RS-232 link, etc.

If your EPC-7 contains a conductive plastic ESD shield on the connector, remove it only when connecting a device. Leaving it on the connector when the connector is not being used will reduce the possibility of ESD (electrostatic discharge) damage through the connector.

Parallel Printer Port

The parallel port on the front panel is compatible with the corresponding DB-25 LPT1 connector on IBM PCs and compatibles. Typically it is used to connect printers and software security keys.

SCSI Port

The SCSI connector is a high-density, 50-pin, standard SCSI-2 connector. The connector type is "shielded alternative 1" in the SCSI-2 specification. This connector is an AMP 174726-4 (or equivalent) socket. This SCSI implementation uses the Adaptec AIC 6360 chip and is therefore compatible with the Adaptec AHA 1520/1522 PC add-in card.

Drivers are available for a range of operating systems and SCSI devices, including disks, streaming tapes, CD-ROMs, and digital audio tapes. These drivers do not ship with the product; contact RadiSys for more information.

External Clock Input

The EPC-7 provides the option, when it is configured as the slot-0 controller, of deriving the ECL CLK10 signal from an internal oscillator or from a 10 MHz external clock source. An SMB connector is provided on the front panel. The external clock input is TTL compatible. It is not resistively terminated. It presents one FAST TTL unit load (I_{IH} < 0.02mA, I_{IL} < -0.6 mA). The external clock signal must have TTL levels. The choice of clock source is specified in the clock control register, 8162. Refer to Chapter 7, *VXIbus Interface*, for more information.

External Clock Output

A second SMB connector provides a TTL form of the CLK10 clock. It can drive a 50 ohm line. This is typically used to synchronize multiple VXI mainframes.

External Trigger

A third SMB connector provides for an external TTL trigger signal input or output. When configured as an input, it is not resistively terminated and presents one FAST TTL unit load (I_{IH} < 0.02mA, I_{IL} < -0.6 mA). When configured as an output, it can drive a 50 ohm line. The direction of the signal and the association to a specific backplane trigger line is controlled by the external trigger register, 8163. Refer to Chapter 7, *VXIbus Interface*, for more information.

4. Configuring the BIOS Setup

Power-On Screen Display

Whenever a hardware reset (power-on or front-panel) occurs on the EPC-7, information is displayed on the attached monitor showing the status of the BIOS selftest and the amount of memory found. If everything proceeds normally, the screen image should appear approximately as shown in the following figure.


```
486 Modular BIOS version 3.05abd,
Copyright (c) 1984-90 Award Software Inc.
Copyright 1991 RadiSys Corporation    BIOS V3.05

TESTING INTERRUPT CONTROLLER #1.....................................OK
TESTING INTERRUPT CONTROLLER #2.....................................OK
TESTING CMOS BATTERY................................................OK
TESTING CMOS CHECKSUM...............................................OK
TESTING VME INTERFACE...............................................OK
TESTING VXI INTERFACE...............................................OK
SIZING SYSTEM MEMORY.....................................640K   FOUND
TESTING SYSTEM MEMORY....................................640K   OK
CHECKING UNEXPECTED INTERRUPTS AND STUCK NMI........................OK
TESTING PROTECTED MODE..............................................OK
SIZING EXPANSION MEMORY.................................7168K  FOUND
TESTING MEMORY IN PROTECTED MODE........................7808K  FOUND
TESTING PROCESSOR EXCEPTION INTERRUPTS..............................OK
TESTING SERIAL PORT #1..............................................OK
TESTING SERIAL PORT #2..............................................OK
TESTING PARALLEL PORT...............................................OK
```

Figure 6. Power-on Screen Display.

Some error messages might occur during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS will display the error on the appropriate line of the screen display and attempt to continue.

BIOS Setup Screen

The EPC-7's BIOS contains a setup function to display and alter the system configuration. This information is maintained in the EPC-7's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-7 hardware.

To invoke the setup function in a "booted" system, press the CTRL+ALT+ESC keys simultaneously. This may be done during system operation in most, but not all circumstances. Some programs that take control of the keyboard at a low level, such as Microsoft Windows, cause this key sequence to be interpreted differently, or not at all. It should always work, however, when the DOS operating system prompt is shown on the screen. The setup function can be invoked prior to system booting by pressing CTRL+ALT+ESC immediately after the initial selftest screen is cleared.

The main setup screen will be similar to the following.

```
RadiSys EPC-7 CMOS Setup, System BIOS V3.05
50MHz 486, 16 MBytes memory


Date (mm/dd/yy) ..............  ... 12/02/93
Time (hh:mm:ss) ..............  ... 07:34:56
Configuration Errors .........  ... Halt on all errors

Diskette Drive A .............  ... 1.4M  3.5 inch
Fixed Disk Drive C  ..........  AT
Fixed Disk Drive D  ..........  None

Bus Priority .................  ... Pri 3       F2  = EXM menu
Bus Release Method ...........  ... RONR        F3  = Fixed disk menu
Bus Arbitration ..............  ... Priority    F10 = Save CMOS and EXM data
COM1: ........................  ... Enabled     ESC = Exit without saving
COM2: ........................  ... Disabled
LPT1: ........................  ... Enabled
```

Figure 7. Main Setup Screen.

Use the up and down cursor (arrow) keys to move from field to field. For most fields, position the cursor at the field and press the left and right cursor (arrow) keys to rotate through the available choices. Once the screen has been changed to appear as desired, press the F10 function key to save the changes in nonvolatile (battery-backed) CMOS RAM and then press the F5 function key to confirm the changes and reboot. Alternately, press the ESC key to ignore any changes and exit.

The fields are explained below.

DATE and TIME

These values are changed by moving to this field and typing in the format shown.

CONFIGURATION ERRORS

This field gives you several choices about the situations under which the BIOS should wait for user input if a configuration error is found. The selections are

1) halt on all errors,
2) ignore all errors,
3) ignore keyboard errors (allows operation without a keyboard),
4) ignore disk errors, and
5) ignore keyboard and disk errors.

DISKETTE DRIVE

This field identifies the type of floppy disk drive installed as the A drive. If the EPC-7 has a floppy drive installed, the proper setting is for a 3.5" 1.44 MB floppy disk drive. If no drive is installed, the proper setting is NONE.

FIXED DISK DRIVE

This display-only field shows the type of disk selected from the fixed disk menu. To see the detailed characteristics of the device or to change the device, use the F3 function key to go to the fixed disk menu.

BUS PRIORITY

This field allows selection among the four VXIbus priority levels. This is the level at which the EPC-7 will contend for the bus when it performs a VXIbus access.

BUS RELEASE METHOD

This field entry toggles between two bus release modes: ROR (release on request) and RONR (request on no request, also known as the VXI fair-requester mode). ROR results in slightly better EPC-7 performance when accessing the VXIbus; RONR directs the EPC-7 to not "park" on the bus and thus slightly improves the access time of other VXIbus masters to the bus. When using RONR, all masters on the VXIbus should be set to RONR to avoid a starvation condition where one master never gains access to the bus.

BUS ARBITRATION

This field toggles between the two arbitration algorithms provided by the EPC-7: priority arbitration and round-robin arbitration. This field is only used when the EPC-7 is configured as the slot-0 controller:

COM1, COM2, LPT1

These fields toggle between the enabled and disabled states. The enabled state enables the controllers for these I/O ports. The disabled state means that the associated I/O port is disabled, and the I/O addresses and IRQs associated with the controller for the port are not responded to by the controller. Putting a port in the disabled state allows use of I/O modules that may have conflicting addresses or IRQs with the built-in ports.

EXM Configuration

A separate EXM setup screen is used to configure the EXM modules in the system. It is displayed by pressing the F2 function key from the main setup screen. The EPC-7's nonvolatile (battery-backed) CMOS holds identification and configuration information for up to six EXM module slots. Note that six EXM slots are indicated even in systems that do not have six EXM slots available. An EPC-7MC module carrier can be added to a standard EPC-7 to provide two additional EXM slots. This is a factory-installed option only.

The BIOS displays the configuration information in hexadecimal format.

```
 RadiSys EPC-7 EXM Setup, System BIOS V3.05
50MHz 486, 16 MBytes memory

              ID   OB1   OB2
 Slot     0   FF    00    00
          1   FF    00    00              F10  = Okay
          2   FF    00    00              ESC  = Cancel
          3   FF    00    00
          4   FF    00    00
          5   FF    00    00
```

Figure 8. EXM Setup Menu.

EXMs must be defined in this screen so the BIOS can correctly identify and initialize each one at boot-up. Each EXM must be listed by slot number, ID and two option bytes as defined below.

SLOT indicates the EXM slot in which the EXM is installed. See the figure below to determine which slot each EXM occupies. Note that, when installed, the floppy disk drive occupies EXM slot 0. Dotted lines indicate EXM slot numbers for an optional EPC-7MC module carrier.

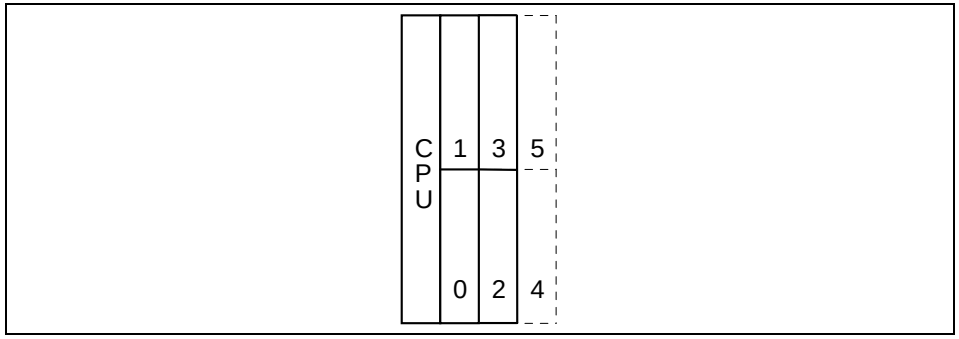


Figure 9. EXM Slot Numbering.

ID is a hard-wired ID value. Each type of EXM has a unique ID value.

OB1/OB2 are two "option" bytes of configuration information.

All slots **not** occupied by an EXM module should show an ID of FF and OB1/OB2 of 00 00 indicating that no EXM is present. This includes slot 0 if the floppy drive is installed.

Consult the EXM manual for the correct configuration information for each EXM expansion module installed.

After all EXMs have been configured, press F10 to save the data or ESC to ignore the changes. In either case you will be returned to the main setup screen.

When using EXMs with configurable interrupts, DMA channels, I/O addresses, and/or memory addresses, avoid conflicts with built-in functions of the EPC-7. Guidelines are:

1. If an interrupt is needed, use IRQ3, IRQ5, IRQ9, IRQ12, or IRQ15. IRQ7 can be used if the printer port is not being used. IRQ3 should not be used if the COM2 port is being used. COM2 is available on the EPC-7AM adapter module. (Refer to Appendix C for installation information concerning the EPC7-AM.)
2. Use DMA channels 1, 3, 6, and 7. Channels 0 and 5 may also be used, depending on whether you are using the SCSI interface and how it is configured.
3. Do not select I/O addresses that conflict with those in the EPC-7. A complete list appears in Appendix B. For instance, I/O addresses in the 300-33F range can be used.
4. If the EXM needs to use upper memory addresses, they must be in the 0D0000-0DFFFF range.

Fixed Disk Menu

The Fixed Disk Menu is used to define the type of hard disk(s) installed in the system. Enter the Fixed Disk Menu screen by pressing the F3 function key from the main setup screen.

The Fixed Disk Menu screen looks similar to the one below.

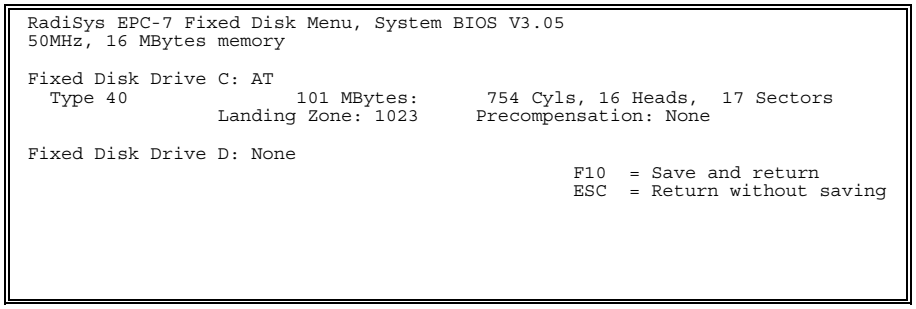


Figure 10. Fixed Disk Menu.

AT Disk type AT denotes the many types of non-SCSI PC/AT compatible drives including IDE. Scroll through the numeric drive types listed to find the one matching the characteristics of the hard drive as shown on the drive sticker located on the right side panel of the EPC-7. If no pre-defined drive type matches the installed drive, use the user-definable drive types 48 or 49.

None Choose None if there is no hard disk present.

SCSI Choose SCSI to activate the built-in SCSI BIOS. Use this option only if you are not using a loadable device driver (such as those included with the EZ-SCSI software). There are no fixed disk characteristics to select because the BIOS determines them dynamically. If Drive C is set to SCSI, Drive D must also be set to SCSI even if no second drive is installed. If this is not done, the system will prompt you to correct the problem before exiting this screen.

EXM Flash Choosing disk type EXM Flash tells the BIOS to use a flash memory device (e.g., EXM-2A) as a drive. An EXM-2A can be made the boot device by making EXM Flash the drive C type. However, if Drive C is EXM Flash, Drive D **must** be set to None.

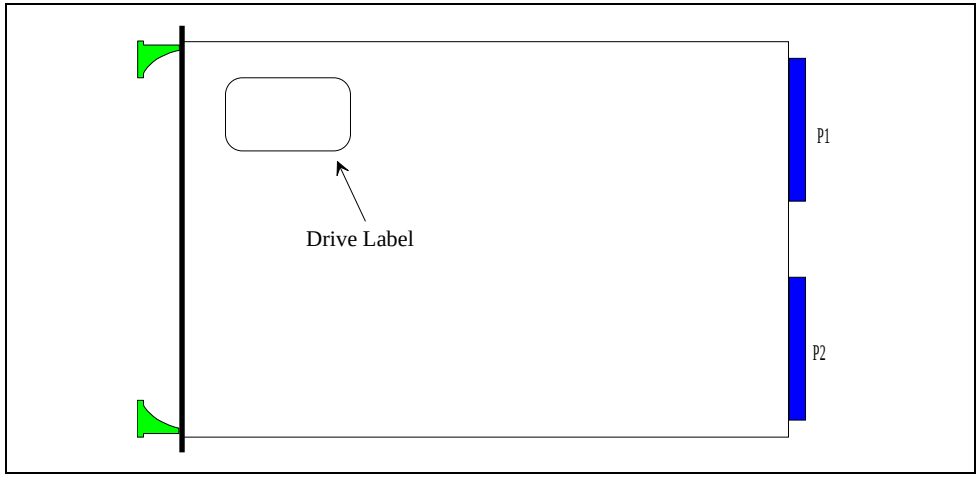


Figure 11. Location of Disk Drive Label.

User-Definable Drive Types

If the correct **AT** disk type is not listed, the EPC-7 provides user-editable drive types 48 and 49. Select either of these drive types. Use the TAB key (→|)or the left and right cursor keys (← →) to move to the next (or previous) field. Note that the default settings for MBytes, Cylinders, Heads, and Sectors is 1. MBytes is a display-only field calculated by the BIOS. Move the cursor to each field (Cyls, Heads, and Sectors) and type the value for that field.

If a drive label exists on the right side panel (refer to Figure 11), use the parameters listed on the label.

When installing a user-supplied replacement IDE hard disk, consult the hard disk manual for the correct values to use for cylinders, heads and sectors. The BIOS allows use of the following maximum values:

Cylinders 1023 Heads 63 Sectors 16

The new hard disk may have parameters larger than the allowable maximum. If the drive parameters are greater than the allowable maximum, divide the actual number of cylinders by 2 and multiply the actual number of heads by 2. IDE drives use Universal translation mode. That is, each sector is addressed as an absolute sequential sector number. Since the embedded "intelligent" controller converts the sector data to an absolute number, these "false" cylinder and head numbers will still allow the drive to be used. The example on the next page shows how this is done.

Example:

	Actual parameters	Conversion factor	Numbers to Use
Cylinders	1350	divide by 2	675
Heads	5	multiply by 2	10
Sectors	32	(none)	32
Total Sectors	216,000		216,000

Table 4. Fixed Disk Configuration Example.

After the Fixed disk(s) have been configured, press F10 to save the data or ESC to ignore the changes. In either case you will be returned to the main setup screen.

Disk Formatting

The hard disk in the EPC-7 is an IDE disk which is "hard sectored"; therefore it does not require low-level formatting. Depending on the context in which you ordered the EPC-7, the disk is either bootable (containing an operating system and other software pre-installed) or empty (neither partitioned nor formatted).

Low-level IDE (AT) Disk Formatting

Low-level formatting was originally performed on "soft-sectored" hard disks to establish logical sectors, map out bad sectors, create the master boot block, etc. Since IDE hard disks are "hard-sectored", they do not need low-level formatting. However, the original purpose of low-level formatting has evolved and it is now also used to wipe a disk clean of all data.

For low-level formatting of an IDE hard drive, a disk utility must be used, such as DOSUTILS from Ontrack Computer Systems, Inc., QAPlus from DiagSoft, Inc., AMIDIAG from American Megatrends Inc., or SuperSoft Service Diagnostics from SuperSoft Inc. Low-level formatting is rarely necessary and in fact, is not possible on some of the new higher capacity IDE drives.

5. Theory of Operation

This chapter specifies other information about the operation of the EPC-7 that might be useful to the system designer. The block diagram below shows the overall data-path structure of the EPC-7. Note that numbers in parentheses denote the data width of the path.

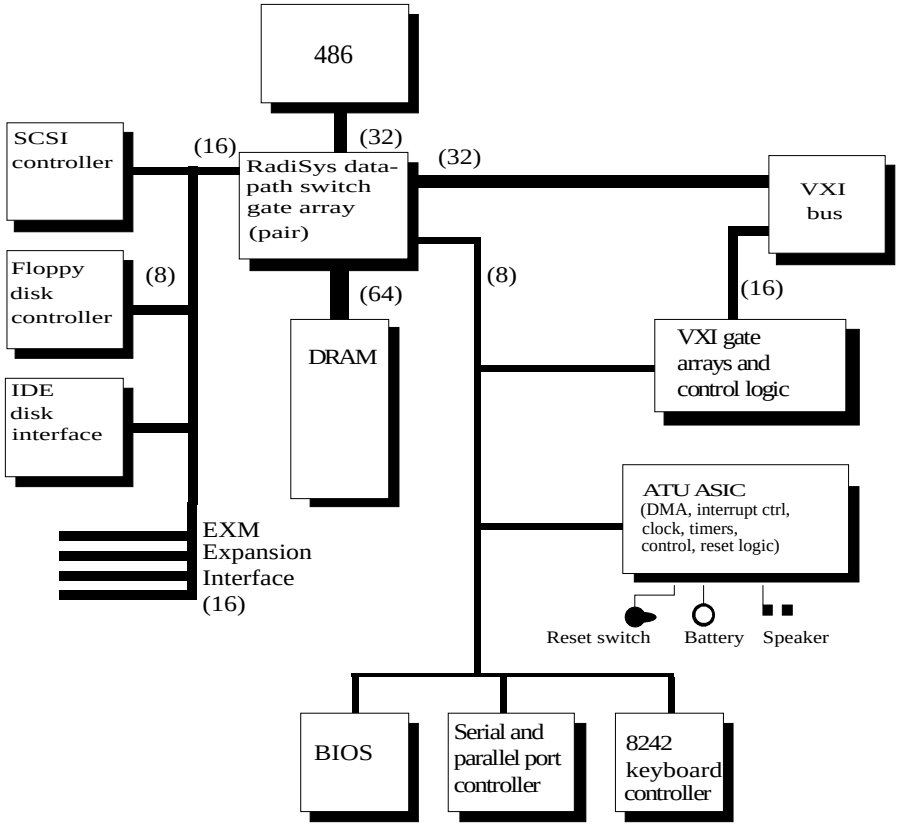


Figure 12. Data Path Block Diagram.

5 5

Memory Map

The 2^{32} byte physical address space seen by the CPU is mapped according to the following table.

Range	Content
00000000 0009FFFF	DRAM
000A0000 000BFFFF	Uncommitted, mapped to EXM expansion interface (typically, with a VGA video controller EXM installed, 0A0000-0BFFFF will be the video RAM and 0C0000-0C7FFF will be the video BIOS)
000C0000 000CFFFF	DRAM (see bit MDCF in memory mode register)
000D0000 000DFFFF	Uncommitted, mapped to EXM expansion interface
000E0000 000EFFFF	Mappable window onto VXI data transfer bus or uncommitted, mapped to EXM expansion interface, controlled by bit in register 8102h
000F0000 000FFFFF	DRAM (used for BIOS shadowing) Write-protected.
00100000 00FDFFFF	DRAM or EXM expansion interface (to DRAM to the extent of the value of MEMS in the memory mode register)
00FE0000 00FFFFFF	Mapped to BIOS ROM or DRAM (see bit MDFF in memory mode register)
01000000 03FFFFFF	DRAM or EXM expansion interface (see bit MEMS in the memory mode register)
04000000 0FFFFFFF	Mapped to EXM expansion interface
10000000 EFFFFFFF	Mapped to VXIbus
F0000000 FFFFFFFF	Mapped to EXM expansion interface. On the EXM expansion interface, ranges xxFExxxx and xxFFxxxx are ROM.

Table 5. Physical Address Space Mapping.

Little-endian and big-endian byte ordering is discussed in Chapter 7, *VXIbus Interface*.

Processor and Memory

The processor is a derivative of the Intel 80486 DX. The EPC-7 was designed to work with a variety of models and frequencies of 486s; the ordering information will identify the exact 486 used. The EPC-7 is shipped as either a 33 MHz 486DX, a 50 MHz 486 DX or a 100 MHz 486 DX4. The 33 Mhz and 50 MHz EPC-7s contain an integrated floating-point coprocessor and 8 KB cache; the 100 MHz EPC-7 contains an integrated floating-point coprocessor and a 16 KB cache.

The processor board contains four 72-pin SIMM sockets. The factory-installed DRAM options are 2, 4, 8, 16, 32, or 64 MB. The DRAM has byte-wide parity. The 50 MHz EPC-7 does not support 4 MBytes of DRAM. The 33 MHz EPC-7 does not support 64 MBytes of DRAM. 100 MHz EPC-7s come with either 8, 16, 32, or 64 MB of DRAM.

Cached and Uncached Addresses

The 486 in the EPC-7 contains a cache. The cache is designed to cache selectively by address range, because many memory areas defined by the PC architecture, as well as memory mapped to the VXIbus and potentially some mapped to the EXM expansion interface, cannot be safely cached. What *is* cached is the first 640 KB of memory and all DRAM above 1 MB, meaning the following address ranges:

0000 0000 to 0009 FFFF
0010 0000 to 03FF FFFF

The use of a cache with dual-port memory (i.e., DRAM in the EPC-7 that is also accessible by other VXIbus masters) raises the issue of "stale data." This is prevented by the "bus watching" logic of the cache controller. Any write into the EPC-7's DRAM from another VXI master will cause the data at these addresses, if it happens to be in the cache, to be invalidated in the cache, meaning that a subsequent read of the data from the 486 will fetch the updated value from DRAM.

ROM and ROM Shadowing

EPC-7 contains a 27010 1 MB EPROM. The EPROM is mapped into the top of the processor's 32-bit address space, and also just below the 16 MB boundary for PC/AT compatibility. The EPROM contains the PC BIOS, selftest program, and the CMOS setup.

For best possible performance, the BIOS initialization software copies 64 KB of the ROM contents into DRAM (called shadowing) at addresses 000Fxxxx. If the BIOS discovers a video controller present containing a video BIOS, the BIOS copies the video BIOS into DRAM at addresses 000C0000-00C7FFF. If the SCSI controller is enabled, the BIOS copies the SCSI BIOS into addresses 000C8000-000CFFFF. The BIOS write-protects these areas of memory, even if not being used for BIOS shadowing.

The BIOS also uses a control bit (MDFF in the memory mode register) to remove the EPROM from just below the 16 MB boundary after initialization to ensure a contiguous DRAM space for EPC-7s with 16 MB or more of memory.

SCSI Controller

The SCSI controller is based on the Adaptec AIC-6360 I/O processor, which is supported by a large base of software drivers. The drivers support a range of operating systems and SCSI devices, including disks, streaming tapes, CD ROMs, and digital audio tapes. SCSI software does not ship with the EPC-7, but a separate SCSI software and manual package is available at not charge. Contact RadiSys Technical Support for ordering information. If you need to use SCSI software with a non-DOS/Windows operating system, contact Adaptec sales at 1-800-442-7274.

The controller is compatible with SCSI-2 and CCS (common command set). It supplies a transfer rate of up to 5 MB/s for synchronous transfers from the buffer on the SCSI bus, or up to 3 MB/sec sustained rate. The controller's registers are mapped to I/O space addresses 340-35E.

The EPC-7 contains no internal SCSI devices; the controller connects only to a front-panel connector for an external SCSI bus. SCSI TERMPWR is provided by a solid-state switch having current limiting and thermal shutdown.

Floppy Disk Controller

The floppy disk controller is a standard PC compatible controller, connecting to one of two floppy disk connectors: a 34-pin or a 26-pin floppy conector. This is a build-time options. The header and cable supply power to the floppy drive, as well as carry the drive signals. This cannot be disabled.

IDE Disk Interface

EPC-7 contains an interface for an internal IDE disk drive. The signals for the drive are supplied on the 40-pin header labeled P9, and power for the drive is supplied on the 4-pin header labeled P13. This cannot be disabled.

Battery

WARNING

Removing the battery will invalidate the CMOS setup. Before removing, record your current values for all screens.

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a shelf life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is significantly lower than 60°C, the battery is estimated to have a life of 10 years.

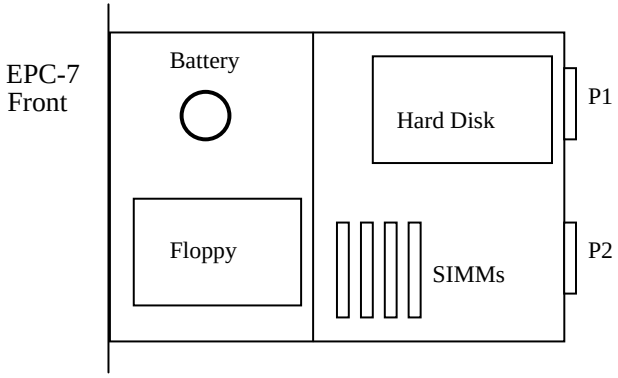


Figure 13. EPC-7 Battery Location.

The battery holder is for a 23 mm coin cell, such as a Panasonic BR2330 or Rayovac BR2335.

To remove or replace the battery, follow the instructions below.

5 5

✉ **MAKE SURE THAT THE PROCESS DESCRIBED HERE IS PERFORMED IN A STATIC-FREE ENVIRONMENT.**

First remove the upper two EXM modules, if present. Remove the side panel from the EPC-7 and locate the battery. The battery cell is held in place by a spring lever. To remove the battery, apply downward pressure to the cell in the vicinity of the base of the spring (a small screwdriver may be used), while at the same time applying lateral pressure to the cell in the direction away from the spring base.

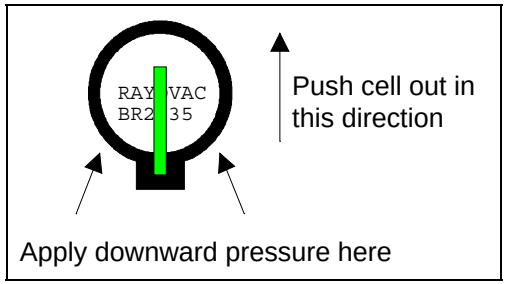


Figure 14. Battery Removal.

A new cell is installed by sliding it beneath the spring until it snaps into the holder. Ensure that the spring has not been damaged and that it is in firm contact with, and applying downward pressure on, the battery cell.

Watchdog Timer

The EPC-7 contains a continually running timer having a period of either about 0.2 or 6.7 seconds (software selectable). This event may be enabled as a source of the IRQ10 interrupt, or as a hardware reset, depending on the outcome of a comparison of registers 8154 and 8155. The watchdog timer event is generated whenever the period expires if the watchdog timer bit is set in 815Dh and the watchdog timer bit is set in the event enable register at 8155h. Otherwise this is masked off. The timer is reset to its maximum value by an I/O read of the module status/control register @ 815Dh.

EXM Expansion Interface

The EXM expansion interface, an I/O expansion bus, is provided at the rear of the front-panel slots in the EPC-7. The EXM expansion interface is very similar to the PC/AT I/O or ISA bus. In addition, it contains a signal -EXMID used for dynamic recognition and configuration of EXMs. EXMs respond to one or more I/O addresses in the range 100h - 105h only when their -EXMID signal is asserted. EXMs are required to return a unique EXM-type identification byte in response to a read from I/O address 100h. The EXM configuration register provides the means to assert the -EXMID signal.

Further information on the EXM expansion interface, its connectors, and standards for building EXMs is available upon request.

VXIbus Interface

The EPC-7 module connects to the VXIbus J1 and J2 connectors in the left of the two slots occupied by the EPC-7, and to the J1 connector in the right slot.

On the left P1 connector, the EPC-7 uses all of the defined VME/VXI lines except the following:

SERCLK
SERDAT
+5V STDBY

On the right P1 connector, the EPC-7 connects to +5VDC, +12VDC, ground, and BG0, BG1, BG2, BG3, and IACK.

On the P2 connector, the EPC-7 uses all of the defined VXIbus lines except the following:

SUMBUS
LBUSC00-LBUSC11
RSV1,RSV2,RSV3
+24V,-24V

5 5

Slot 0 and System Controller Functions

When the EPC-7 is configured as the slot 0 controller, it performs the VXI slot-0 functions and the VME system controller functions.

The slot-0 functions consist of generation of the CLK10 signals and MODID support. The system controller functions are the following:

- Serves as the bus arbiter (priority or round-robin)
- Drives the 16 MHz SYSCLK signal
- Starts the IACK daisy chain.
- Provides Bus Timer function

When configured as the system controller, the EPC-7 detects and terminates data transfer bus timeouts. Once it sees either the `DS0` or `DS1` lines asserted, a counter is started. If the counter expires before both `DS0` and `DS1` are deasserted, the EPC-7 asserts the VMEbus `BERR` signal until both data strobes are deasserted. The duration of the VMEbus timeout counter is 100-120 μsecs. When the EPC-7 is configured as the slot-0 controller, this timeout cannot be disabled and the duration cannot be changed.

Although the EPC-7 provides the required timeout function for data transfer time-out, it does not provide the optional bus grant timeout. If another master has been granted permission to use the data bus but does not access (or relinquish) the data bus, the bus will be "hung" indefinitely.

Reset Behavior

Setting bit RSTP in the status/control register puts the EPC-7 in the soft reset state. The EPC-7 continues to execute instructions in this state, and an interrupt (VXR) can be enabled to detect entry into this state.

(For more information about the registers and their bits that are discussed in this section, refer to Chapter 7, *VXIbus Interface*.)

The soft reset state inhibits any VXI data-transfer operations and prevents the assertion of the VXI interrupt and trigger lines. It does so by clearing the following registers:

- Bits 0-2 of the interrupt generator register
- TTL trigger drive register
- External trigger register
- VME A31-24 address register
- VME A21-16 address register
- VME modifier register
- PASS and RDY bits in the status/control register

In addition, the VXR bit is set, the EVME bit is masked off, and the SBER bit is masked on.

Assertion of the VXI SYSRESET signal when bit SRIE in the status/control register is zero also places the EPC-7 in the soft reset state, except the PASS and RDY bits are not cleared in this case.

Four conditions cause a full hardware reset of the EPC-7:

- SYSRESET signal (when enabled in the status/control register)
- Front-panel reset switch
- Expiration of the watchdog timer when bit WDTR in the module status/control register is set
- Power on

Printed Circuit Board

The following diagram shows areas of interest on the EPC-7 circuit board.

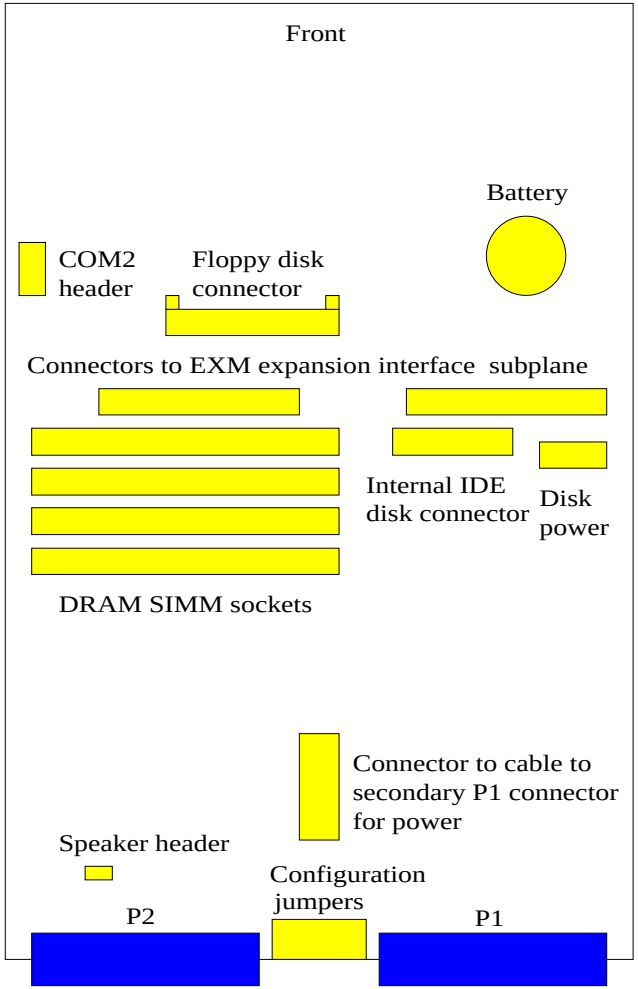


Figure 15. PCB Layout.

6. Connectors

This chapter specifies the details of the connectors of the EPC-7.

The DB-9 COM1 serial port connector is defined in the following table.

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal ground		

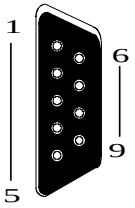
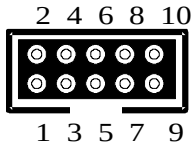


Table 6. DB-9 Pin-out.

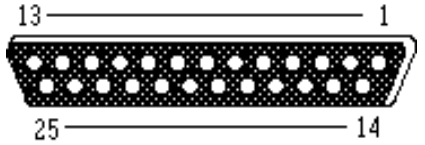


A second serial port, addressable as PC serial port COM2, exists in the form of a 10-pin header on the printed-circuit board near the bottom of the front panel. Pin 1 is the pin closest to the front panel and the bottom of the EPC-7 printed circuit board. The header is defined in the table below.

Pin	Signal	Pin	Signal
1	Carrier detect	6	Clear to send
2	Data set ready	7	Data terminal ready
3	Receive data	8	Ring indicator
4	Request to send	9	Signal ground
5	Transmit data	10	Unconnected

Table 7. COM2 10-Pin Header Pin-out.

The female DB-25 LPT1 printer and parallel port on the front panel is defined in the following table.



Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper end	25	Signal ground
13	Select		

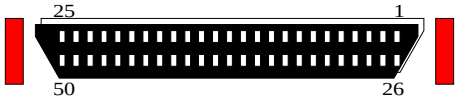
Table 8. DB-25 LPT1 Pin-out.

The keyboard connector is an IBM PS/2 style connector. It is not compatible with the older larger 5-pin keyboard connectors, but an adapter cable is provided. The connector pins are defined in the table below.

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	unconnected	5	Clock
3	Ground	6	unconnected

Table 9. Keyboard Connector Pin-out.

The SCSI connector is a high-density, 50-pin, standard SCSI-2 connector of type AMP 174726-4 or equivalent. The mating connector is AMP part number 750342-5. The connector type is "shielded alternative 1" in the SCSI-2 specification. The connector pins are defined in the following table.



Pin	Signal	Pin	Signal
1	Ground	26	-DB(0)
2	Ground	27	-DB(1)
3	Ground	28	-DB(2)
4	Ground	29	-DB(3)
5	Ground	30	-DB(4)
6	Ground	31	-DB(5)
7	Ground	32	-DB(6)
8	Ground	33	-DB(7)
9	Ground	34	-DB(P)
10	Ground	35	Ground
11	Ground	36	Ground
12	Ground	37	Ground
13	unconnected	38	TERMPWR
14	Ground	39	Ground
15	Ground	40	Ground
16	Ground	41	-ATN
17	Ground	42	Ground
18	Ground	43	-BSY
19	Ground	44	-ACK
20	Ground	45	-RST
21	Ground	46	-MSG
22	Ground	47	-SEL
23	Ground	48	-C/D
24	Ground	49	-REQ
25	Ground	50	-I/O

Table 10. SCSI Port Pin-out.

The speaker header on the EPC-7 circuit board is defined in the table below.

Pin	Signal	Pin	Signal
1	Reference voltage	2	Speaker tone

Table 11. Speaker Header Pin-out.

The front-panel CLK-IN connector is a miniature SMB coax connector. The input signal must be a TTL signal capable of driving a 74F04 input (interface circuit must source a Vol=0.5V max @ 1mA sink and must source a Voh=2.4V min @ 500uA source current

The front-panel CLK-OUT connector is a miniature SMB coax connector. It is a TTL output signal. CLK-OUT can drive a 50 ohm line to 2.25V.

The front-panel TRIG connector is a miniature SMB coax connector. Whether it is an input or output is determined by the external trigger register (refer to Chapter 7, *VXIbus Interface*). The input signal must be a TTL signal capable of driving a 74F04 input (see CLK-IN). As an output, TRIG can drive a 50 ohm line to 2.25V.

VXI Signal Usage

The following table shows the usage of the VXI expansion interface signals on the "main" P1 connector (the leftmost of the two P1 connectors). The "use" column defines how the signal is used. I denotes input, O denotes output, IO denotes input/output, P denotes power, G denotes ground, and blank denotes unused and unconnected. Superscripted numbers represent notes.

	Row A		Row B		Row C	
Pin	Name	Use	Name	Use	Name	Use
1	D00	IO	BBSY*	IO	D08	IO
2	D01	IO	BCLR*	IO [2]	D09	IO
3	D02	IO	ACFAIL*	I	D10	IO
4	D03	IO	BG0IN*	I	D11	IO
5	D04	IO	BG0OUT*	O	D12	IO
6	D05	IO	BG1IN*	I	D13	IO
7	D06	IO	BG1OUT*	O	D14	IO
8	D07	IO	BG2IN*	I	D15	IO
9	GND	G	BG2OUT*	O	GND	G
10	SYSCLK	IO [1]	BG3IN*	I	SYSFAIL*	IO
11	GND	G	BG3OUT*	O	BERR*	IO
12	DS1*	IO	BR0*	IO [3]	SYSRESET*	IO
13	DS0*	IO	BR1*	IO [3]	LWORD*	IO
14	WRITE*	IO	BR2*	IO [3]	AM5	IO
15	GND	G	BR3*	IO [3]	A23	IO
16	DTACK*	IO	AM0	IO	A22	IO
17	GND	G	AM1	IO	A21	IO
18	AS*	IO	AM2	IO	A20	IO
19	GND	G	AM3	IO	A19	IO
20	IACK*	IO	GND	G	A18	IO
21	IACKIN*	I	SERCLK		A17	IO
22	IACKOUT*	O	SERDAT*		A16	IO
23	AM4	IO	GND	G	A15	IO
24	A07	IO	IRQ7*	IO	A14	IO
25	A06	IO	IRQ6*	IO	A13	IO
26	A05	IO	IRQ5*	IO	A12	IO
27	A04	IO	IRQ4*	IO	A11	IO
28	A03	IO	IRQ3*	IO	A10	IO
29	A02	IO	IRQ2*	IO	A09	IO
30	A01	IO	IRQ1*	IO	A08	IO
31	-12V	P	+5VSTDBY		+12V	P
32	+5V	P	+5V	P	+5V	P

Table 12. VXIbus Signal Usage.

Notes to preceding table:

1 SYSCLK as an input is used only in conjunction with the SYSC bit in the status/control register. SYSCLK is an output only if the EPC-7 is configured as the system controller.

2 An output only if the EPC-7 is configured as the system controller.

3 An input only if the EPC-7 is configured as the system controller, or if the bus release mode is set to RONR.

The following table shows the usage of signals on the VXIbus P2 connector.

	Row A		Row B		Row C	
Pin	Name	Use	Name	Use	Name	Use
1	ECLTRG0	IO	+5V	P	CLK10+	IO
2	-2V	P	GND	G	CLK10-	IO
3	ECLTRG1	IO	RSV1		GND	G
4	GND	G	A24	IO	-5.2V	P
5	MODID12	IO	A25	IO	LBUSC00	
6	MODID11	IO	A26	IO	LBUSC01	
7	-5.2V	P	A27	IO	GND	G
8	MODID10	IO	A28	IO	LBUSC02	
9	MODID09	IO	A29	IO	LBUSC03	
10	GND	G	A30	IO	GND	G
11	MODID08	IO	A31	IO	LBUSC04	
12	MODID07	IO	GND	G	LBUSC05	
13	-5.2V	P	+5V	P	-2V	P
14	MODID06	IO	D16	IO	LBUSC06	
15	MODID05	IO	D17	IO	LBUSC07	
16	GND	G	D18	IO	GND	G
17	MODID04	IO	D19	IO	LBUSC08	
18	MODID03	IO	D20	IO	LBUSC09	
19	-5.2V	P	D21	IO	-5.2V	P
20	MODID02	IO	D22	IO	LBUSC10	
21	MODID01	IO	D23	IO	LBUSC11	
22	GND	G	GND	G	GND	G
23	TTLTRG0*	IO	D24	IO	TTLTRG1*	IO
24	TTLTRG2*	IO	D25	IO	TTLTRG3*	IO
25	+5V	P	D26	IO	GND	G
26	TTLTRG4*	IO	D27	IO	TTLTRG5*	IO
27	TTLTRG6*	IO	D28	IO	TTLTRG7*	IO
28	GND	G	D29	IO	GND	G
29	RSV2		D30	IO	RSV3	
30	MODID00	IO	D31	IO	GND	G
31	GND	G	GND	G	+24V	
32	SUMBUS		+5V	P	-24V	

Table 13. VXIbus P2 Connector.

The P1 connector below is the "rightmost" one used for power. The connector propagates the bus-grant and IACK daisy chains through the rightmost slot occupied by the EPC-7 so that installing backplane jumpers in this slot is unnecessary.

	Row A		Row B		Row C	
Pin	Name	Use	Name	Use	Name	Use
1	D00		BBSY*		D08	
2	D01		BCLR*		D09	
3	D02		ACFAIL*		D10	
4	D03		BG0IN*	I	D11	
5	D04		BG0OUT*	O	D12	
6	D05		BG1IN*	I	D13	
7	D06		BG1OUT*	O	D14	
8	D07		BG2IN*	I	D15	
9	GND	G	BG2OUT*	O	GND	
10	SYSCLK		BG3IN*	I	SYSFAIL*	
11	GND	G	BG3OUT*	O	BERR*	
12	DS1*		BR0*		SYSRESET*	
13	DS0*		BR1*		LWORD*	
14	WRITE*		BR2*		AM5	
15	GND	G	BR3*		A23	
16	DTACK*		AM0		A22	
17	GND	G	AM1		A21	
18	AS*		AM2		A20	
19	GND		AM3		A19	
20	IACK*		GND		A18	
21	IACKIN*	I	SERCLK		A17	
22	IACKOUT*	O	SERDAT*		A16	
23	AM4		GND		A15	
24	A07		IRQ7*		A14	
25	A06		IRQ6*		A13	
26	A05		IRQ5*		A12	
27	A04		IRQ4*		A11	
28	A03		IRQ3*		A10	
29	A02		IRQ2*		A09	
30	A01		IRQ1*		A08	
31	-12V		+5VSTDBY		+12V	P
32	+5V	P	+5V	P	+5V	P

Table 14. P1 Connector Pin-out.

Floppy Connector

The EPC-7 offers two floppy connectors: a 34-pin connector and a smaller 26-pin connector that is a subset of the 34-pin connector. This is a build-time option. The pinouts are as follows:

Pin	Signal	Pin	Signal
1	GND	2	GND
3	n/c	4	n/c
5	n/c	6	n/c
7	Fused VCC *	8	~INDEX
9	Fused VCC *	10	~DS0
11	Fused VCC *	12	~DS1
13	GND	14	GND
15	GND	16	~MO
17	GND	18	~DIR
19	GND	20	~STEP
21	GND	22	~WDATA
23	GND	24	~WGATE
25	GND	26	~TRK00
27	GND	28	~WRPRT
29	GND	30	~RDATA
31	GND	32	~SIDE
33	GND	34	~DSKCH

Pin	Signal	Pin	Signal
1	Fused VCC *	2	~INDEX
3	Fused VCC *	4	~DS0
5	Fused VCC *	6	~DSKCH
7	n/c	8	n/c
9	n/c	10	~MO
11	n/c	12	~DIR
13	n/c	14	~STEP
15	GND	16	~WDATA
17	GND	18	~WGATE
19	GND	20	~TRK00
21	GND	22	~WRPRT
23	GND	24	~RDATA
25	GND	26	~SIDE

Table 15. 34-pin and 26-pin Floppy Connector Pin-outs.

* Note: Pins 7, 9, and 11 on the 34-pin connector or pins 1, 3 and 5 on the 26-pin connector are not connected unless the fuse is installed. The EPC ships with the fuse installed and the fuse is not user-replaceable.

7. VXIbus Interface

This chapter describes the EPC-7 VXIbus interface as seen by a program. Wherever possible, users should avoid direct use of most of these facilities. The VXIbus interface should be accessed through RadiSys' EPConnect software, an easy-to-use, high-level interface that frees you from most machine-dependent considerations.

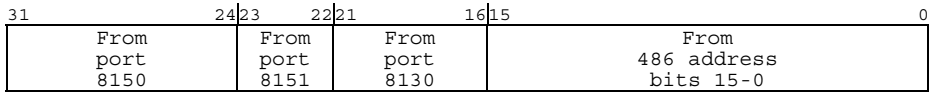
Concepts

Memory Map

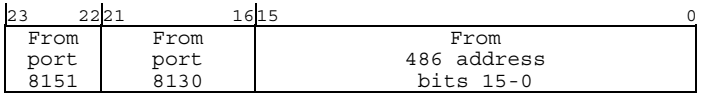
VMEbus accesses are available either by mapping a 64K segment of the VMEbus through the 0E0000-0EFFFF "E page" window or by direct mapping above 256 MB.

The following summarizes the source of the VMEbus address lines for accesses through the E page.

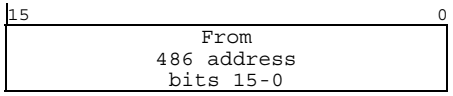
A32



A24



A16



It should be noted that the EPC-7 drives all 32 address lines even when performing an A24 or A16 access. Therefore, all the above registers (8150, 8151, 8130) should be

set for every access using the E-page window. Make sure that those registers not directly supplying address lines are set to "FF" values in the appropriate bit positions.

Direct VMEbus Accesses

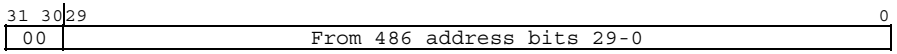
An alternate way to perform VMEbus accesses, providing that the EPC-7 is running in protected mode is to perform reads and writes at 486 addresses above 10000000h (256 MB). For instance, a 4-byte read at address 40000000h will result in a 4-byte VMEbus read access at address 00000000 with an address modifier specifying A32, supervisory data and no byte-swapping (little-endian mode).

With the EPC-7, addresses above 256 MB, with one exception for PC compatibility, map onto the VMEbus. When direct "protected-mode" addressing of A24 or A16 space, the high-order nibble is used to define the access mode and byte ordering. For A32 space, the high-order 2 bits define the access mode leaving 30 bits available for addressing. Thus, only the first 1 Gigabyte of VMEbus A32 space is directly addressable. All A24 and A16 space is directly addressable. The chart following shows how this direct mapping is used.

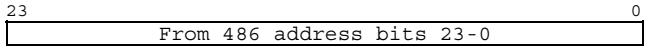
Address Range	Access Mode	Byte Order
1xxx0000 - 1xxxFFFF	VME A16 supervisory data	little endian
2x000000 - 3xFFFFFF	VME A24 supervisory data	little endian
40000000 - 7FFFFFFF	VME A32 supervisory data (mapped to VME 00000000-3FFFFFFF)	little endian
80000000 - BFFFFFFF	VME A32 supervisory data (mapped to VME 00000000-3FFFFFFF)	big endian
Cxxx0000 - DxxxFFFF	VME A16 supervisory data	big endian
Ex000000 - ExFFFFFF	VME A24 supervisory data	big endian
F0000000 - FFFEFFFF	Mapped to EXM expansion interface	
FFFF0000 - FFFFFFFF	486 upper ROM area	

When accessing the VMEbus in this manner, the source of the VMEbus address lines is defined below.

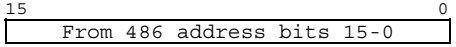
A32



A24



A16



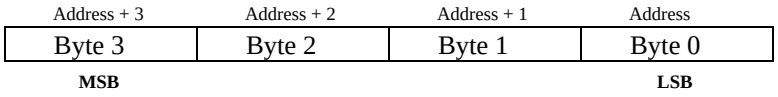
The main purpose of the direct VMEbus access mechanism, as opposed to the E-page mechanism, is for multitasking 32-bit operating-system environments, where multiple tasks need to make VMEbus accesses. Without this, the tasks would have to coordinate their use of the E-page mapping registers.

When using the EPC-7 this way to perform VMEbus accesses, one would typically set up the E-page window for interrupt acknowledge accesses. Also note that the direct access mappings do not cover the entire VMEbus A32 address range and do not provide all VMEbus-defined address modifier encodings, but one can use the E-page mechanism if needed to provide these.

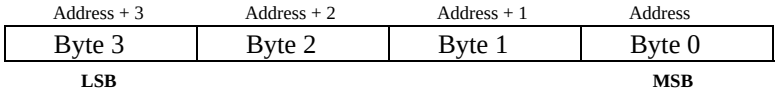
Byte Ordering

There are two fundamentally different ways of storing numerical values in byte locations in memory:

- Little endian, characteristic of Intel microprocessors, where the **least**-significant data byte (LSB) is stored in the lowest byte address



- Big endian, characteristic of Motorola microprocessors and the VMEbus environment in general, where the **most**-significant data byte (MSB) is stored in the lowest byte address



The EPC-7 contains programmable byte-swapping hardware to allow programs to read or write VMEbus memory in either byte order. When using the E-page to access the VMEbus, the order is selected by bit 5 (BORD) in the VME modifier register (8151). When using direct memory mapping, the order is address-range dependent (e.g., E0000000-E0FFFFFF accesses the A24 space with big endian byte ordering, and 20000000-20FFFFFF accesses the A24 space with little endian byte ordering).

When performing a single byte (D08) access, the byte order makes no difference. However, word (D16) or double-word (D32) accesses may require byte-swapping.

When little-endian is selected, bytes pass straight through unchanged. Little endian should only be used when reading or writing data between two Intel processor systems. The results of using little-endian byte ordering to transfer a double-word integer between an Intel processor and a Motorola processor are shown below.

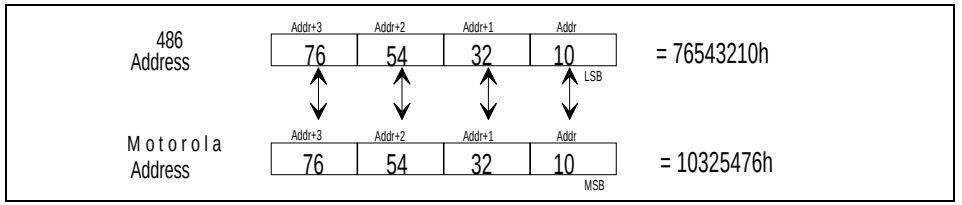


Figure 16. Little-Endian Byte Order.

Since the 486 processor uses Addr as the least-significant byte and the Motorola processor uses Addr as the most-significant byte, the processor receiving the data gets a "scrambled" value.

When big-endian is selected, the bytes are swapped between the 486 and VME. See the diagram below.

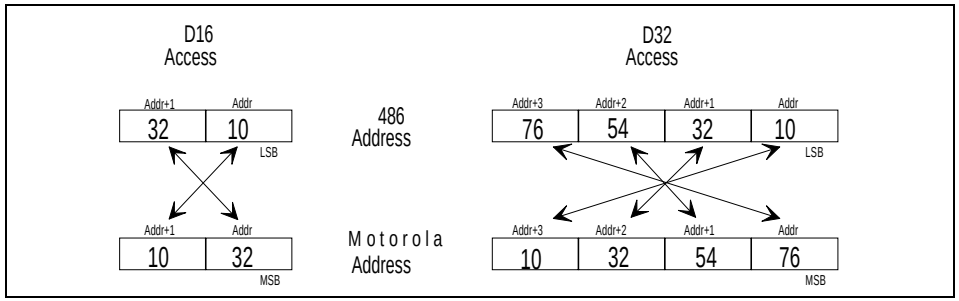


Figure 17. Big-Endian Byte-swapping.

When using big-endian byte ordering, care must be taken to assure that the VME address is aligned on a boundary; for D16 accesses the VME address must be on a word boundary (address evenly divisible by 2) and for D32 accesses the VME address must be on a double-word boundary (evenly divisible by 4). If this is not done, the results will be "scrambled" data. Although the VMEbus address must be boundary-aligned to match the data width (word or double-word), the 486 address does not need to be boundary-aligned.

Another consideration is the compiler being used. Some compilers produce two 16-bit accesses when a 32-bit access is desired. When this occurs, again the data will be "scrambled."

When transferring a 32-bit floating-point number, special care must be taken to assure that both processors use the same floating-point format; that both systems expect the mantissa and exponent in the same byte locations. As long as this is correct, transferring a floating-point number will work correctly. Since transferring a 64-bit floating-point number is not supported in hardware, two 32-bit transfers must be used with little-endian byte order and then byte-swapping must be accomplished in software.

Byte swapping applies only to EPC-7 initiated (master) **accesses; it does not apply to slave accesses** (from other VMEbus masters to the EPC-7's DRAM).

The EPConnect software provides a means of selecting the byte ordering during memory-copy operations.

Slave Accesses from the VMEbus

When SLE (Slave Enable) in the status/control register (8145) is set, the EPC-7's dual-ported memory will respond to accesses from other VMEbus masters.

All types of VME accesses (reads, writes, and read-modify-writes of all lengths) are supported, except for block transfer cycles. The EPC-7 responds to supervisory, non privileged, program, or data access modes.

The amount of memory that will be dual-ported is limited to the first (lowest address) 4 Mbytes in A24 space or all available memory in A32 space. In both cases, the slave memory's local (PC) address starts at Segment 0000, Offset 0000. This, of course, means that it is possible to overwrite the memory space occupied by the operating system. As such, care must be taken in writing to the EPC-7's memory.

When such an access is fielded by the EPC-7, the EPC-7's A24 or A32 base address is effectively subtracted from the VMEbus address value, and the result is treated as if the access came from the 486. However, note the following:

1. Any access that maps to local addresses 000A0000-000BFFFF, 000D0000-000EFFFF, to addresses mapped to the EPC-7's EXM expansion interface, and to addresses beyond the extent of the installed DRAM cause the EPC-7 to respond with BERR (bus error).
2. Write accesses to write-protected DRAM terminate normally (DTACK response), but with no effect on the DRAM.

Enabling the EPC-7 as a slave and specification of the address space (A24 or A32) and the base address is controlled by the EPConnect software. Use the Start-Up Resource Manager (SURM) or edit the **DEVICES** file.

Self Accesses Across the VMEbus

Since the EPC-7's DRAM can be mapped into the VMEbus A24 or A32 address space, the EPC-7 can access its DRAM in an alternate way - by generating VMEbus accesses to addresses mapped as the EPC-7's VME slave memory. This can be of use in multiple-processor systems where some of the EPC-7's DRAM is used as shared global memory; it means that the EPC-7 can access the global memory with the same addresses as used by other processors without needing to understand that the memory is actually on-board.

This ability is also useful in system checkout (i.e., checking operation of the backplane) and in giving an EPC-7 program the ability to view its memory in big endian format.

A24 and A32 slave accesses result in accesses to the on-board DRAM and never to the cache. Because the EPC-7's cache is a write-through cache, there is never a discrepancy between data in the cache and the DRAM. When a slave access results in a *write* into the DRAM, the EPC-7 automatically purges the cached entry, if it exists.

Given the above, another subtle use for the ability of the EPC-7 to access its own DRAM via a VMEbus access is selective purging of the cache. For instance, if the EPC-7 is mapped at address base 18000000h in the A32 space and a program is meant to purge location 0000AB00h from the cache, a read from 0000AB00h followed by a write of the read data back to 1800AB00h will accomplish the task.

Read-Modify-Write Operations

VMEbus RMW (read-modify-write) cycles can be performed through use of the LOCK instruction prefix with certain instructions. All of these instructions perform a read followed by a write. When such a read occurs that is mapped to the VMEbus, the EPC-7 treats it as the start of a VME RMW cycle. The next VME access from the CPU is treated as the write that terminates the RMW cycle. Keep in mind that accesses that cross a 32-bit boundary are actually performed as two accesses. For this reason, RMW accesses that cross a 32-bit boundary will not behave as expected.

The EPC-7 provides synchronization integrity in its local DRAM between accesses from the CPU into the DRAM and RMW VME accesses from other masters into the DRAM.

When a VMEbus slave read access occurs to the local DRAM, the EPC-7 watches the VMEbus data and address strobes to determine if the cycle is an RMW cycle. If it is, accesses by the CPU are held up until the terminating access of the RMW cycle occurs.

When the CPU performs a locked access (e.g., via an instruction using the LOCK instruction prefix) to the local DRAM or the cache, VMEbus slave accesses are held up until the last locked access completes.

One more case of interest is when the EPC-7 performs a locked access that results in a self access. These function correctly (i.e., as if the access was not a self access), providing that operating-system tables (e.g., page tables) that are accessed by the CPU by implicit locked accesses are not mapped into VME. This would only be a concern for user-written operating systems.

VMEbus Interrupt Response

When the EPC-7's Interrupt Generator register (815F) is used to assert an interrupt, the EPC-7 formulates a status/ID value that is transmitted on the bus as the response to a matching interrupt acknowledge cycle. The EPC-7 acts as both a D08(O) and D16 interrupter. For D08 interrupt acknowledge cycles, the status/ID value is the contents of register 815C. For D16 and D32 interrupt acknowledge cycles, the status/ID value consists of 16 bits. The upper eight bits are the upper half of the response register (the value in I/O port 814B) and the lower eight bits are the contents of register 815C.

Registers Specific to EPC-7

Registers in the I/O space that are specific to the EPC-7 are defined below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I/O port
EXM Configuration Reg	reserved					Slot Number			96
Battery Backed Register	ARBPRI		RELM	ARBM	RAM	SDMA	EVME	0	8102
Memory Mode Register	MDFF	MDCF	RAM	MEMS			RAM	RAM	8104
VME A21-16 Address Reg	VMEbus address bits 21-16						RAM	RAM	8130
ID Register, lower	1	1	1	0	1	1	0	0	8140
ID Register, upper	1	0	0	A32	1	1	1	1	8141
Device Type Reg, lower	1	1	1	0	1	1	1	1	8142
Device Type Reg, upper	0	Slave Size		1	0	0	0	S	8143

Status/Control Reg, lower	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	8144
Status/Control Reg, upper	SLE	MODI	SYSR	1	1	1	1	1	8145
Slave Offset Reg, lower	1	1	1	1	1	1	1	1	8146
Slave Offset Reg, upper	Base								8147
Protocol/Signal Reg, lower	1	1	1	1	1	1	1	1	8148
Protocol/Signal Reg, upper	0	0	0	1	1	0	1	1	8149
Response Register, lower	LOCK	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG	814A
Response Register, upper	0	1	DOR	DIR	ERR	RRDY	WRDY	1	814B
Message High Reg, lower									814C
Message High Reg, upper									814D
Message Low Reg, lower									814E
Message Low Reg, upper									814F
VME A31-24 Address Reg									8150
VME Modifier Register	VME WA23-22		BORD	IACK	AM5	AM4	AM2	AM1	8151
VME Interrupt State Reg	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8152
VME Interrupt Enable Reg	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR	8153
VME Event State Register	1	1	VXRCP	SIGR	WDT	ACFA	BERR	SYSF	8154
VME Event Enable Register	DSOR	VWR	VXRCP	SIGR	WDT	ACFA	BERR	SYSF	8155
TTL Trigger Sample Reg	TTS7	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0	8156

7 7

MODID / Interrupt Gen Reg	MO04	MO03	MO02	MO01	MO00	Interrupt-out			8158
MODID Upper Register	MO12	MO11	MO10	MO09	MO08	MO07	MO06	MO05	8159
TTL Trigger Drive Register	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0	815A
ECL Trigger / Misc Reg	ES1	ES0	ED1	ED0	VXR	SBER	1	BSAM	815B
Unique Logical Addr Reg									815C
Module Status/Control Reg	1	IST	1	BTOE	WDTR	FWDT	1	1	815D
Signal Reg FIFO, lower									815E
Signal Reg FIFO, upper									815F
TTL Trigger Latch Register	TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0	8161
Clock Control Register	1	1	1	1	1	1	1	ENXC	8162
External Trigger Register	1	1	1	1	OUT	Trigger-line			8163
Trig Interrupt Enable Reg	TTI7	TTI6	TTI5	TTI4	TTI3	TTI2	TTI1	TTI0	8164

The following additional registers do not reside in the I/O space but are mapped into the VXI A16 address space.

	15							0	
A24 Shared Mem Ptr High									xx10
	15							0	
A24 Shared Mem Ptr Low									xx12
	15							0	
A32 Shared Mem Ptr High									xx14
	15							0	
A32 Shared Mem Ptr Low									xx16

	15						8	7						0	
Alternate Response Register	11111111							Copy of response register, lower							xx20

Where a bit position has been described by a 0 or 1, the bit is a ROM bit, and writing to it has no effect. Bit positions labeled "RAM" are register storage bits that have no special hardware interpretation. Unless otherwise noted below, all registers and bit values are readable and writeable.

EXM Configuration Reg

reserved	Slot Number

96

This register is used to assert a -EXMID signal to a specific EXM slot. For instance, writing the value 02 causes the -EXMID signal to be asserted for slot 2. Writing FF causes all -EXMID signals to be deasserted. Slot number can be assigned a value 0-5.

Battery Backed Register

ARBPRI	RELM	ARBM	RAM	SDMA	EVME	0

8102

This register is used by the BIOS to control certain system configuration options. The BIOS transfers information into the register at initialization time from the battery backed CMOS RAM.

ARBPRI Arbitration priority. This defines the level at which the EPC-7 will arbitrate for the VMEbus. 11 means 3, 10 means 2, 01 means 1, 00 means 0.

RELM Bus release mode. If set, the bus release mode is ROR (release on request); otherwise it is the VXI RONR "fair requester" mode (request on no request).

ARBM Arbitration mode. This bit is pertinent only if the EPC-7 is jumpered to be the VXIbus slot 0 controller. If set, the EPC-7 is a priority arbiter; otherwise it is a round-robin arbiter.

SDMA SCSI DMA channel. If set (1), the SCSI controller uses 16-bit DMA channel 5. Otherwise it uses 8-bit DMA channel 0. This bit can be used to avoid conflicts with EXM modules that might use one of these DMA channels.

EVME Enable VME master access. If set (1), master accesses to the VXI data transfer bus are enabled. Otherwise these accesses are mapped to the EXM expansion interface (using the lower 24 bits of address) and typically time out, meaning that writes appear to complete and reads return F's. EVME can be used to inhibit VXI accesses by certain operating systems (e.g., OS/2) which probe through the address space during initialization.

Whenever the EPC-7 is held in the reset state, EVME is masked off (but the register bit is not changed).

Bit 0 Set to 0.

Memory Mode Register

MDFF	MDCF	RAM	MEMS	RAM	RAM

8104

This register controls certain DRAM operational parameters.

MDFF When set (1), the 00FFxxxx region of memory is treated as normal DRAM. When 0, reads to this region are mapped into the ROM area of the address space.

MDCF This bit controls accesses to the 000Cxxxx and 000Fxxxx regions of the address space. The former is where a video BIOS and SCSI BIOS typically reside and the latter is where the ROM BIOS resides. When set (1), writes to these regions are mapped to the EXMbus and reads come from DRAM. When 0, writes are mapped to DRAM and reads from 000Cxxxx are mapped to the EXMbus and reads from 000Fxxxx are mapped to DRAM. This bit is used by the BIOS to copy itself and video and SCSI BIOS's into DRAM.

MEMS These bits control the address decoding (i.e., which addresses map to DRAM versus the EXMbus). They are set by the BIOS with the following encoding:

000	invalid (DRAM disabled)
001	invalid (DRAM disabled)
010	2 MB
011	4 MB
100	8 MB
101	16 MB
110	32 MB
111	64 MB

ID Register, lower

1	1	1	0	1	1	0	0

8140

ID Register, upper

1	0	0	A32	1	1	1	1

8141

This read-only register defines the EPC-7 as a message-based device with the manufacturer being RadiSys Corporation (manufacturer code 4076).

Since the EPC-7 is a DC device (a device whose ULA can be assigned dynamically by the resource manager), an initial write to this register address from the VXIbus assigns a ULA to the EPC-7.

A32 If set (1), the EPC-7 is an A16/A32 device; otherwise it is an A16/A24 device. This is a read-only bit that is controlled by the device type register 8143 below.

Device Type Reg, lower	1	1	1	0	1	1	1	1	8142
Device Type Reg, upper	0	Slave Size		1	0	0	0	S	8143

This register defines how much address space the EPC-7 consumes as a slave device, and defines the EPC-7's VXI model code.

Slave size Only the high-order bit (bit 6) is writeable. Bit 5 takes on the value of bit 6. That is, the two encodings are 00 and 11. If 11, the EPC-7 responds to a 16 MB range in the A32 space, and bit A32 in the ID register is set. If 00, the EPC-7 responds to a 4 MB range in the A24 space, and bit A32 in the ID register is 0.

S This read-only bit specifies if the EPC-7 has been jumpered as a slot-0 controller. 1 denotes no and 0 denotes yes. S forms part of the VXI model code, which is 239 (S=0, denoting slot-0 controller) or 495 (S=1).

Status/Control Reg, lower	SRIE	1	SYSC	1	RDY	PASS	NOSF	RSTP	8144
Status/Control Reg, upper	SLE	MODI	SYSR	1	1	1	1	1	8145

This register contains VXI specified bits and EPC-7 device-dependent bits.

SLE Slave enable. If set (1), the EPC-7 will respond to certain A24 or A32 accesses from the VXI data-transfer bus.

MODI If clear (0), it denotes that the EPC-7's MODID pin is being asserted.

SYSR SYSRESET. The EPC-7 asserts the VXI SYSRESET line while this bit is 1. When using this bit, it is software's responsibility to ensure that the VXI/VME specified minimum assertion time of SYSRESET is met. This bit is read-only when accessing this register from the VXI A16 space.

SRIE SYSRESET input enable. If set, assertion of VXI SYSRESET generates a reset of the EPC-7. One use of this bit is having software reset the VXI system (via bit SYSR) without resetting the EPC-7. This bit is read-only when accessing this register from the VXI A16 space.

SYSC SYSCLK status bit. All writes to this register have the effect of clearing this bit. The bit is then set if four rising edges of the VXI SYSCLK signal are detected. This bit is intended to be used to detect that SYSCLK is being generated on the backplane.

RDY This RAM bit, if set while PASS=1, denotes that the EPC-7 is ready to accept operational commands. Setting the RSTP bit always clears this bit.

PASS If set (1), the EPC-7 has completed its selftest successfully. If this bit is clear, the Test LED on the EPC-7 front panel is lit. The VXI SYSFAIL line is asserted whenever PASS=0 and NOSF=0. This bit is read-only when accessing this register from the VXI A16 space. Setting the RSTP bit always clears this bit.

NOSF SYSFAIL inhibit. If set, the EPC-7 cannot assert the VXI SYSFAIL line.

RSTP Reset EPC. Setting this bit will reset portions of the VME/VXI interface of the EPC-7. Reset behavior is discussed in the next chapter.

Slave Offset Reg, lower	1	1	1	1	1	1	1	1	8146
Slave Offset Reg, upper	Base								8147

7 7

This register defines the location of the EPC-7's slave memory.

Base If A32=1 and SLE=1, this field defines the upper eight bits of the A32 addresses to which the EPC-7 responds. If A32=0 and SLE=1, the upper two bits of this field define the upper two bits of the A24 addresses to which the EPC-7 responds. That is, this field defines into which of 256 16MB A32 regions or 4 4MB A24 regions the EPC-7 is mapped.

Protocol/Signal Reg, lower	1	1	1	1	1	1	1	1	8148
Protocol/Signal Reg, upper	0	0	0	1	1	0	1	1	8149

A read of this register reads the protocol register; a write writes the signal register.

The protocol register (the read value) defines the EPC-7 as being a servant and commander, having a signal register, being a bus master and an interrupter, providing the shared-memory protocol, and not providing fast handshake mode.

When written from the VXIbus, this register is the signal register. The value written enters the signal FIFO (two deep) or returns a bus error (BERR) if the FIFO is already full.

Response Register, lower	LOCK	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG	814A
Response Register, upper	0	1	DOR	DIR	ERR	RRDY	WRDY	1	814B

This register contains some VXI-defined state bits associated with message handling, and several EPC-7 dependent bits.

DOR RAM bit available to software for VXI communication protocols.

DIR RAM bit available to software for VXI communication protocols.

ERR RAM bit available to software for VXI communication protocols.

RRDY Read ready. A 1 denotes that the message registers contain outgoing data to be read by another device. RRDY is cleared when the message low register is read.

WRDY Write ready. If set, the message registers are armed for an incoming message. When a write occurs into the message-low register, WRDY is cleared and the MSGR interrupt condition is asserted.

LOCK RAM bit available to software.

ABMH This EPC-7 specific bit is cleared when the message high register is read or written from the VXIbus. It serves as a location monitor for determining whether a message is 16 or 32 bits in length.

SIG If this EPC-7 specific bit is 0, the signal register FIFO is empty.

MLCK This EPC-7 specific bit is used for synchronization of messages from multiple senders, something not provided for in the VXI specification. If 1, the message register can be locked for the sending of a message. If 0, the message register has been locked.

WRCP This EPC-7 specific bit is a read-only copy of the WRDY bit.

FSIG Defined only when SIG=1, in which case FSIG is the number (0 or 1) of the register in the FIFO holding the earliest signal.

LSIG Defined only when SIG=1, in which case LSIG is the number (0 or 1) of the register in the FIFO holding the most recent signal.

FSIG and LSIG have no utility to software. They exist as read-only bits for tests of the EPC-7 during manufacture.

The bits RRDY, WRDY, ABMH, and MLCK in the response register are altered by hardware-detected conditions. A read from the message-low clears RRDY. A write into all or the lower 8 bits of the message low register clears WRDY. A read or write to all or the lower 8 bits of the message high register clears ABMH. A read of the alternate response register clears MLCK if WRDY is set.

Message High Reg, lower		814C
Message High Reg, upper		814D
Message Low Reg, lower		814E
Message Low Reg, upper		814F

The message registers may be used to implement the VXI message protocols. The message-low register is typically used as an incoming message register for word-serial messages; the sender does D16 writes into it from the VXIbus. The message-high register is an extension for 32-bit longword serial messages. An access to this register in the A16 space on the VXIbus clears flag ABMH in the response register.

VME A31-24 Address Reg		8150

This register is one of several that supply the VXIbus address bits when the EPC-7 makes an access in its "E page." This register supplies address bits A31-A24.

VME Modifier Register

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

8151

This register is also used when the EPC-7 makes an access through its E page to the VXIbus. Bits 7 and 6 provide VXI address bits A23 and A22, respectively. Bits 3-0 define the value placed on the associated VXI address-modifier lines. Register bits are not defined for the address-modifier AM3 and AM0 lines since, for all defined address-modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware.

BORD Byte order. This bit controls the ordering of data bytes for D16 and D32 VXIbus accesses. If 0, the bytes are transmitted in little endian (Intel) order; if 1, byte-swapping hardware transmits the bytes in big endian (Motorola) order.

IACK This bit, when set, is used to define the VXIbus access as an interrupt acknowledge cycle. The interrupt being acknowledged must be encoded by software as a value on address lines A1-A3.

VME Interrupt State Reg

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR

8152

This read-only register defines the state of the VXI and message interrupts.

IRQx If clear (0), the associated VXI interrupt line is asserted.

MSGR If clear (0), a message interrupt is being signaled. MSGR is clear if both of bits RRDY and WRDY in the response register are clear.

VME Interrupt Enable Reg

IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	MSGR

8153

This is a mask of the interrupt conditions in the interrupt state register. A 1 denotes that the corresponding interrupt is enabled. If any bit in this register is a 1 and the corresponding bit in the interrupt state register is a 0, the EPC-7 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

VME Event State Register	1	1	VXRCP	SIGR	WDT	ACFA	BERR	SYSF	8154

Similar to the interrupt state register, this register defines additional conditions that may result in an IRQ10 interrupt. If the bit is 0, the condition is present.

VXRCP A reset has occurred. This is a copy of bit VXR in the ECL trigger/misc register. It provides a way to generate an interrupt because of certain reset conditions.

SIGR Signal register FIFO is not empty.

WDT The EPC-7 watchdog timer period has expired.

ACFA VXIbus ACFAIL is asserted.

BERR An access from the EPC-7 to the VXIbus was terminated with a BERR (bus error).

SYSF VXIbus SYSFAIL is asserted.

VME Event Enable Reg	DSOR	VWR	VXRCP	SIGR	WDT	ACFA	BERR	SYSF	8155

The low-order six bits are a mask of the interrupt conditions in the event state register. A 1 denotes that the corresponding event is enabled as an interrupt. If any bit in this register is a 1 and the corresponding bit in the event state register is a 0, the EPC-7 IRQ10 interrupt is asserted. Software may then examine the interrupt and event state registers to determine the cause.

The following two bits are read-only state bits:

DSOR Clear whenever either of the VXI DS0/DS1 data strobes is asserted. DSOR=0 thus indicates a data transfer in progress.

VWR When DSOR is 0, VWR=0 indicates that the data transfer is a write operation.

TTL Trigger Sample Reg	TTS7	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0	8156

This read-only register contains the state of the eight TTL trigger lines on the VXI J2 backplane. A 1 denotes an asserted trigger. Note that this register does not necessarily match the value in the TTL drive register because of the open-collector nature of the trigger lines.

MODID / Interrupt Gen Reg	MO04	MO03	MO02	MO01	MO00	Interrupt-out	8158

This register serves two purposes: driving the VXI MODID lines and generating a VXI interrupt.

If the three low-order bits are not 000, one of the seven VXI interrupt lines is asserted by the EPC-7. The line is the decoded value of these three bits (e.g., 001 denotes IRQ1, 111 denotes IRQ7). If and when an interrupt acknowledge cycle is sent to the EPC-7, the Interrupt-out bits are cleared. Software can also deassert an asserted interrupt by clearing these bits at any time. A reset of the EPC-7 or setting bit RSTP in the status/control register clears the Interrupt-out bits.

The MODID bits are explained in the context of the following register.

MODID Upper Register	MO12	MO11	MO10	MO09	MO08	MO07	MO06	MO05	8159

This register and the previous one drive and sample the LBUSA local bus signals on the VXI P2 connector. When the EPC-7 is installed in slot 0, these signals are the MODID signals on the VXI backplane. The bits named MO00-MO12 are associated with signals MODID00-MODID12.

When a write occurs to this register (8159), the EPC-7 drives the MODID signals on the backplane. A read of this register (8159) terminates the driving of the signals; the value returned from this "driver-terminating" read is not specified and should not be used. All other reads of both registers sample the MODID signals from the backplane. A reset of the EPC-7 or setting bit RSTP in the status/control register terminates driving of the MODID lines.

TTL Trigger Drive Register	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0	815A

This read/write register drives the VXI TTL trigger lines; a 1 bit causes the associated trigger line to be asserted. The actual change in state to the trigger lines is synchronized to the 10 MHz CLK10 to support the VXI trigger start/stop protocol. Reading this register does not sample the triggers; it simply returns what was previously stored in this register. Sampling the trigger lines is performed with register 8156.

A reset of the EPC-7 clears this register.

ECL Trigger / Misc Reg	ES1	ES0	ED1	ED0	VXR	SBER	1	BSAM	815B

This read/write register contains the following bits:

ES Read-only bits that show the state of the ECL trigger lines on the backplane (1 meaning asserted).

ED A 1 asserts the corresponding ECL trigger.

VXR VXI reset. This bit is cleared by an assertion of the VXI SYSRESET signal, by setting the RSTP bit in the status/control register, or by other hardware reset conditions (reset pushbutton, watchdog timer reset). It is a sticky bit that remains clear until set by software. This bit drives the bit of the same name in the event state register, one purpose of which is to give software the opportunity to handle reset as an interrupt. When this bit is cleared, it affects several other bits and registers. Please refer to the section *Reset Behavior* in Chapter 5 for more information.

SBER "Sticky BERR." This bit is cleared whenever a VXI data-transfer bus access by the EPC-7 is terminated by a BERR. By initially setting the bit and then performing a series of data transfers, software can determine if a bus error occurred. (Alternatively, software could examine the BERR bit in the event state register after each access, or enable the BERR event to generate an interrupt.)

BSAM This bit is 0 if a pipelined write is active from the EPC-7 onto the VXI data-transfer bus. It allows software to wait for the completion of a write (e.g., to determine when SBER can safely be examined after a series of writes).

7 7

Unique Logical Addr Reg		815C

This register contains the EPC-7's ULA. Until a value is stored in this register, the EPC-7's register base in the A16 space is FFC0, and it responds only when its MODID is asserted. The ULA is changed by writing into this register or into the ID register).

Module Status/Control Reg	1	IST	1	BTOE	WDTR	FWDT	1	1	815D

This register contains the following miscellaneous status and control bits:

IST Interrupt status type. This bit specifies whether a response status/ID or an event status/ID is used in an interrupt acknowledge cycle.

If IST is 0, the response format is used. In the 16-bit status/ID value returned, the upper 8 bits are the value of the upper 8 bits of the response register, and the lower 8 bits are the EPC-7's ULA.

If IST is 1, the event format is used. The upper 8 bits of the status/ID value are the value of the upper 8 bits of the message high register, and the lower 8 bits are the EPC-7's ULA. In this case software uses the message high register for the event code, meaning that longword serial messages cannot be used at the same time.

BTOE Bus timeout enable. Enables the slot-0 bus timeout timer. This is used by the BIOS.

WDTR Watchdog timer reset enable. If 1, expiration of the watchdog timer generates a reset of the EPC-7. If 0, only the WDT event is signaled.

FWDT Fast watchdog timer. If clear, the period of the watchdog timer is about 6.7 seconds. If set, the period is about 210 ms.

A read of the module status/control register also has a side effect of resetting the watchdog timer. Therefore, if you are using the watchdog timer, the intention is that you are required to read this register within the defined period of the timer to prevent its generating an interrupt.

Signal Reg FIFO, lower		815E
Signal Reg FIFO, upper		815F

If the signal register FIFO is not empty, a read of these registers returns the oldest value in the FIFO. The value is removed from the FIFO upon reading of the "lower" byte (port 815E). If the FIFO is empty, the value returned is not specified.

TTL Trigger Latch Register	TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0	8161

This register catches assertions of the TTL trigger that last longer than 30 ns. A read of the register returns the latched contents and clears the latches immediately thereafter. The duration of the clear pulse is 125 ns.

This register is intended for use in implementing the asynchronous trigger protocol defined in the VXI specification. Note that the register should be read repeatedly until it is seen to be cleared. The register is not cleared by reset.

Clock Control Register	1	1	1	1	1	1	1	ENXC	8162

ENXC has meaning only when the EPC-7 is configured as the slot-0 controller. If ENXC is set (1), the clock source attached to the CLOCK10 input on the front panel is used to drive the VXI CLOCK10 signal on the backplane. If ENXC is 0, the VXI CLOCK10 signal on the backplane is driven by an internal 10 MHz clock having an accuracy of ± 100 ppm.

A write to this register will cause the CLOCK10 signal to stay in the high state for the duration of the I/O write cycle to meet the requirements of rule B.6.4 of the VXI specification.

If ENXC is set and there is no external clock source connected, it cannot be cleared by writing 0 to the register; a hardware reset will be necessary. This provides a way to test for the presence of the external clock signal. To do so, (1) set ENXC to 1, (2) try to write 0 to EXNC, (3) read EXNC; if 1, issue a warning message and request that the system be reset; if 0, set ENXC back to 1.

External Trigger Register	1	1	1	1	OUT	Trigger-line	8163

This register controls the external TTL trigger connector on the front panel.

OUT — If set (1), the external trigger is an output. If 0, the external trigger is an input.

Trigger-line — Specifies the TTL trigger line from the backplane to be connected to the external trigger connector. 000 specifies TTLTRG0, ..., 111 specifies TTLTRG7.

Trig Interrupt Enable Reg	TTI7	TTI6	TTI5	TTI4	TTI3	TTI2	TTI1	TTI0	8164

This is a mask of the interrupt conditions in the trigger latch register. A 1 denotes that the corresponding interrupt is enabled. If any bit in this register is a 1 and the corresponding bit in the trigger latch register is a 1, the EPC-7 IRQ10 interrupt is asserted. Software may then examine the interrupt state register, event state register, and trigger latch register to determine the cause.

The following registers are mapped as offsets from the EPC-7's VXI A16 base address.

	15 … 0	
A24 Shared Mem Ptr High		xx10
A24 Shared Mem Ptr Low		xx12
A32 Shared Mem Ptr High		xx14
A32 Shared Mem Ptr Low		xx16

These registers form a 32-bit address register for the optional shared-memory protocol. There are only a total of 32 physical register bits. If bit A32 in the ID register is 1, the shared-memory register is mapped at offset 14 in the EPC-7's register space in the VXI A16 address space. If A32=0, the register is mapped at offset 10.

	15 – 8	7 – 0	
Alternate Response Register	11111111	Copy of response register, lower	xx20

bits 7-0	LOCK	1	ABMH	SIG	MLCK	WRCP	FSIG	LSIG

The upper half of this register is 1111 1111 and the lower half is a read-only copy of the lower half of the response register. The alternate response register is associated with multiple senders of messages to the EPC-7 and the MLCK bit; reading this register performs a test-and-set operation on MLCK if WRDY is set (WRDY in the response register).

The protocol for synchronization of multiple senders of messages is as follows. A sender must first read the alternate response register. If both WRCP (WRCP is a copy of WRDY) and MLCK are set, the sender can send the message; otherwise the sender must reread the alternate response register until this condition is true. For 16-bit messages, the sender writes into the message low register. For 32-bit messages, the sender must write into the message high register before writing into the message low register.

Register State after Reset

A hardware reset of the EPC-7 (not a keyboard CTRL+ALT+DEL reset) clears all of the register bits to 0 in the following registers (except those bits defined as a constant 1): 8130, 8150, 8151, 8158 bits 0-2, 815A, and 8163. This shuts down transfers to the data-transfer bus and driving of trigger and interrupt lines. Also, during reset, bit EVME in the battery backed register is masked off, the VXI reset condition (VXR) is set, and the sticky BERR condition is masked on, which causes any outgoing VXI data transfers to appear to complete with bus error without actually accessing the VXI bus.

The BIOS clears the VME interrupt and event enable registers during initialization.

VXIbus Mapped Registers

The EPC-7 contains a set of configuration and operational registers mapped into the VXIbus A16 address space as 16-bit registers. These registers begin at a base related to the EPC-7's logical address. This base is given by

11uu uuuu uu00 0000

where uuuuuuuu is the EPC-7's unique logical address (ULA). The EPC-7 is a VXI DC device (dynamic configuration), meaning that after a system reset, its ULA is FFh, and it only responds to A16 accesses at the resultant base FFC0h and beyond if the MODID line is asserted. Once the EPC-7 is assigned a ULA, uuuuuuuu becomes this new ULA (whose value appears in the ULA register).

The mapping of registers in the A16 space is shown in the following table. For registers that are also accessible from within the EPC-7 via an I/O address, the I/O address is given in parentheses.

Offset	Upper byte	Lower byte
0	ID (8141)	ID (8140)
2	Device type (8143)	Device type (8142)
4	Status/control (8145)	Status/control (8144)
6	Slave offset (8147)	Slave offset (8146)
8	Protocol/signal (8149)	Protocol/signal (8148)
A	Response (814B)	Response (814A)
C	Message high (814D)	Message high (814C)
E	Message low (814F)	Message low (814E)
10	A24 shared memory pointer high	
12	A24 shared memory pointer low	
14	A32 shared memory pointer high	
16	A32 shared memory pointer low	
20	Alternate response register	

Table 16. A16 Register Mapping.

Supported Address Modifiers

2Dh	A16 supervisor
39h	A24 non-privileged data
3Ah	A24 non-privileged program
3Dh	A24 supervisor data
3Eh	A24 supervisor program
09h	A32 non-privileged data
0Ah	A32 non-privileged program
0Dh	A32 supervisor data
0Eh	A32 supervisor program

Table 17. Supported Address Modifiers.

Low-Level Programming the VMEbus Interface

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It is recommended that rather than performing accesses in this low-level hardware dependent form, the BusManager component of the EPConnect software package be used instead.

VMEbus Accesses

Two examples are given here including both a verbal description and the Microsoft C source code for performing VMEbus accesses through the "E" page.

Example #1 performs a 16-bit read from the VMEbus A16 space.

1. Set the EVME access bit in Register 8102.

2. Determine the correct address modifier for A16 supervisory access (2Dh)

3. The unused address lines A31-A16 may float when not being used. Registers 8150 and 8130 must be set so that each line is a 1.

   Set register 8130 to FCh and register 8150 to FFh.

4. Set the access mode in the VME Modifier Register (8151) as follows:

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

(Note that register bits are not defined for the VMEbus address modifier lines AM3 and AM0 since, for all defined address modifier values in the VMEbus specification, AM3 is 1 and AM0 is the inverse of AM1. Therefore these two bit values are generated by hardware.)

Bits 7 & 6 Since the A16 space does not use VMEbus address lines A23 & A22, set these values to 1.

VME WA 23-22 = 11

Bit 5 Set the byte order to "little endian".

BORD = 0

Bit 4 Clear the IACK bit so this is not an interrupt acknowledge cycle.

IACK = 0

Bits 3-0 Use the address modifier (in binary form) to determine the appropriate values for these bits. 2Dh = 00**<u>10</u>**1**<u>10</u>**1b

Bit 3 (Address Modifier bit 5) = 1
Bit 2 (Address Modifier bit 4) = 0
Bit 1 (Address Modifier bit 2) = 1
Bit 0 (Address Modifier bit 1) = 0

Thus, 8151 should be set to 1100 1010 or CAh.

5. Map the address.

   Add the A16 address to the "E page" address

   Addr ← E0000000 + A16 address

6. Read the data.

Data ← value pointed to by Addr

Microsoft C code for Example 1 -

```
#define WORD  unsigned short
#define LWORD unsigned long

WORD addr;   /* 16-bit A16 address */
WORD data;
WORD far * wptr;

outp(0x8102,(inp(0x8102)|2));        /* set VME access bit */
outp(0x8130,0xFC);
outp(0x8150,0xFF);
outp(0x8151,0xCA);  /* Set address modifier to A16 supervisory access */
wptr = (WORD far *) (0xE0000000L + addr);
data = *wptr;       /* Read through window */
```

Example #2 performs a byte (8-bit) write into the VMEbus A32 space. Here the upper 16 bits of the VME address need to be stored in the appropriate registers.

1. Set the VME access bit in Register 8102.
2. Set register 8150 with the value corresponding to the 8 high-order address bits.

VMEbus Address bits 31-24 WA31-24

3. Determine the correct address modifier for A32 supervisory access.
4. Calculate the value and set register 8151 as follows:

VME WA23-22	BORD	IACK	AM5	AM4	AM2	AM1

Bits 7 & 6	VME address bits 23-22
Bit 5	BORD = 0
Bit 4	IACK = 0
Bits 3-0	Bit 3 (Address Modifier bit 5)
	Bit 2 (Address Modifier bit 4)
	Bit 1 (Address Modifier bit 2)
	Bit 0 (Address Modifier bit 1)

5. Set register 8130 with the value corresponding to bits 21-16 of the VMEbus address with the two low order bits of the register set to 0.

VMEbus Address bits 21-16	Res	Res

6. Map the address.

7. Write the data

Microsoft C code for Example 2 -

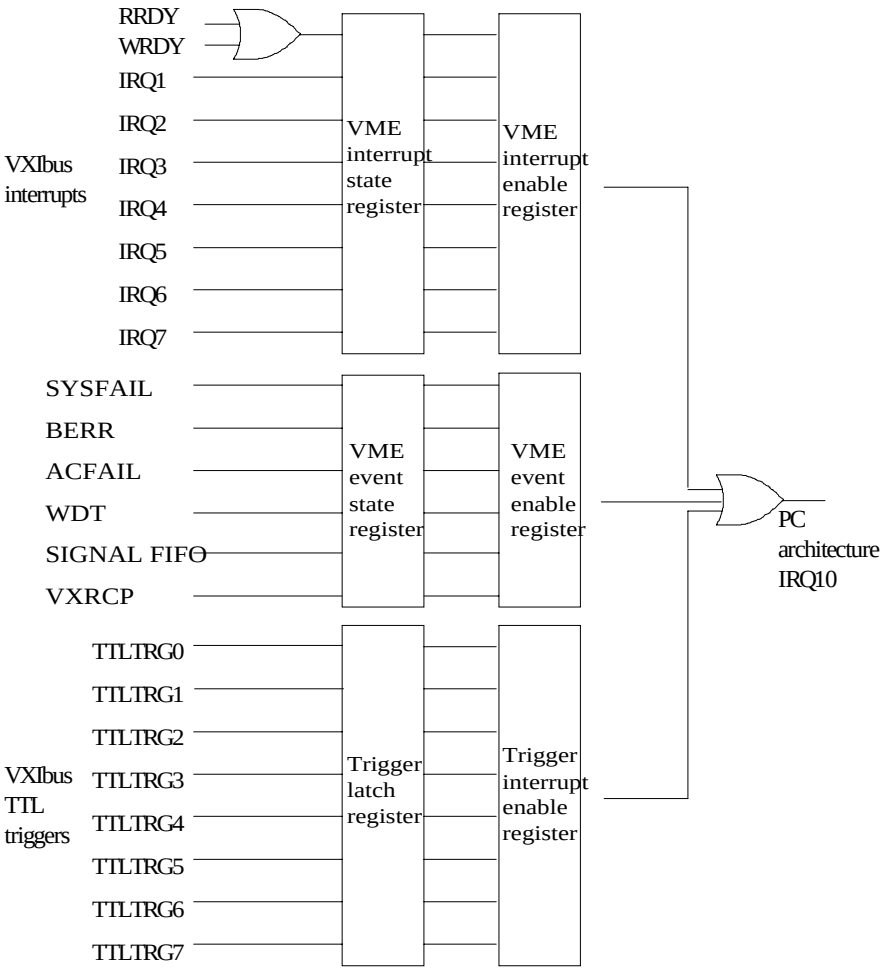
```
LWORD addr;   /* 32-bit A32 address */
BYTE  data;
BYTE  far * wptr;


outp(0x8102,(inp(0x8102)|2));                /* set VME access bit */
outp(0x8150,(WORD)(addr >> 24));          /* A31-A24 */
outp(0x8151,2 | (((addr << 8) >> 30) << 6));
  /* A23-A22 and address modifier for A32 supervisory data access */
outp(0x8130,(WORD)((addr << 10) >> 24);  /* A21-A16 */
wptr = (BYTE far *) (0xE0000000L + (addr & 0X0000FFFFL));
*wptr = data;                            /* Write through window */
```

The success of the access can be checked either by enabling BERR as an interrupt or by looking at the BERR bit in the event state register (8154) after each access. Since writes are pipelined, software that looks at the BERR bit should first wait until the DONE bit is set.

VXIbus Interrupt Handler

Although software available for the EPC-7 shields the user from the details of interrupt handling, the following information is provided for the reader who needs further detail.

The relationship between VME/VXI interrupts (and other interrupt-causing events) and an interrupt as seen by a program is shown in the following diagram.



Interrupt-causing signals are visible in three state registers. Most of these are unlatched, meaning that a read of the state register shows the actual state of the signals at the instant of the read.

The exceptions are (1) BERR, which is a "sticky" bit, meaning that the bit signifies whether BERR had ever been asserted (the VXR register bit), and (2) the TTL trigger signals, which for interrupt purposes are taken from the trigger latch register. The convention used is that a 0 bit signifies an asserted (interrupting) state.

The primary purpose of the state registers is to let the interrupt handler software determine which interrupts and events generated the IRQ10 interrupt to the processor.

The state registers can also be read by non-interrupt-handler software to poll for the state of these signals.

The enable registers allow one to mask selectively these 22 status signals. A 0 status bit and a corresponding 1 enable bit causes the PC architecture IRQ10 interrupt to be asserted.

Unlike the 22 input conditions, which are level sensitive inputs, the PC architecture defines the PC interrupts, such as IRQ10, as edge sensitive. This requires special attention if you are writing your own interrupt handlers. Because IRQ10 is edge triggered, you could miss an incoming interrupt/event that occurs when IRQ10 is disabled, meaning that your software needs to test for and handle all pending interrupts/events before you leave from the IRQ10 interrupt handler. To do this correctly, follow the following steps. These steps assume the reader is familiar with the programming of the 8259 interrupt controller in the PC architecture.

1. Depending on your environment, you may wish to switch to another stack (a must under DOS), and may wish to save the state of the VME modifier and address registers if you will be using them.
2. To prevent reentry to the interrupt handler, mask off all the interrupts/events or mask off the IRQ10 interrupt. (Reenable what you have masked off at the end of the interrupt handler.)
3. Acknowledge the interrupt by sending end-of-interrupt to both 8259 interrupt controllers.
4. Find an enabled pending interrupt/event.
5. If an enabled pending VXIbus interrupt is found, do an interrupt-acknowledge cycle by setting the IACK bit in the VME modifier register and performing a VMEbus read, setting address bits A3-A1 to denote the interrupt number. This returns the status/ID value from the interrupter. For the other controllable conditions (message, sticky BERR, watchdog timer), you may follow the instructions earlier in this chapter to remove these interrupting conditions.
6. Perform application-dependent handling of the interrupt/event.
7. If there are still enabled pending interrupts/events, go to step 4. If not, return from the IRQ10 interrupt handler.

Read-Modify-Write Operations

The EPC-7 provides synchronization integrity in its local DRAM between accesses from the 486 into the DRAM and RMW VXI accesses from other masters into the DRAM.

When a VXIbus slave read access occurs to the local DRAM, the EPC-7 watches the VXIbus data and address strobes to determine if the cycle is an RMW cycle. If it is, accesses by the 486 are held up until the terminating access of the RMW cycle occurs.

When the 486 performs a locked access (e.g., via an instruction using the LOCK instruction prefix) to the local DRAM, VXIbus accesses are held up until the last locked access completes.

One more case of interest is when the EPC-7 performs a locked access that results in a self access. These function correctly (i.e., as if the access were not a self access), providing that operating-system tables (e.g., page tables) that are accessed by the 486 by implicit locked accesses are not mapped into VXI. This would only be a concern for user-written operating systems.

VXIbus RMW (read-modify-write) cycles can be performed through use of the 486's LOCK instruction prefix with certain instructions. All of these instructions perform a read followed by a write. When such a read occurs that is mapped to the VXIbus, the EPC-7 treats it as the start of a VXI RMW cycle. The next VME access from the 486 is treated as the write that terminates the RMW cycle. For this reason, RMW accesses that cross a 32-bit boundary will not behave as expected (because the 486 issues two read accesses).

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Soft Reset and VME Sysreset

The EPC-7 supports two device states specified by the VXI: soft reset and safe. These states are identical except that, in the safe state, the EPC-7 cannot drive SYSFAIL. The soft reset state is entered by setting bit RSTP. Setting bit NOSF when FSTP is set denotes the safe state.

In the soft reset state, a device is inactive, interrupts which are pending are unasserted, and all pending bus requests are removed. While in this state, the device's VMEbus slave interface is active. To achieve this functionality without resetting everything on the board, the EPC-7 performs a sequence of events when RSTP bit is set or when VME SYSRESET is asserted and SYSREST INPUT ENABLE bit is clear (bit 7 of VSC, register 8144). This disables the SYRESET - PCRESET logic. The following sequence occurs:

Bit VXR of the VET register (VXI Reset, bit 3 of register 815B) is asynchronously cleared as long as RSTP is set. The VXR bit, when asserted, causes an interrupt if bit 5 of the BEE register (8155) is set. An asserted VXR bit places several other register bits in the reset state. Bits 2-0 of VMOL (8158) are held asynchronously reset by the VXR bit. This removes any pending interrupt request from the bus. The VXR bit also disables VME/VXI accesses from occurring by masking off the VMEEN bit (bit 1 of 8102). This steers all VME/VXI memory references onto the AT bus (EOX, EOI). SBER, bit 2 of the VET register, is also cleared by VXR, but bit BERRR (bit 1 of BES, register 8154) is not cleared. In addition, the TTD (TTL Trigger Drive register, 815A) the BMA (8130/8132/8134/8136), BWA (8159), BWM (8151), and the ETR (8163) registers are cleared by the VXT bit.

Finally, TTLTRIG0 drive is disabled while the VXR is asserted (This bit is treated differently than the other Trigger drive bits since clearing the ETR may cause the external trigger to drive TTLTRIG0).

Software can recognize the safe/soft reset states in the following ways:

1) Enable VXR interrupt.

When a VXR interrupt is handled, check the VSC register to see if this is the safe or soft reset state. If the RSTP bit is set, then software must wait to be reset from the soft reset state. When this has been done by another VME/VXI agent, software must still reset the VXR bit in the VET register before VME activity can again commence. This is accomplished by writing a 1 into bit position 3 of register 815B. Also, SBER should be reset at this time. If the RSTP bit is clear and the PASSED bit is clear, then an external VXI agent has both set the board into the soft or safe states and then reset the RSTP bit, before the interrupt handler had a chance to handle the safe/soft reset state. The VXR and SBER bit must again be reset by software. If the RSTP bit is clear and the PASSED bit is set, the VME SYSREST was asserted and software is free to perform whatever cleanup actions it desires. Again, the VXR and SBER bits should be reset before attempting any VME bus accesses.

2) Poll SBER after VME/VXI bus accesses.

IF SBER is asserted by itself, then a BERR response occurred to one of the VME accesses. If both SBER and VXR bits are asserted, then the checking described in point 1 must be followed to determine the source of the VXR.

Two conditions generate hardware resets that include resetting all of the hardware. One is receipt of VME SYSREST with bit SRIE set. The other is expiration of the watchdog timer period, when bit WDA is set (meaning that one wants the watchdog timer to generate a reset rather than an interrupt).

8. Upgrades

✉ **DO NOT HANDLE THE EPC-7 MODULE UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT.**

Memory

The EPC-7 can be configured for 4 MB, 8 MB, 16 MB or 32 MB. The 32 MB configuration is a factory build-time option only.

The 33 MHz and 50 MHz EPC-7 memory configurations use SIMMs with the following specifications:

- 72 pin
- fast page mode
- 80 nanosec. (or better)
- single-sided

For 4 MB,	Use 4 each 256K x 36 SIMMs. RadiSys P/N 70-0032 We recommend Toshiba THM362500ASG-80
For 8 MB,	Use 2 each 1M x 36 SIMMs. RadiSys P/N 70-0042 We recommend Toshiba THM361000ASG-80
For 16 MB,	Use 4 each 1M x 36 SIMMs. RadiSys P/N 70-0042 We recommend Toshiba THM361000ASG-80
For 32 MB,	Not upgradeable. This is a factory build-time option only.

The 100 MHz EPC-7 memory configurations use SIMMs with the following specifications:

- 72 pin
- fast page mode
- 60 nanosec. (or better)
- single-sided or double-sided

For 8 MB,	Use 2 each 1M x 36 SIMMs. RadiSys P/N 70-0074
For 16 MB,	Use 4 each 1M x 36 SIMMs. RadiSys P/N 70-0074
For 32 MB,	Use 2 each 4M x 36 SIMMs. RadiSys P/N 70-0075
For 64 MB,	Use 4 each 4M x 36 SIMMs. RadiSys P/N 70-0075

The EPC-7 SIMMs work in pairs. When configuring an EPC-7 with two SIMMs, the SIMMs should be placed in sockets 1 and 3. Sockets 2 and 4 should remain empty. See Figure 18 below for SIMM socket locations.

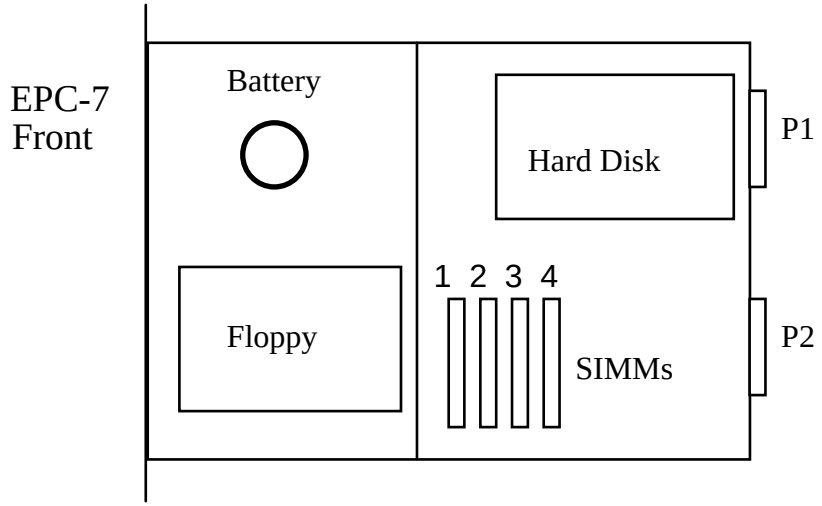

Figure 18. Location of SIMM sockets.

After upgrading the memory, reboot the system. The error message "`Memory Size error - run setup`" will display after the power-on self-test completes. Press CTRL+ALT+ESC to enter the Main Setup Menu. Verify that the top line of this screen shows the correct amount of memory. Press F10 to save and F5 to confirm and reboot. The system will reboot and no error messages should be displayed.

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9. Troubleshooting & Error Messages

Troubleshooting

This section deals with problems that you may encounter that do not provide an error message. If an error message is displayed, see the next section of this chapter, *Common Error Messages*.

Symptoms	Possible cause(s)	Solution
System appears to boot (evidenced by RUN LED being on, floppy and hard disk being accessed) but provides no video.	Video adapter not fully seated.	Remove the video adapter.
	Monitor or cable problem.	Verify that the cable pins are not bent and the cable is fully seated in the video adapter. If necessary, try the monitor on another system to verify that the monitor is good.
	Video adapter failure.	Call RadiSys Technical Support.
	EPC-7 cannot talk to EXM expansion interface.	Call RadiSys Technical Support.

Symptoms	Possible cause(s)	Solution
System fails at power-up - will not run power-on self-test.	The system is not getting power.	Check the backplane and verify that +5V power is good. Verify that the EPC-7 is fully seated in the chassis.
	Hardware failure.	This cannot be diagnosed in the field. Call RadiSys Technical Support.
Serial port(s) do not work.	Bad power.	Verify that backplane +12V and -12V are good.
	Interrupt conflicts	An EXM module is using the same interrupts as COM1 and/or COM2. Verify that no other card in the EPC-7 subsystem is using IRQ3 or IRQ4.
	Port hardware failure.	Call RadiSys Technical Support.
System hangs during boot process (Master LED on; RUN LED off)	Chassis has no Slot-0 controller providing bus timeout.	You are probably loading an expanded memory manager (for example, EMM386.EXE) in your CONFIG.SYS file. This can cause the system to hang if - there is no Slot-0 controller - the Slot-0 controller is not providing the proper bus timeout - the Bus Grant jumpers are not installed.

System will not talk across VMEbus.	The VMEbus backplane may not be jumpered correctly.	See the section *Installing the VXIbus Backplane Jumpers*, on page 7.
	More than 1 master may be set to provide Slot-0 functions.	Make sure that only 1 system is configured as the Slot-0 controller and that it is the left-most system in the chassis.
	The EPC-7 may have bent pins.	Remove the EPC-7 and verify that no pins are bent. Then reinsert the EPC-7.
	VMEbus interface failure.	Power off, then back on. Verify that the results of the power-on self test indicate VMEbus interface and VXIbus interface report “ok.”

Common Error Messages

This section contains a summary of error and warning messages alphabetized by message text. These are messages generated by the BIOS and MS-DOS that may be related to your hardware configuration.

CMOS CHECKSUM INVALID

Problem: Something in the nonvolatile CMOS RAM is incorrect.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-7's battery has failed.

CMOS RAM ERROR, CHECK BATTERY / RUN SETUP

Problem: Something in the nonvolatile CMOS RAM is incorrect.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-7's battery has failed.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

Problem: No boot disk could be found.

Solution(s): This could occur in several different ways.

Your hard disk may not have been partitioned into logical drive(s). PCs look for logical drives to boot from. Hard disks are physical drives; partitions are logical drives.

Your BIOS setup screen has all disks disabled, or if your hard disk is disabled and no floppy diskette is inserted in the A: drive. Run the BIOS setup program and verify that all disk parameters are correct. If they are, insert a bootable floppy disk in the A: drive and press enter. If a hard disk is present, verify that it is properly partitioned and formatted as a system disk and one partition is set active.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Problem: The floppy diskette installed in the system does not match the configuration information listed in the BIOS setup screen. This may be due to incorrect entries in the BIOS setup screen or the drive may not be responding at power-up.

Solution(s): Press CTRL+ALT+ESC to run the BIOS setup program. Make sure the BIOS setup entries relating to floppy drives correctly reflect the attached floppy drives. If a floppy exists, drive A should be set to "1.4M". If you have no floppy drive, both drive A should be set to none.

ERROR INITIALIZING HARD DISK 0

Problem: The IDE disk controller for drive C cannot be initialized.

Solution(s): The EPC-7 uses an internal IDE interface and drive. If it fails, either the setting is wrong or the system needs repair.

If you are not using an IDE drive, press CTRL+ALT+ESC to enter the BIOS setup program. Press F3 to enter the Fixed disk menu. Change the drive type to match the device being used.

EXM CONFIGURATION ERROR

Problem: The EXMs installed (or not installed) do not match the configuration information in the CMOS Setup.

Solution(s): Press CTRL+ALT+ESC to run the BIOS setup program. Press F2 to enter the EXM menu. Verify the information listed on the screen, save any changes and reboot.

If necessary, refer to the section *EXM Setup Screen*, shown in Chapter 4 of this manual, and/or refer to your EXM manual(s) for more details.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Problem: The configuration information in the BIOS setup says that one or more floppy disk drives are expected, but a floppy disk controller could not be found.

Solution(s): If you have no floppy diskette drives, enter the setup program and set both floppy drives to "NONE."

If you should have a floppy diskette drive configured, return the EPC-7 to RadiSys for repair.

GENERAL FAILURE READING DRIVE ...

Problem: This almost always indicates the presence of an unformatted hard disk partition or diskette.

Solution(s): Format the partition or diskette using the utilities supplied by your operating system.

INVALID DRIVE SPECIFICATION

Problem: You are trying to access a logical drive (e.g., A:, B:, ...) that is not known to the operating system.

Solution(s): Select a different logical drive. If you are trying to access a hard disk, you may need to create the logical partition.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Problem: This message indicates that the system did not recognize a keyboard at power-up or you pressed a key during the power-on self test.

Solution(s): Check the integrity of the keyboard connector.

If you think you pressed a key during power-up, reboot the system using the front panel reset button.

Some keyboards are designed with a switch (or jumper) to allow the user to configure the keyboard for use with an AT machine or an XT machine. If this is the case with your keyboard, verify that the switch is in the AT position.

The keyboard may not be a valid PC/AT keyboard (e.g., it is a PC/XT-only or PS/2 keyboard). If this is the case, replace the keyboard with a PC/AT style keyboard.

MEMORY PARITY INTERRUPT AT ...

Problem: This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Solution(s): Attempt to repeat the error. If the error occurs during the execution of your own proprietary software, verify that the memory location specified in your software is valid.

MISSING OPERATING SYSTEM

Problem: Although the system could read the hard disk and find the active partition, the operating system files could not be found.

Solution(s): This is can be caused by using a drive type number in the Fixed Disk Menu that does not match the type number used to format the hard disk. Press CTRL+ALT+ESC to run the BIOS setup program. Press F3 to enter the Fixed Disk Menu. Select the correct drive type to match the type used to format the disk originally. Save the changes and reboot the system.

This can also occur if the hard disk is partitioned and one partition is set active, but the partition was not formatted.

NON-SYSTEM DISK OR DISK ERROR
REPLACE AND PRESS ANY KEY WHEN READY

Problem: This is caused by an attempt to boot from a disk or diskette that is not recognized as a system disk; that is no system files exist on the disk or diskette.

Solution(s): Most often it results when you reboot with a non-system diskette in the floppy drive, because the BIOS always attempts to boot from the floppy drive if a diskette is installed.

If you are trying to boot from the hard disk, make sure that you do not have a diskette in the A: drive and press any key.

If you are trying to boot from floppy, insert a known good bootable system diskette in the A: drive and press any key.

NOT READY READING DRIVE ...

Problem: This is usually caused by not fully inserting a diskette into the floppy drive.

Solution(s): Eject the floppy diskette and reinsert making sure that the diskette seats completely into the floppy drive.

PARITY ERROR IN SEGMENT ...

Problem: This could be a software error (reading a nonexistent memory area) or a true hardware failure.

Solution(s): Attempt to repeat the error. If the error occurs during the execution of your own proprietary software, verify that the memory location specified in your software is valid.

PRESS A KEY TO REBOOT

Problem: A C: drive partition exists but is not set active.

Solution(s): Run your operating system disk partitioning program (like FDISK) and set the primary partition active.

REAL TIME CLOCK ERROR - RUN SETUP

Problem: The battery-backed TOD clock is incorrect.

Solution(s): Run the BIOS setup program to determine what is wrong, and correct it. If the error occurs repeatedly, the EPC-7's battery has failed.

SCSI related problems

SCSI DEVICE WON'T BOOT

Problem: BIOS extension ROM is not enabled for the SCSI device to boot.

Solution(s): The fixed disk drive in the main setup menu must be set to specify NONE as the drive type. The hard drive must be partitioned and formatted on the EPC-7 and the SCSI partition must be the active partition. Run your operating system disk partitioning program (like FDISK) and set the primary partition active. See your operating system manual for instructions on formatting a disk.

Always attempt to solve the problem yourself first. If you are unable to solve the problem, call RadiSys Technical Support at (503) 646-1800.

NOTES

10. Support and Service

In North America

Technical Support

RadiSys maintains a technical support phone line at (503) 646-1800 that is staffed weekdays (except holidays) between 8 AM and 5 PM Pacific time. If you have a problem outside these hours, you can leave a message on voice-mail using the same phone number. You can also request help via electronic mail or by FAX addressed to RadiSys Technical Support. The RadiSys FAX number is (503) 646-1850. The RadiSys E-mail address on the Internet is *support@radisys.com*. If you are sending E-mail or a FAX, please include information on both the hardware and software being used and a detailed description of the problem, specifically how the problem can be reproduced. We will respond by E-mail, phone or FAX by the next business day.

Technical Support Services are designed for customers who have purchased their products from RadiSys or a sales representative. If your RadiSys product is part of a piece of OEM equipment, or was integrated by someone else as part of a system, support will be better provided by the OEM or system vendor that did the integration and understands the final product and environment.

Bulletin Board

RadiSys operates an electronic bulletin board (BBS) 24 hours per day to provide access to the latest drivers, software updates and other information. The bulletin board is not monitored regularly, so if you need a fast response please use the telephone or FAX numbers listed above.

The BBS operates at up to 14400 baud. Connect using standard settings of eight data bits, no parity, and one stop bit (8, N, 1). The telephone number is (503) 646-8290.

Repair Services

Factory Repair Service is provided for all RadiSys products. Standard service for all RadiSys products covers factory repair with customers paying shipping to the factory and RadiSys paying for return shipment. Overnight return shipment is available at customer expense. Normal turn-around time for repair and re-certification is five working days.

Quick Exchange services (immediate shipment of a loaner unit while the failed product is being repaired) or other extra-cost services can be arranged, but need to be negotiated in advance to allow RadiSys to pool the correct product configurations. RadiSys does not maintain a general "loaner" pool: units are available only for customers that have negotiated this service in advance.

RadiSys does not provide a fixed-price "swap-out" repair service, as customers have indicated that issues of serial number tracking and version control make it more convenient to receive their original products back after repair.

Warranty Repairs

Products under warranty (see warranty information in the front of this manual) will have manufacturing defects repaired at no charge. Products sent in for warranty repair that have no faults will be subject to a recertification charge. Extended Warranties are available and can be purchased at a standard price for any product still under warranty. RadiSys will gladly quote prices for Extended Warranties on products whose warranties have lapsed; contact the factory if this applies.

Customer induced damage (resulting from misuse, abuse, or exceeding the product specifications) is not covered by the standard product warranty.

Non-Warranty Services

There are several classes of non-warranty service. These include repair of customer induced problems, repairs of failures for products outside the warranty period, recertification (functional testing) of a product either in or out of warranty, and procurement of spare parts.

All non-warranty repairs are subject to service charges. RadiSys has determined that pricing repairs based on time and materials is more cost-effective for the customer than a flat-rate repair charge. When product is received, it will be analyzed and, if appropriate, a cost estimate will be communicated to the customer for authorization. After the customer authorizes the repair and billing arrangements have been made, the product will be repaired and returned to the customer.

A recertification service is provided for products either in or out of warranty. This service will verify correct operation of a product by inspection and testing of the product with standard manufacturing tests. There is a product-dependent charge for recertification.

There are only a few components that are generally considered field-repairable, but, because RadiSys understands that some customers want or need the option of repairing their own equipment, all components are available in a spares program. There is a minimum billing charge associated with this program.

Arranging Service

To schedule service for a product, please call RadiSys Technical Support directly at (503) 646-1800. Have the product model and serial numbers available, along with a description of the problem. A Technical Support representative will issue a Returned Materials Authorization (RMA) number, a code number by which we track the product while it is being processed. Once you have received the RMA number, follow the instructions of the Technical Support representative and return the product to us, freight prepaid, with the RMA number clearly marked on the exterior of the package. If possible re-use the original shipping containers and packaging. In any case, be sure you follow good ESD-control practices when handling the product, and ensure that anti-static bags and packing materials with adequate padding and shock-absorbing properties are used.

Ship the product, freight prepaid, to

Product Service Center
RadiSys Corporation
15025 SW Koll Parkway
Beaverton, Oregon 97006-6902

When shipping the product, include the following information: return address, contact names and phone numbers in purchasing and engineering, and a description of the suspected problem. Any ancillary information that might be helpful with the debugging process will be appreciated.

Other Countries

Contact the sales organization from which you purchased your RadiSys product for service and support.

Appendix A: Interrupts & DMA Channels

Interrupts and DMA Channels

All of the following interrupts are used on the EPC-7 and cannot be disabled (except COM1, COM2, and LIP1, which can be disabled in the Setup Screen.) The assignment of interrupts is shown in the following table:

NMI	DRAM parity error, EXM expansion interface I/O channel check
IRQ0	timer
IRQ1	keyboard
IRQ3	COM2 serial port
IRQ4	COM1 serial port
IRQ5	unassigned
IRQ6	floppy disk controller
IRQ7	LPT1 parallel port
IRQ8	clock
IRQ9	unassigned
IRQ10	VXI interrupt/event
IRQ11	SCSI controller
IRQ12	unassigned
IRQ13	unassigned
IRQ14	IDE disk
IRQ15	unassigned

Table 18. Interrupt Assignments.

The assignment of DMA channels is shown in the following table.

0	SCSI or unassigned (see battery-backed register)
1	unassigned
2	floppy disk controller
3	unassigned
5	SCSI or unassigned (see battery-backed register)
6	unassigned
7	unavailable

Table 19. DMA Channels.

Appendix B: I/O Map

I/O Map

The following defines the I/O addresses decoded by the EPC-7. It does not define addresses that might be decoded by EXMs in the EPC-7.

Port	Functional group	Usage
00	DMA	Channel 0 address
01		Channel 0 count
02		Channel 1 address
03		Channel 1 count
04		Channel 2 address
05		Channel 2 count
06		Channel 3 address
07		Channel 3 count
08		Command/status
09		DMA request
0A		Command register (R)
		Single-bit DMA req mask(W)
0B		Mode
0C		Set byte pointer (R)
		Clear byte pointer (W)
0D		Temporary register (R)
		Master clear (W)
0E		Clear mode reg counter (R)
		Clear all DMA req mask(W)
0F		All DMA request mask
20	Interrupt controller 1	Port 0
21		Port 1
24	83000 Controller	Data register
26		Index register
40	Timer	Counter 0
41		Counter 1
42		Counter 2
43		Control (W)
60	Keyboard controller	Data I/O register
61	NMI status	NMI status
64	Keyboard controller	Command/status register
70	Real-time clock	RTC index reg / NMI enable
71		RTC data register
		0 seconds
		1 seconds alarm
Port	Functional group	Usage
		2 minutes

B B

		3	minutes alarm
		4	hours
		5	hours alarm
		6	day of week
		7	date of month
		8	month
		9	year
		A	status A
		B	status B
		C	status C
		D	status D
		E	RAM
		...	
		3F	RAM
81	DMA	Channel 2 page register	
82		Channel 3 page register	
83		Channel 1 page register	
87		Channel 0 page register	
89		Channel 6 page register	
8A		Channel 7 page register	
8B		Channel 5 page register	
8F		Refresh page register	
96	EXM Configuration	EXMID driver	
A0	Interrupt controller 2	Port 0	
A1		Port 1	
C0	DMA	Channel 4 address	
C2		Channel 4 count	
C4		Channel 5 address	
C6		Channel 5 count	
C8		Channel 6 address	
CA		Channel 6 count	
CC		Channel 7 address	
CE		Channel 7 count	
D0		Command/status	
D2		DMA request	
D4		Command register (R)	
		Single-bit DMA req mask(W)	
D6		Mode	
D8		Set byte pointer (R)	
		Clear byte pointer (W)	
DA		Temporary register (R)	
		Master clear (W)	
DC		Clear mode reg counter (R)	
		Clear all DMA req mask (W)	
DE		All DMA request mask	

F0	Coprocessor	Clear coprocessor busy
F1		Reset coprocessor
Port	Functional group	Usage
1F0	IDE disk controller	Data register
1F1		Error / write precompensation
1F2		Sector count
1F3		Sector number
1F4		Cylinder low register
1F5		Cylinder high register
1F6		SDH register
1F7		Status/command register
2F8	COM2 serial port	Receiver/transmitter buffer Baud rate divisor latch (LSB)
2F9		Interrupt enable register Baud rate divisor latch (MSB)
2FA		Interrupt ID register
2FB		Line control register
2FC		Modem control register
2FD		Line status register
2FE		Modem status register
340	SCSI controller	Sequence control register
341		Transfer control 0 register
342		Transfer control 1 register
343		Signal out register
344		Rate control register
345		Selection/reselection ID register
346		Latched data register
347		Data bus register
348		Count 0 register
349		Count 1 register
34A		Count 2 register
34B		Interrupt status 0 register
34C		Status 1 register
34D		Status 2 register
34E		Status 3 register
34F		Status 4 register
350		Interrupt mode 0 register
351		Interrupt mode 1 register
352		DMA control 0 register
353		DMA control 1 register
354		DMA status register
355		FIFO status register
356		Data port register
358		Burst control register
35A		Port A register
35B		Port B register
35C		Revision register
35D		Stack register
35E		Test register
Port	Functional group	Usage

B B

378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register
3F2	Floppy disk controller	Operations
3F4		Command
3F5		Data
3F7		Control, also IDE drive address reg
3F8	COM1 serial port	Receiver/transmitter buffer Baud rate divisor latch (LSB)
3F9		Interrupt enable register Baud rate divisor latch (MSB)
3FA		Interrupt ID register
3FB		Line control register
3FC		Modem control register
3FD		Line status register
3FE		Modem status register
8102	System control	Battery backed register
8104		Memory control
8130		VME A21-16 address
8132		*alias address of 8130*
8134		*alias address of 8130*
8136		*alias address of 8130*
8140	VXI registers	ID low
8141		ID high
8142		Device type low
8143		Device type high
8144		Status/control low
8145		Status/control high
8146		Slave offset low
8147		Slave offset high
8148		Protocol low
8149		Protocol high
814A		Response low
814B		Response high
814C		Message high low
814D		Message high high
814E		Message low low
814F		Message low high
8150	VXI/VME control	VME map WA31-24
8151		VME modifier
8152		VME interrupt state
8153		VME interrupt enable
8154		VME event state
8155		VME event enable
8156		TTL trigger sample
8158		MODID/Interrupter

Port	Functional group	Usage
8159		MODID upper
815A		TTL trigger drive
815B		ECL trigger
815C		ULA
815D		Module status/control
815E		Signal FIFO (lower)
815F		Signal FIFO (upper)
8161		Trigger capture
8162		Clock control
8163		External trigger control
8164		Trigger interrupt enable
8380	Non-volatile memory control	Address
8381		Address
8382		Address
8383		Flash data
8384		SRAM data

Table 20. I/O Map.

NOTES

Appendix C: Using the EPC7-AM

The EPC7-AM is a factory-installed option which bolts to the right side of the EPC-7 and occupies an additional VXI slot (3 slots total). It is designed to allow the addition of one PC add-in card for use with the EPC-7 controller. In addition, it also provides a second front-panel serial port connector (COM2).

The EPC7-AM supports all types of PC (8 bit) and PC/AT (16 bit) add-in cards except bus masters that require taking over control of the ATbus (e.g., some high performance disk controllers).

Installing a PC Add-In Card

Installation of an add-in card is simple. Follow the instructions below.

✉ MAKE SURE THAT THE INSTALLATION PROCEDURE DESCRIBED HERE IS PERFORMED IN A STATIC-FREE ENVIRONMENT.

Do not remove any modules from their anti-static bags unless you are in a static-free environment. The EPC-7 and EPC7-AM modules, like most other electronic devices, are susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

C C

First, set any jumpers or switches on your add-in card. Make sure that any selections you use for IRQ levels, base addresses, or DMA channels do not conflict with the EPC-7 or any EXMs already installed. Be especially careful about cards that are software configurable. Consult the EPC-7 and EXM module manuals if necessary. If there are conflicts, your add-in card may not be recognized by the system.

Lay the EPC-7/EPC7-AM assembly on a static-free work surface with the EPC7-AM side up and the front panel to your left as shown in Figure C-1 below. This will position the bottom of the assembly closest to you.

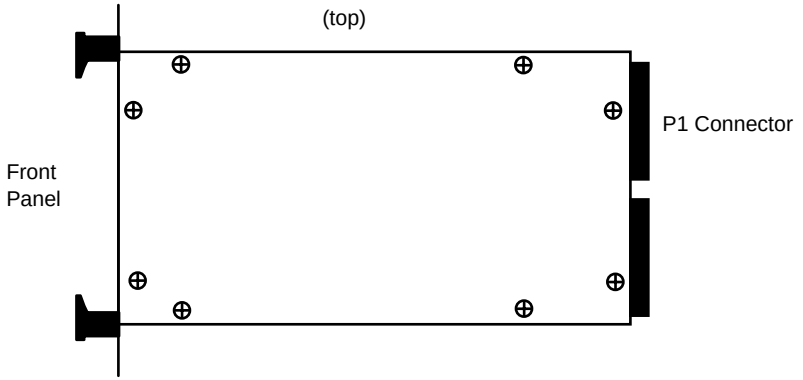

Figure C-1. EPC-7/EPC7-AM Orientation.

ÿ Remove the 8 side panel screws shown in Figure C-1 above. Set these screws aside for now. You will need them later.

ÿ If you are installing a full size add-in card (long card), you will need to temporarily remove the rear panel of the EPC7-AM. Remove the 4 screws shown in Figure C-2 below.

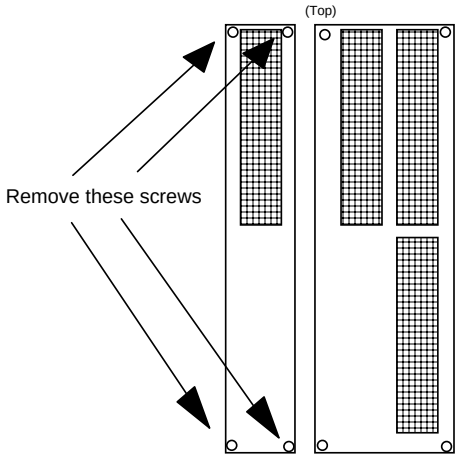

Figure C-2. EPC-7/EPC7-AM Orientation.

ÿ Loosen the front-panel thumb screw shown in Figure C-3 below. Slide the retainer clip up (toward the top of the EPC7-AM) as far as it will go.

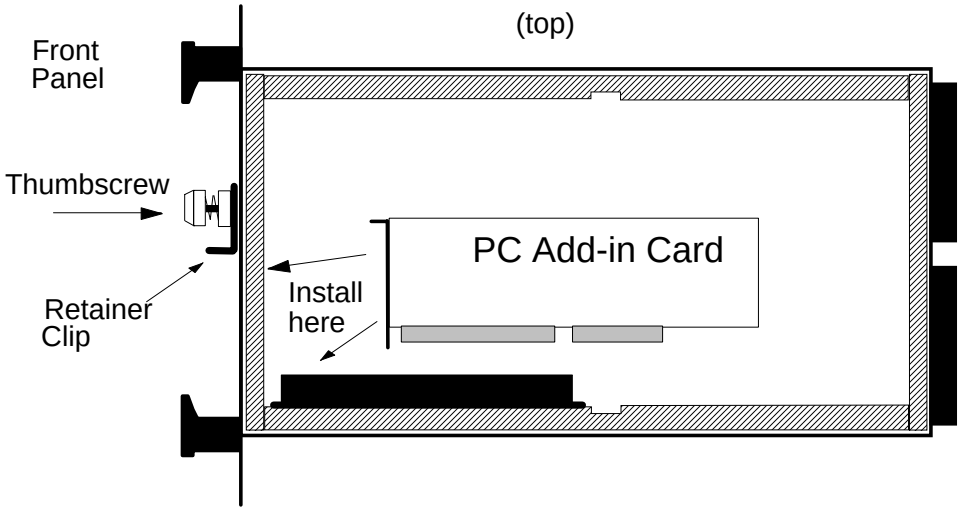

Figure C-3. Inserting the PC Add-In Card.

C C

C C

ÿ Position the add-in card inside the EPC7-AM as shown in Figure C-3 above. Slide the add-in card toward the front panel until the metal end-panel of the add-in card is past the card-edge connector. Then move the add-in card down and slide it forward again to allow the flange on the top of the metal end-plate to pass through the slot in the front of the EPC7-AM as shown in Figure C-3.

ÿ Slide the add-in card down so the care-edge inserts into the card-edge connector. Make sure that the tab on the bottom of the metal add-in card end plate seats into the retainer slot of the EPC7-AM as shown in Figure C-4 below.

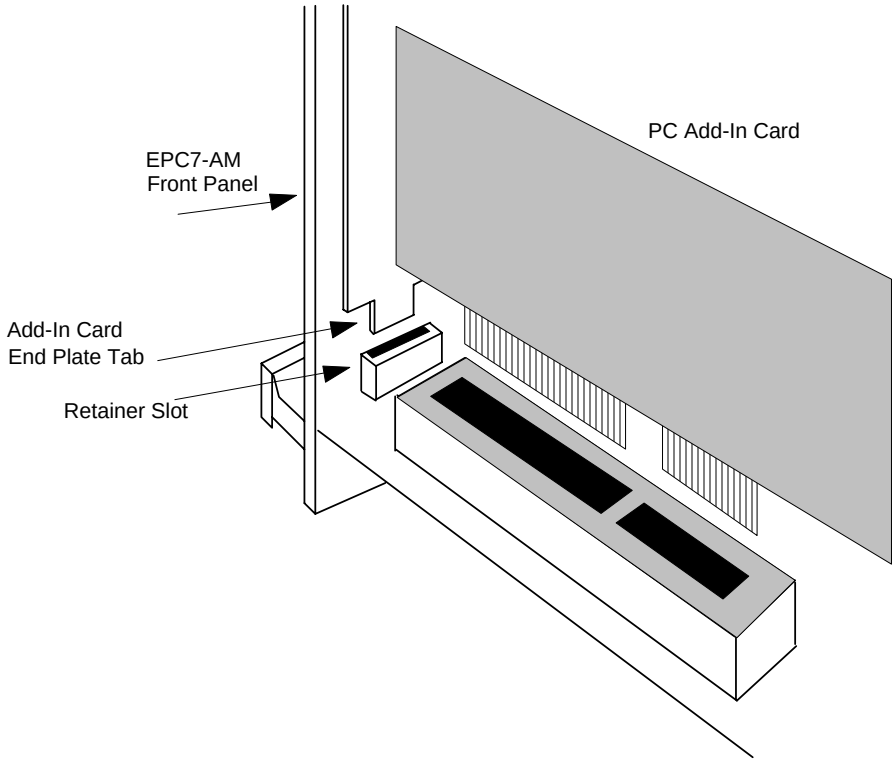

Figure C-4. Cut-Away Diagram Showing Retainer Slot.

ÿ Slide the front-panel retainer clip down until it is secure against the add-in card end plate flange. Tighten the thumb screw.

ÿ If you previously removed the rear panel of the EPC7-AM, replace it now. Make sure to align the rear edge of the add-in board so it inserts into the card guide on the rear panel and restore the four screws that attach the rear panel to the EPC7-AM.

ÿ Replace the side panel of the EPC7-AM with the 8 screws removed previously.

The add-in card is now installed and ready to use.

NOTE

There are a few full length PC add-in cards whose exceptionally large dimensions will require you to also remove the front panel of the EPC7-AM for proper installation.

To remove the front panel, start by prying off the name plates on the top and bottom handles of the EPC7-AM. This exposes two screws that hold the top and bottom handles in place. Remove both screws. Note that removing the screw on the bottom handle will cause the retainer slot on the inside of the front panel to fall off. Refer to Figure C-4, above. Next, remove the four corner screws that hold the front panel to the top and bottom rails. You can now remove the front panel itself and install the add-in card as described earlier.

Once the add-in card is in position and you have replaced the rear-panel, replace the front panel by reversing the above procedure. Note that when screwing the bottom handle back on the front panel, you will need to hold the retainer slot back in place on top of the add-in card's metal end plate.

WARNING: Any component on the add-in card that exceeds 0.50" in height will mechanically rest on the EPC7-AM internal adapter board. Though this will not cause any electrical interference, it may cause premature failure of that component due to mechanical fatigue. Most PC and PC/AT add-in cards do NOT exceed this height.

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