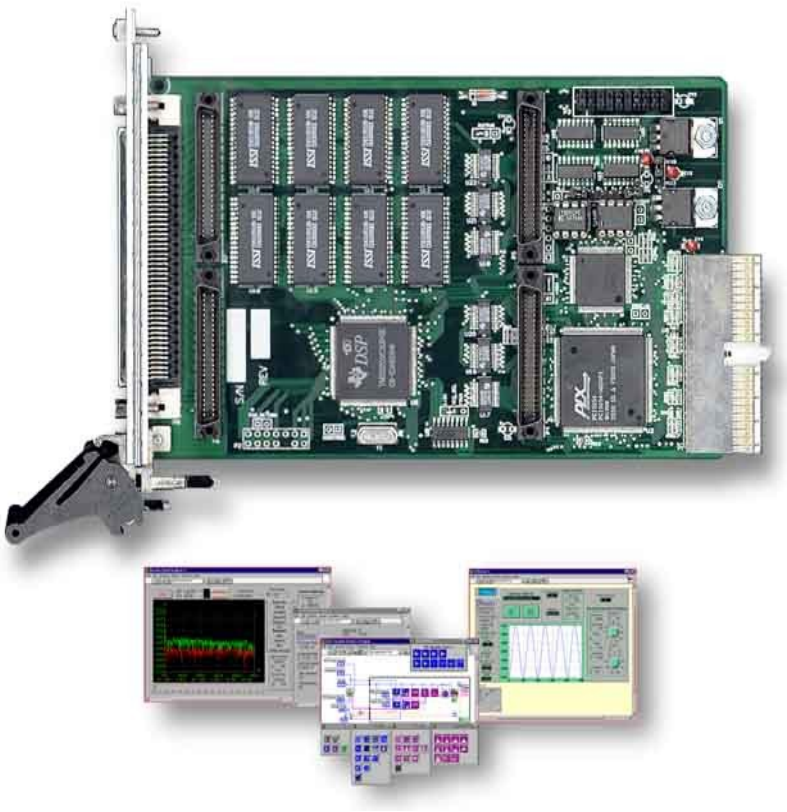
SI-C33DSP-cPCI

C33 DSP Board for cPCI/PXI Bus

Key Features

- 150 MFLOPS peak performance, 32 bit floating point precision.
- 128Kx32 words of one (1) wait state Dual Access SRAM Memory, expandable to 1Mx32 words.
- Full bi-directional cPCI/PXI initiated bus mastering, with 132MB/sec peak transfer rate.
- Memory mapped host communications port.
- Software development tools from Sheldon Instruments includes **QuVIEW**, **QuBASE** and the **SI-DDKs**; as well compatibility with separately purchased TI and third party tools.
- Win98/2000/XP and Linux drivers and sample application support.
- Expansion connectors for prototyping, analog & digital I/O daughtercards.
- JTAG port for in system development and debugging.



Introduction

The SI-C33DSP-cPCI from Sheldon Instruments is a powerful Digital Signal Processor (DSP) card for your system equipped with a cPCI/PXI bus. It is based on Texas Instruments' 150Mhz TMS320VC33, 32 bit floating point DSP, and can transform your system into an ultra high performance development system and DSP accelerator. A full line of software development tools are available from Sheldon Instruments and TI, which include compilers, assemblers, linkers, and debuggers.

Host cPCI/PXI bus to DSP Link

All communication between the host and the DSP take place by means of PLX's PCI 9054 IC. Three (3) methods may be used for data transfer between the cPCI/PXI bus and the DSP's memory: dual access mode, cPCI/PXI initiated bus mastered transfer mode with the 9054 acting as the bus master, and bus mastering with the DSP acting as the cPCI/PXI bus master.

For the dual access mode, all of the DSP's zero wait state SRAM memory is simultaneously accessible by both the cPCI/PXI bus and the DSP with the 9054 behaving as a target peripheral. The DSP's memory is directly mapped into the first target region of the 9054, which can be accessed with standard memory access calls.

Onboard control logic arbitrates the appropriate timing between the C33's primary bus, the SRAM, and the 9054's Local bus. This is accomplished by asserting the C33 HOLD signal for no more than three (3) of its own clock cycles, every time the cPCI/PXI side performs an access.

In addition to the dual access memory, large blocks of data can be transferred using cPCI/PXI bus master transfers. The first bus master transfer method involves using the 9054's DMA capabilities to access the DSP memory. The second bus master transfer method allows the DSP to act as the cPCI/PXI bus master, where it actually has direct access to the host computer's main memory! Both cPCI/PXI bus master methods may allow for the highest possible burst transfer rates to take place over the cPCI/PXI bus without host processor intervention.

Hardware Support

The SI-C33DSP-cPCI includes expansion connectors allowing for custom designs, or for attaching 'off the shelf' multifunction I/O modules from Sheldon Instruments. Sheldon Instruments offers several daughter modules for multichannel analog and digital I/O, including 4 to 64 channels of 16 bit ADCs and DACs.

Software Support

The SI-C33DSP-cPCI is available with extensive development tools from Sheldon Instruments and TI.

For quick turnkey development, Sheldon Instruments offers **QuVIEW** and **QuBASE**, which are a set of DSP-resident libraries for real time performance that greatly accelerate data acquisition, signal processing, and control applications. QuVIEW is a real time accelerator for LabVIEW, and QuBASE a real time accelerator for Visual Basic. A full range of examples and tutors are provided to demonstrate their ease of use and breadth of functionality and capabilities. QuBASE runs under Win98/2000/XP, while QuVIEW also runs under Linux.

Typical benchmarks for a 150Mhz C33 processor include the computation of a 1024 point Radix-2 complex FFT at 400us.

When purchased as a DSP evaluation board, Sheldon Instruments also includes free sample DSP and Win98/2000/XP or Linux device driver source code to accompany TI's development environment. The DSP source code illustrates full communication modes, and the Win98/2000/XP or Linux device driver source code includes the complete **SI-DDK**, along with COFF file loader utilities.

Technical Specifications

Processor for SI-C33DSP-cPCI:

- TMS320VC33 150Mhz DSP.
- Dual DMA channel.

Memory Options:

- "-128" option:
    - 128K x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.
- "-512" option:
    - 512K x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.
- "-1M" option:
    - 1M x 32 bit words one (1) wait state dual access SRAM on C33's primary bus.

Interface to Host:

- PCI initiated bus master transfer speeds:
    - Up to 132Mbyte/sec bursts with block sizes of eight (8) 32 bit words.
    - Up to 12Mbyte/sec sustained transfers of any block size, using DMA.
- Four 32 bit, bi-directional communications modes between TMS320VC33 primary bus and the 9054:
    - Target/Dual access mode.
    - Block Mode DMA Bus Master mode, using the 9054 as the cPCI/PXI bus master.
    - cPCI/PXI Initiated/Local Master with DSP I/O, using the DSP as the cPCI/PXI bus master.
    - cPCI/PXI Initiated/Local Master with DSP DMA, using the DSP's DMA as the cPCI/PXI bus master.
- The 9054's internal registers are mapped into the C33's primary bus, address space starting at 0xFF0000.
- INT0 used by C33 for basic communication and DMA transfer initialization; INT2 and INT3 available on expansion connectors.

Peripheral Expansion:

- One external 100 pin half pitch DSUB connector (Hippi style), and four 50 pin half pitch DSUB plug connectors (I-Pack style):
    - First 50 pin DSUB pair for interfacing custom/expansion daughter board to the DSP's bus.
    - Second 50 pin DSUB pair for interfacing external user defined signals to custom/expansion daughter board. Linked only to externally accessible 100 pin half pitch DSUB connector, J1.
    - External 100 pin, half pitch (0.050"), Series III DSUB connector, designated J1, for interfacing external user defined signals to P1. AMP part 787169-9, 787170-9, or 787362-9.
- Second DSUB connector pairs decode 8Kx32 words, mapped into the C33's primary bus, address space ranging from 0xFE0000 to 0xFE1FFF.
- Second DSUB connector pairs contain the following C33 signals:
    - Address: A12-A0.
    - Data: D31-D0
    - Control: R/W, STRB, INT2 & INT3, IACK, RDY, H1 & H3.
    - I/O lines: Serial port 0, XF0 & XF1, TMCK0 & TMCK1.
    - Host +3.3Vdc, +5Vdc, -5Vdc, +12Vdc, -12Vdc and GND.
- One 14 pin header for JTAG port
- One 2x10 pin header for direct access to DSP's serial bus

Software:

- Win98/2000/XP and Linux driver support.
- Extensive QuVIEW DSP-resident libraries for LabVIEW, including examples for real time acquisition, signal processing, and control.
- Extensive QuBASE DSP-resident libraries for Visual Basic, including examples for real time acquisition, signal processing, and control.
- Sample code for COFF loaders, PC <-> DSP communications source code and SI-DDK.
- Compatible with separately purchased TI debuggers, C/C++ compilers, assemblers and linkers.

Physical Dimensions & Electrical Requirements:

- 3U size cPCI/PXI-bus card measuring 160mm(L) x 100mm(H).
- 0.31lbs or 140 grams.
- Supply Voltages: 3.3V for all circuitry, and 5V for expansion bus buffers; 3V expansion buffers may be placed on special request. +/-12V supplies passed on to expansion connector and not used by on-board circuitry.
- 1.5 watts typical (3.3V @ 0.5A) with 128Kx32 words SRAM .

Ordering Information:

- SI-C33DSP-cPCI:
  - SI-C33DSP-cPCI-128.
  - SI-C33DSP-cPCI-512.
  - SI-C33DSP-cPCI-1M.

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