ICS-110BL 24-BIT DATA ACQUISITION BOARD

No. 24, Rev. D Interactive Circuits & Systems Ltd.

INTRODUCTION

The ICS-110BL is designed to provide a complete data acquisition solution in a single 6U VMEbus slot. The ICS-110BL includes 32 24-bit, 100 kHz/channel sigma-delta ADCs, 64K FIFO buffer and VME, VSB and FPDP interfaces. It can accept an optional signal conditioning daughter card which offers 2-pole anti-alias filtering consistent with the anti-aliasing requirements of sigma-delta ADCs, programmable gain of up to 31 dB in 0.5 dB steps, and internal test signal generation and injection capabilities. Designed for applications in sonar, digital audio, vibration analysis, and test and measurement, the ICS-110BL board is a superior replacement for the company's highly popular ICS-110A board.

The ICS-110BL combines the ultimate in analog and digital technologies to offer unparalleled features and performance. The very high density of the ICS-110BL board allows users to implement a 576-channel signal conditioning and data acquisition system (with simultaneous sampling at high sample rates) in a single 20-slot VMEbus enclosure (see Figure 2). The ICS-110BL base board offers:

- up to 32 differential input channels;
- 24-bit sigma-delta A/D converters;
- simultaneous sampling at rates up to 100 kHz/ch.;
- optional 16-bit mode of operation;
- software selectable high pass filter for low frequency rejection;
- external or internal clock and trigger;
- internal clock programmable in steps of less than 20 Hz at output frequency;
- greater than 105 dB signal-to noise ratio (including harmonic distortion and crosstalk);

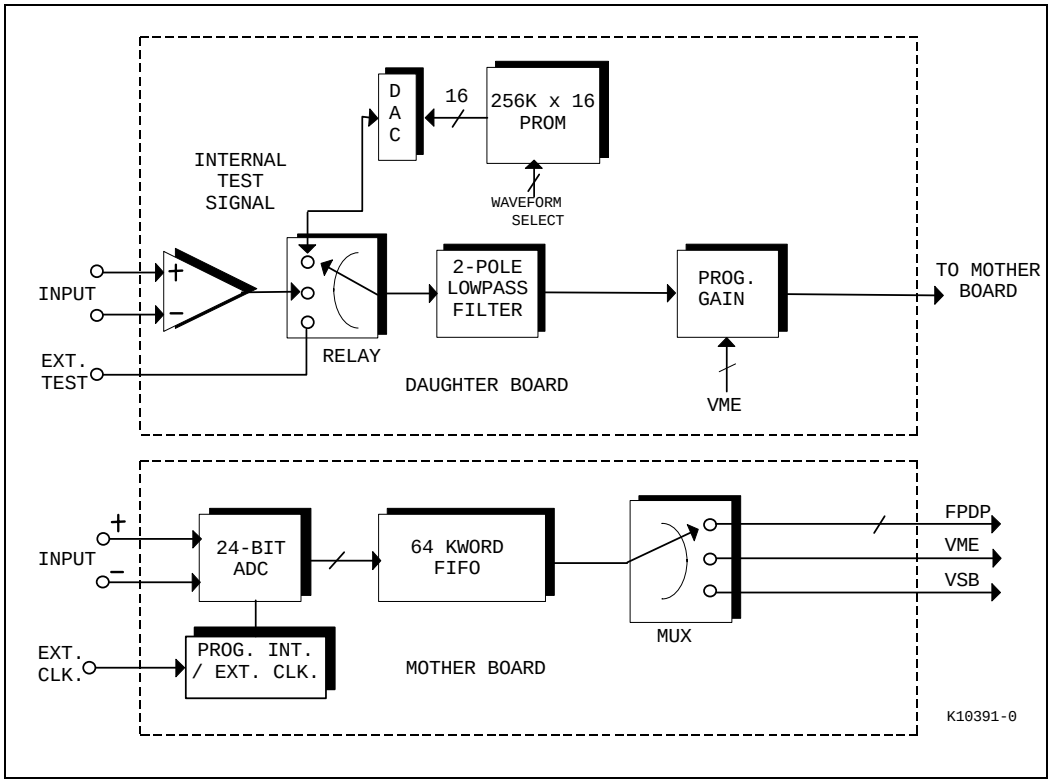

Figure 1 - Simplified single-channel block diagram of the ICS-110BL with daughter board (model ICS-110BL)

- 64 Kword on-board storage;
- VME, VSB and FPDP interfaces for ADC data;
- front-panel sync bus for sample synchronization and Front Panel Data Port (FPDP) bussing of up to 32 boards.

The ICS-110BL, which contains the optional daughter card, features:

- up to 32 differential inputs;
- high input impedance;
- 2-pole low pass anti-alias filters;
- -95.0 dB to 31.5 dB programmable gain in steps of 0.5 dB;
- internal or external test signal injection to all 32 channels by means of relays;
- internal test signal stored in PROM (up to 8 16-bit signals of 32 K samples each).

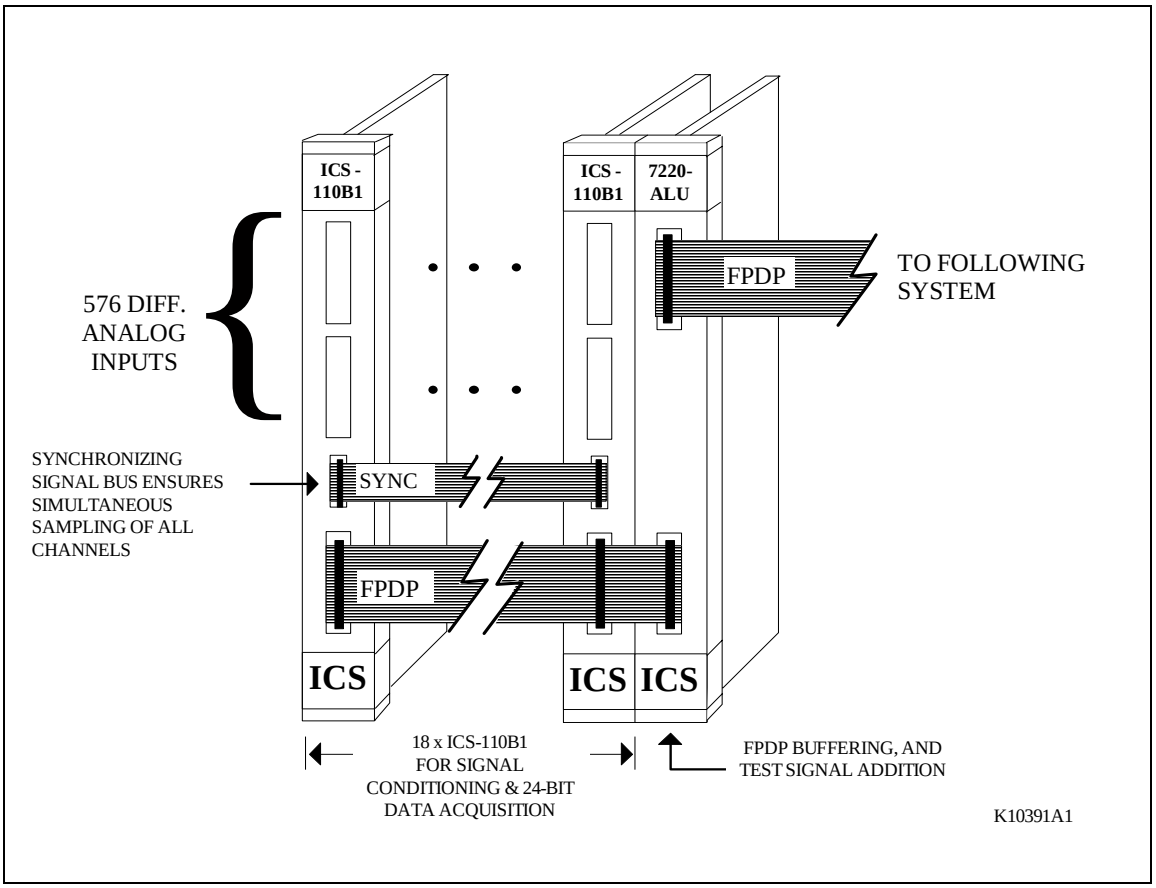

Figure 2 - A 576 channel signal conditioning and data acquisition system can now be included in a 20-slot VME enclosure using ICS-110BL boards

SPECIFICATIONS

ICS-110BL Mother Board

No. of Diff. Analog Inputs:	8, 16 or 32
Input Impedance:	10 kOhm
Full Scale Input:	2.0 V pp differential*
Max. Input Signal BW:	40 kHz
Input Sample Rate:	128 X Output Rate for BW < 22 kHz 64 X Output Rate for BW > 22 kHz
Output Rate (Effective Sample Rate):	Max. 100 kHz/Ch. Min. 2 kHz/Ch
Internal Sample Clock:	Programmable in steps of 20 Hz (at output frequency)
Dynamic Range	> 110 dB in 128x oversampling mode > 105 dB in 64x oversampling mode
Total Harmonic Distortion:	< -105 dB
Crosstalk:	< -105 dB
On-Board Storage:	64 K Words
Output Word length:	32 bits packed for 2 channels or 24 bits for 1 channel on both VME or VSB 24 bits only on FPDP
VMEbus Interface:	A32/24/16 D32 BLT Slave Vectored Interrupts
VSBbus Interface:	A32 D32 BLT Slave Polled Interrupts
FPDP Interface:	Refer to ICS Input Technical Note No. 15 Programmable Word Rate, up to 20Mwords/s
Power:	6.0 Amps @ +5 V 0.42 Amps @ +12 V 0.25 Amps @ -12 V
Operating Temp:	0 to +50 Deg. C
Storage Temp:	-40 to +85 Deg. C
Humidity:	#95% Rel. Humidity, non-condensing
Board Size:	6U VMEbus Standard

ICS-110BL Daughter Card

No. Of Diff Inputs:	8, 16 or 32
Input Impedance:	>1 M Ohm (with ±5 V max. input) >100 K Ohm (with ±25 V max. input)
Max. Input Level:	±3.75V differential standard option (Contact factory for other options)
Lowpass Filter:	2 - Pole Butterworth with a cut-off frequency of 75 kHz for a flat response up to 40kHz (Contact Factory for Other Options)
Gain:	-95.0 dB to +31.5 dB in steps of 0.5 dB
Internal Test Signal:	8 16-bit preprogrammed waveforms in a 256K X 16 PROM
Dynamic Range:	>85 dB at 0 dB Gain and 2 Vpp Diff. Input
Power:	0.34 Amps @ +5 V 0.29 Amps @ + 12 V 0.20 Amps @ -12 V
Environmental:	Same as ICS-110BL Mother Board

* 2.0Vpp on each wire of differential pair.

Specifications are subject to change without notice

GENERAL DESCRIPTION

MOTHER BOARD

Figure 3 shows a simplified block diagram of the ICS-110BL baseboard. The board includes up to 32 separate Sigma-Delta ADCs to simultaneously digitize all channels at rates up to 100 KHz/ch. All inputs are differential to suppress common mode noise. The serial output from each ADC is converted to a 24-bit word before being stored in a FIFO for read-out.

The ICS-110BL uses AKM's AK5393 24-bit sigma-delta ADC converters. Each ADC converter samples the analog input signal at 64 or 128 times the output rate (Fo). For Fo < 50 kHz, 128 x oversampling mode is recommended. For Fo > 50 kHz only 64 x oversampling mode can be used. The sampling mode is set via the control register, which alters the decimation ratio of the digital filter. The maximum sample output frequency is 100 kHz. The AK5393 also includes a digital highpass filter after the decimator to remove low-frequency noise. The -3dB point is at 1.8 X Fs/48. In other words, the -3dB point of the highpass filter's response is at 3.6 Hz for Fs=96 kHz. The high pass filter can be disabled using a bit in the control register. The standard group delay through the AK5393 FIR low pass filters is 34/Fo (all filters are linear phase). The group delay can be reduced to 10/Fo if the minimum phase filter option is selected. All of the converter's programmable features are available to the user.

At the output, data is read as 32-bit words. Data from consecutive odd and even channels may be truncated to 16-bit resolution and packed together to form a 32-bit word for faster read-out from the VMEbus or VSB. Data may also be read-out in unpacked format as 24-bit words. The FPDP output, however, only supports unpacked format. A VMEbus or VSB interrupt can be generated at FIFO half-full to facilitate real-time operation.

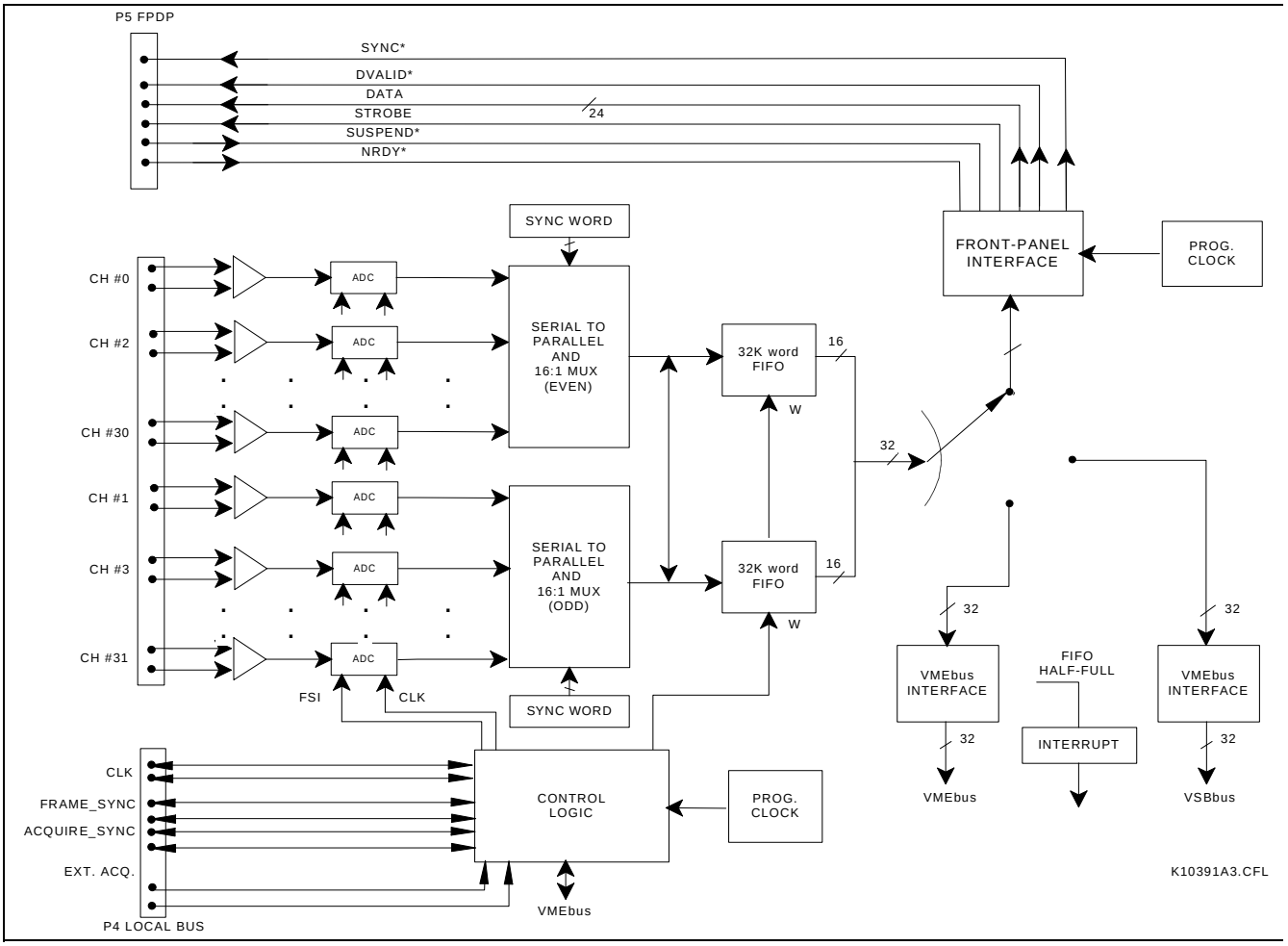

Figure 3 - ICS-110BL Mother Board Block Diagram

The ICS-110BL can use either an external clock or the board's internal clock as the sampling clock. The required clock frequency is 256 times the output data rate. The internal clock can be programmed to produce a sampling rate with excellent accuracy (usually to within 40ppm) by writing the appropriate clock frequency word to the board's PROGRAM_CLOCK register. The minimum Fo is 2 kHz. The board includes a programmable decimator, which simply rejects output samples to reduce Fo by a factor of up to 16. Note, however, that the antialising characteristics of the sigma-delta converters are lost when this feature is selected. Hence, this mode should only be selected when using a Fo of less than 2kHz.

The acquisition period can be controlled either from the VMEbus (through software control), or by applying an external signal conforming to differential TTL signal levels to the EXTERNAL_ACQUIRE input. A high level signal causes acquisition to occur, while a low level signal causes acquisition to stop. Acquisition is automatically synchronized so that a full frame of data is always written to the FIFO at the beginning or end of an acquisition cycle.

The ICS-110BL includes a very powerful FPDP interface, which allows up to 32 ICS-110BL boards to be bussed. To synchronize multiple ICS-110BL boards, one board must be configured as "master" in order to supply synchronization signals to the other slave boards. These signals are available at the front-panel P4 local bus connector.

DAUGHTER CARD

The ICS-110BL base board includes a provision for a daughter card for signal conditioning. Figure 4 provides a simplified block diagram of the daughter card version (ICS-110BL), which includes the following:

- A 2-pole low-pass filter with a fixed cut-off frequency of 75 kHz in order to ensure a flat passband response extending up to 40 kHz. Typically, no more than a 2-pole filter is required for anti-aliasing because of the high input sampling rate inherent in a sigma-delta ADC converter. An alternate filter cut-off frequency may be offered. Contact factory for details.

- A programmable attenuation/gain stage which offers -95.0 dB to +31.5 dB attenuation/gain in steps of 0.5 dB.

- An internal or external test signal injection capability that allows injection of a test signal to all 32-signal conditioning and ADC stages. The test signal input is signal is single-ended. The internal test signal is generated from a preprogrammed PROM, which can hold as many as 8 waveforms up to 32K samples each. The PROM is operated in a loop address mode in order to generate a periodic signal. The standard option for test signals include: single-tone; dual-tone; pseudo-noise; etc. A 16-bit filtered delta-sigma DAC is used to produce an analog signal. The switching between the actual input signals, external test signal and internal test signal is done under software control.

Other signal conditioning daughter cards are being planned for different applications. Please contact the factory for details.

DETAILED DESCRIPTION

DAUGHTER BOARD

Figure 4 shows a simplified block diagram of the signal conditioning daughter card for the ICS-110BL board. It includes, for each channel, a differential receiver, which offers high input impedance. A resistive divider stage is included at the input to allow an over voltage capability. The input impedance is dependent on the maximum voltage input requirement.

The signal conditioning circuit also includes a 2-pole low pass filter with a fixed cut-off frequency and a gain stage which offers programmable gain from -95.0 dB to 31.5 dB in steps of 0.5 dB.

For off-line test, an internal or an external test signal can be injected into the signal path following the differential receiver stage. The internal test signal is factory programmed in to a 256K x 16 EPROM. The user can select one of any 8 pre-stored signals. A 16-bit delta-sigma DAC is used for digital-to-analog conversion. The typical dynamic range is around 90 dB. Note that high-reliability electro-mechanical relays are used to switch between internal/external test signals or actual signals. All channels receive the same test signals.

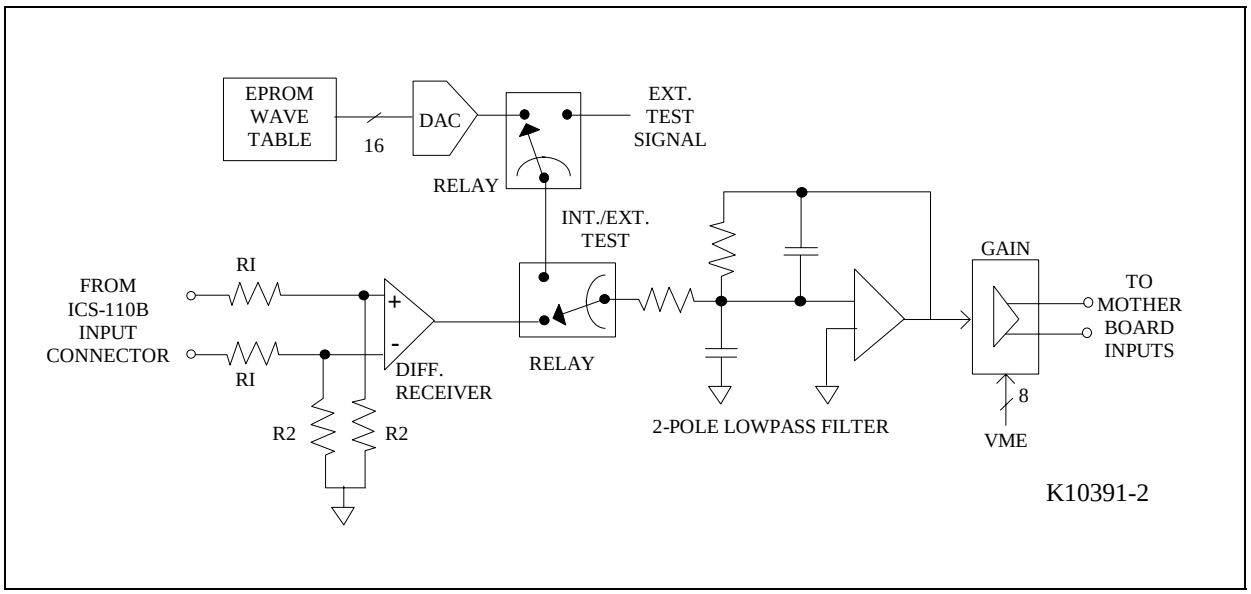

Figure 4 - Signal Conditioning Daughter Card (Single Channel Shown)

MOTHER BOARD

Sigma-Delta Analog Conversion

The operation of a Sigma-Delta ADC differs significantly from traditional ADCs. A simple 1-bit analog-to-digital conversion is performed at a very high rate. The total quantization noise energy remains constant, but by spreading it over a wider spectrum, the amount in the frequency band of interest is reduced. The noise in the passband is further reduced by filtering (noise shaping). The oversampled signal is then lowpass filtered to remove the out-of-band quantization noise. This is achieved using two digital filters: a decimating comb filter and an FIR low-pass filter/decimator. The resultant output spectrum is equivalent to a traditional ADC.

The AK5393 uses a 7th order tri-level delta-sigma modulator to sample the analog input signal at either 128 or 64 times the output sample rate of the device. The result of such high rate sampling of the input signal is that the Nyquist frequency is moved to at least 6 octaves (for 64 times oversampling) or 7 octaves (for 128 times oversampling) away from the highest signal frequency. The anti-aliasing requirement is, therefore, drastically reduced.

Since the input differential amplifier for each channel of the ICS-110BL board has a finite bandwidth, no more than a 2-pole filter is required for anti-aliasing. The signal conditioning daughter card of the ICS-110BL board includes a filter of this type.

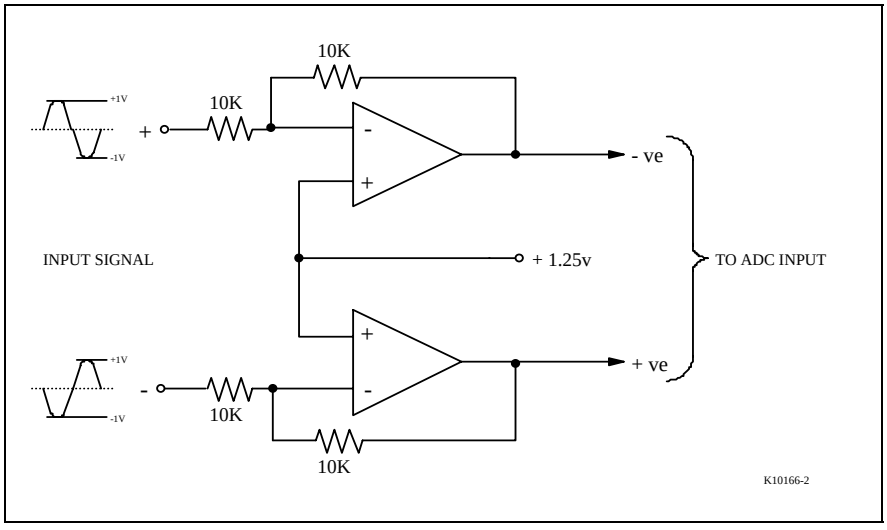

Figure 5 - ICS-110BL Analog Input Configuration

Input Section

The ICS-110BL board accepts true differential input signals; peak amplitudes of ± 1.0V on each input, as shown in Figure 5, produce a full-scale output. The input impedance is 10K ohm. The maximum input signal bandwidth is 40 kHz.

For best performance, differential input signals are recommended. If, however, single-ended inputs must be used, the -ve input terminals can be tied to a common analog ground, preferably the ground of the source. The input signal is applied to the +ve terminal. The full-scale swing of the input signal should not exceed ± 1.0V. Thus, for single ended input, there is a 6 dB loss in dynamic range.

Dynamic Range

The ICS-110BL typically offers 110 dB S/N ratios in the 128 times oversampling mode. The S/N ratio is approximately 105 dB in the 64 times oversampling mode. The total harmonic distortion is typically -105 dB. A typical 1024-point FFT plot of the ADC output is shown in Figure 6(a). The input is a synthesized single tone (differential) and the output rate is 100 kHz/channel. The crosstalk performance of a typical channel (input shorted) while all other channels are driven by a 20 kHz tone is illustrated in Figure 6(b). Note that all spurious components lie below -110 dB with respect to the ADC full-scale output.

The ICS-110BL offers excellent gain and phase matching across channels. Since the Sigma-Delta converters employ minimal analog technologies, such performance is expected.
In the design of the ICS-110BL board, extreme care has been
Taken in the generation of sampling clocks in order to assure precise simultaneous sampling on every card, and across cards in a multi-board system.

The frequency response is flat over the entire signal bandwidth (45% of the output rate).

Sampling Clock

The ICS-110BL board can be configured (by programming the control register) for internal or external sampling. The external CLOCK input is TTL differential. A single-ended TTL clock signal can also be used provided that the high logic level is above 3.5 volts. This CLOCK input frequency must be 256 times the desired output.

As mentioned above, the sampling clock can also be sourced from an internal programmable clock oscillator, which has a resolution of less than 20 Hz at the sample output frequency.

The internal clock (after conversion to differential TTL signals) is available at the P4 front-panel connector pins in order to supply clock signals to other ICS-110B boards for synchronous operation. The board generating the clock signal (master board) requires appropriate jumper settings in order to route the clock signals back to the P4 connector. All slave ICS-110BL boards must be configured for external clock. Thus all boards including the master see identical propagation delays for the clock signal, regardless of whether it is generated by an ICS-110BL board or applied from an external source. The maximum clock frequency is 25.6 MHz and the minimum clock frequency is 512 kHz.

Output Decimation

The output rate can be reduced using decimation. At the output, samples are automatically discarded, which has the effect of lowering the effective sampling rate. The decimation factor can be as high as 16.

The user is cautioned that decimating the output requires anti-aliasing (similar to using a conventional ADC) in order to bandlimit the input signal to the Nyquist frequency, which is equal to half the final output rate. Thus, output decimation is only recommended for reducing the output rate below 2 kHz.

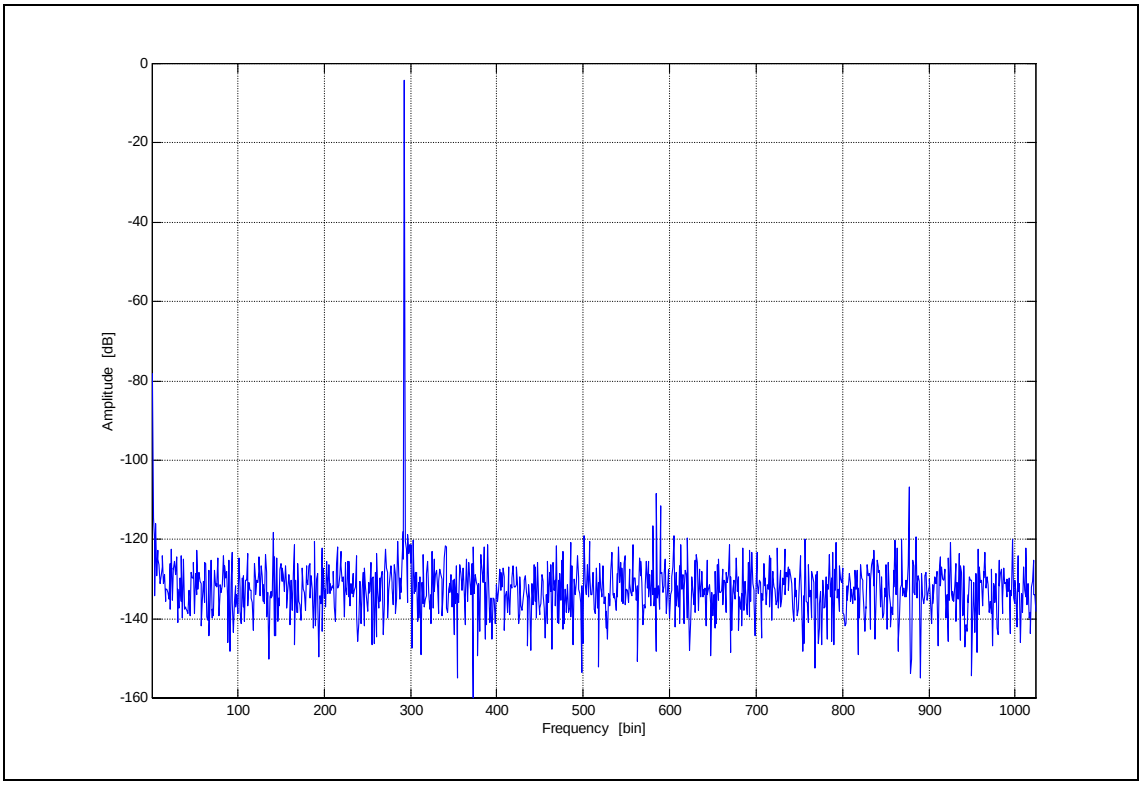

Figure 6(a) - 2048-point FFT in 24-bit mode at 100 kHz

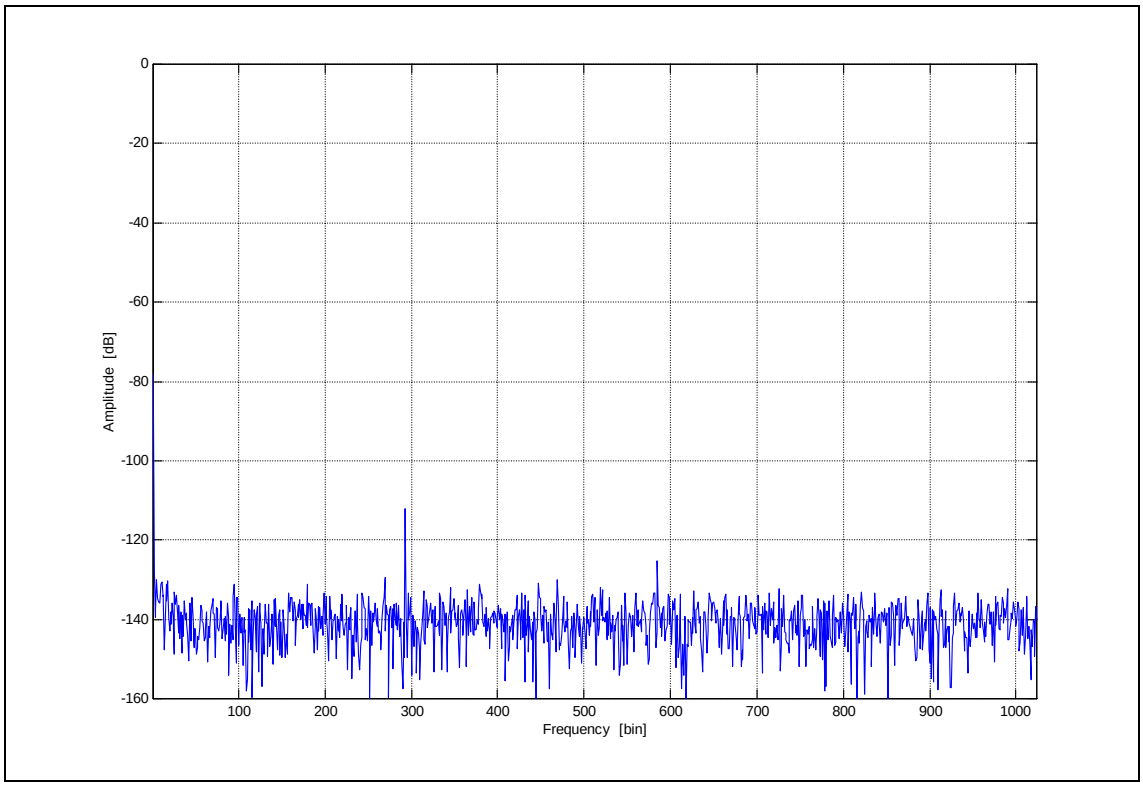

Figure 6(b) - Crosstalk Performance with 20 kHz Tone on all Other Channels

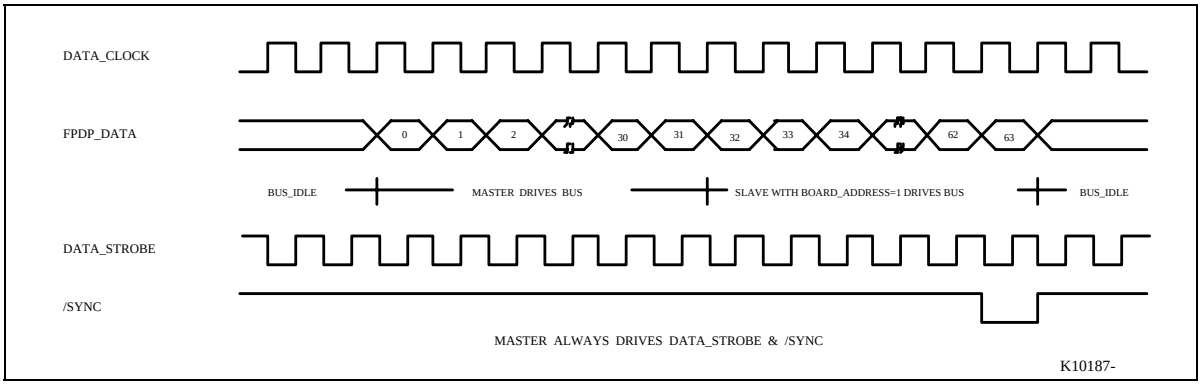

Figure 7 - FPDP Timing with Multiple Boards

Acquisition Trigger

The triggering of acquisition can be done either internally, by writing to the control register, or externally, by applying a signal to the EXTERNAL_ACQUIRE input. In either case, the effect is to start and stop acquisition by inhibiting FIFO writes; the ADCs are always converting data. The operation is frame-oriented: acquisition can only be started at the beginning of a frame and stopped at the end of a frame; a frame is defined as a set of sampled data for all selected channels for one sample instant. The number of channels included in the frame is programmable, but always starts from channel 1 and runs consecutively up to the number of channels selected. Only even numbers of channels may be selected.

For external control of acquisition start/stop, the differential EXTERNAL_ACQUIRE input must be used. A TTL high level starts acquisition and the acquisition stops when the signal is dropped to a TTL low level. Bringing the signal back to a TTL high level can restart the acquisition. Here again, a single-ended TTL signal can be used provided the high logic level is above 3.5 volts.

SYNC Word

When reading data from the 32-bit VMEbus or VSB interface, a user-programmable 32-bit sync word can be used to maintain synchronization. This optional SYNC_WORD
is automatically written to the ADC_DATA FIFO at the beginning of every frame. The SYNC_WORD option is not available on the front panel data port.

Front Panel Interface

The ICS-110BL includes a Front Panel Data Port (FPDP) for high-speed data transfer. The FPDP protocol for data transfer is supported by all ICS products, including the ICS-2200 DSP board, the ICS-7220 General Purpose I/O board, and the ICS-115 Analog Output board. An 80-pin connector (KEL 8831-080-170L) is provided for the FPDP. Refer to INPUT Technical Note No.15 for more details.

The ICS-110BL FPDP may be bussed between multiple ICS-110BL boards for systems requiring more than 32 channels of analog input. The first board of a cluster must be configured as the master, by means of wire links on the board. The master generates the FPDP Strobe, Data Valid and Sync signals and terminates various bus signals. It also generates signals on the P4 local bus, which control the timing for the slave boards so that each board drives its data onto the bus in the correct time period. This feature, combined with the multiple board synchronization capability of the ICS-110BL described elsewhere in this note, allows the user to construct large data acquisition systems of up to 1,024 channels with simultaneous sampling across all channels and a single FPDP cable passing data to one or more FPDP receive interfaces.

Figure 7 illustrates the timing relationship of the FPDP data and control signals for a 2 board 64-channel system. The FPDP Data Strobe (clock) rate is software programmable, with a maximum frequency of 20 MHz. Two types of Data Strobe signal are available: the TTL level STROB and the positive-logic ECL differential clocks (PSTROBE+ & PSTROBE-). The latter signals support longer cable lengths and higher speed operation, and provide better noise immunity. The ICS-110BL supports only the unpacked 24-bit data width on the FPDP port.

The Front Panel Data Port operates using two FIFO memories in a swing buffer configuration, as shown in Figure 8. During one frame, data is converted and written to one FIFO memory, while data is being read from the other over the FPDP. At the end of the frame, the two banks switch. Before any new ADC data is written to the swapped FIFO memory, it is automatically reset to ensure channel synchronization. In the unlikely event that the synchronization is lost, the scheme ensures that it is recovered in the next frame.

By programming the FPDP_BLOCK_COUNT register, the user can set the bank switch to occur after storing a user-programmable number of frames.

VMEbus Interface

The ICS-110BL is supported by a Slave A32/D32 VMEbus interface. The VMEbus interface supports D32 block transfers and vectored interrupts. Data rates up to 32 MBytes/sec are achievable.

Although data is always accessed using 32-bit data transfers, channel data can be organized as two channels per transfer (packed format) or one channel per transfer (unpacked format). In packed format, the data is truncated to 16 bits and ordered so that channel N is in the upper 16 bits, and channel N+1 is in the lower 16 bits of the 32-bit data word. In unpacked format, the channel data is located in the upper 24 bits of the 32-bit data word; the lower 8 bits are forced to zero.

VSB Interface

The ICS-110BL also includes a Slave A32/D32 VSB interface. The VSB interface supports block transfers, as well as polled interrupts. Data rates up to 40 MBytes/sec are achievable. Data organization is as discussed in the VMEbus Interface section.

Multiple-Board Synchronization

An important design feature of the ICS-110BL card is its ability to be integrated into a multi-board system in perfect synchronism using no additional hardware and no additional design effort. This section discusses in some detail the P4 Local Bus signals used to achieve synchronism in a multi-board system. The interface requires only the bussing of the master ICS-110BL P4 Local Bus connector to one or more slave cards, and the initialization of a few registers on the master.

To ensure sampling synchronization from board to board in a multiple board configuration, three synchronization signals are driven by the master ICS-110BL and decoded by all boards across the P4 Local Bus connector. To keep sampling skew to a minimum, all SYNC signals are generated and then received locally by the master, so that the master sees the same gate delays and decoding logic as seen by the slave cards. In effect, the master is its own slave.

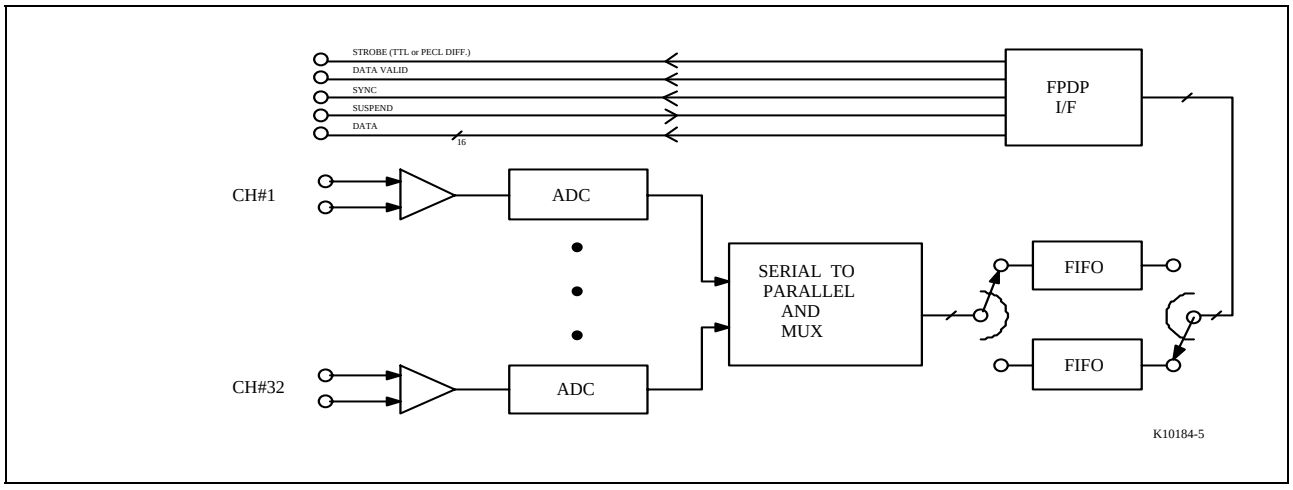

Figure 8 - ICS-110BL FPDP Configuration

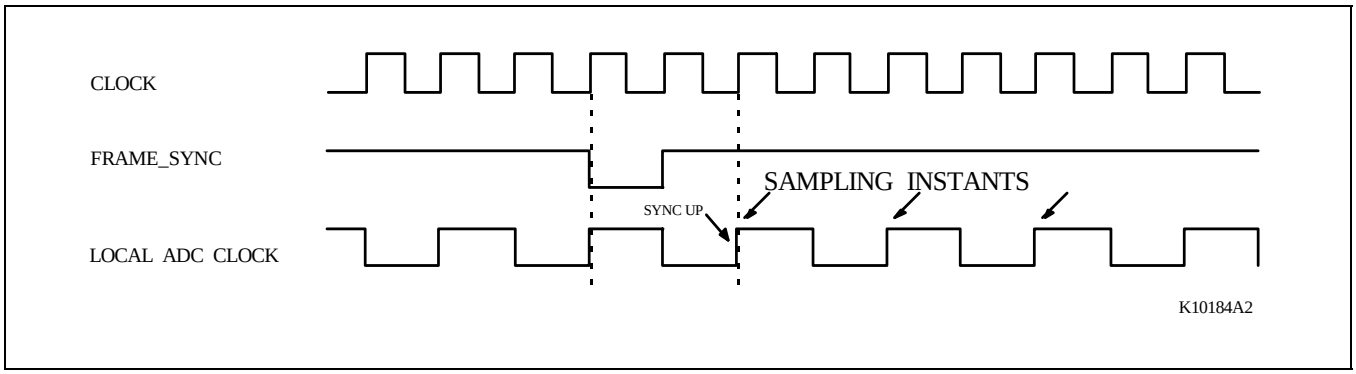

Figure 9 - Master/Slave CLOCK Phase Synchronization

FRAME_SYNC

The FRAME_SYNC signal is used to synchronize all boards with respect to the sampling clock. This signal is received.
By each slave board and used to re-synchronize the converters at the next rising edge of the oversampling clock, as shown in Figure 9

ACQUIRE_SYNC

The ICS-110BL is capable of decimating the Sigma-Delta output by a user-defined number of frames. The ACQUIRE_SYNC signal simply ensures that both the master and its slaves decimate the same frames by informing the slaves who converted data frame is to be stored to the ADC_DATA FIFO. Decimated frames are simply rejected and not written to the ADC_DATA FIFO.

Memory Map

The ICS-110BL memory map is shown in Figures 10, 11 and 12. Figure 10 shows a summary of the map, while Figures 11 and 12 show the bit allocation within registers. The control register allows the user to configure the following operating parameters:

- Acquisition start and stop control
- Master/slave (multiple board) selection
- Acquisition source (internal/external)
- Output mode (VMEbus, VSB, FPDP)
- Sync word enable/disable
- Clock source (internal/external)
- VSB interrupt enable/disable
- VMEbus interrupt enable/disable

Register Descriptions

The NUM_CHANS register must be programmed to specify the number of channels to be used on the board. The NUM_CHANS_FPDP register allows the user to select the total number of channels when using the FPDP for output with multiple ICS-110BL boards; it only needs to be programmed on the master board. The number of channels in either case must be an even number, and, in a multiple board configuration, all boards except the last must be 32-channel boards and must have a full complement of channels selected.

For example, an 80-channel system would consist of three boards defined as follows:

Master: NUM_CHANS=31 (32 channels)
NUM_CHANS_FPDP=79 (80 channels)

Middle Slave: NUM_CHANS=31 (32 channels)

End Slave: NUM_CHANS=15 (16 channels)

The maximum number of channels in a multiple board system when using the front panel data port is limited to 1,024, i.e. 32 boards (NUM_CHANS_FPDP=1023).

The DECIMATION register allows the user to specify the decimation factor in the range 1 to 16. The FPDP ADDRESS register specifies the board address in a multiple board system when using FPDP.

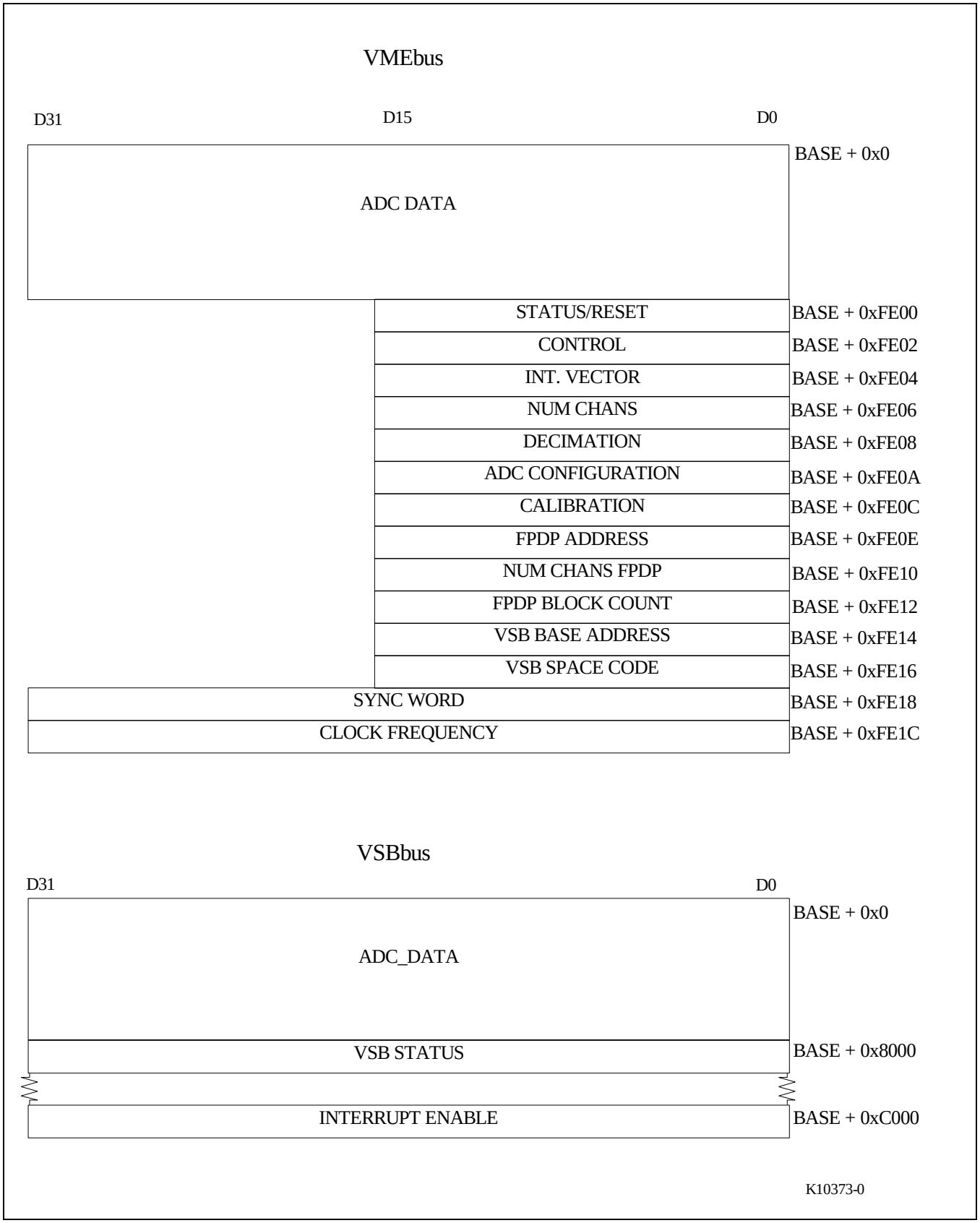

Figure 10 - ICS-110BL Memory Map

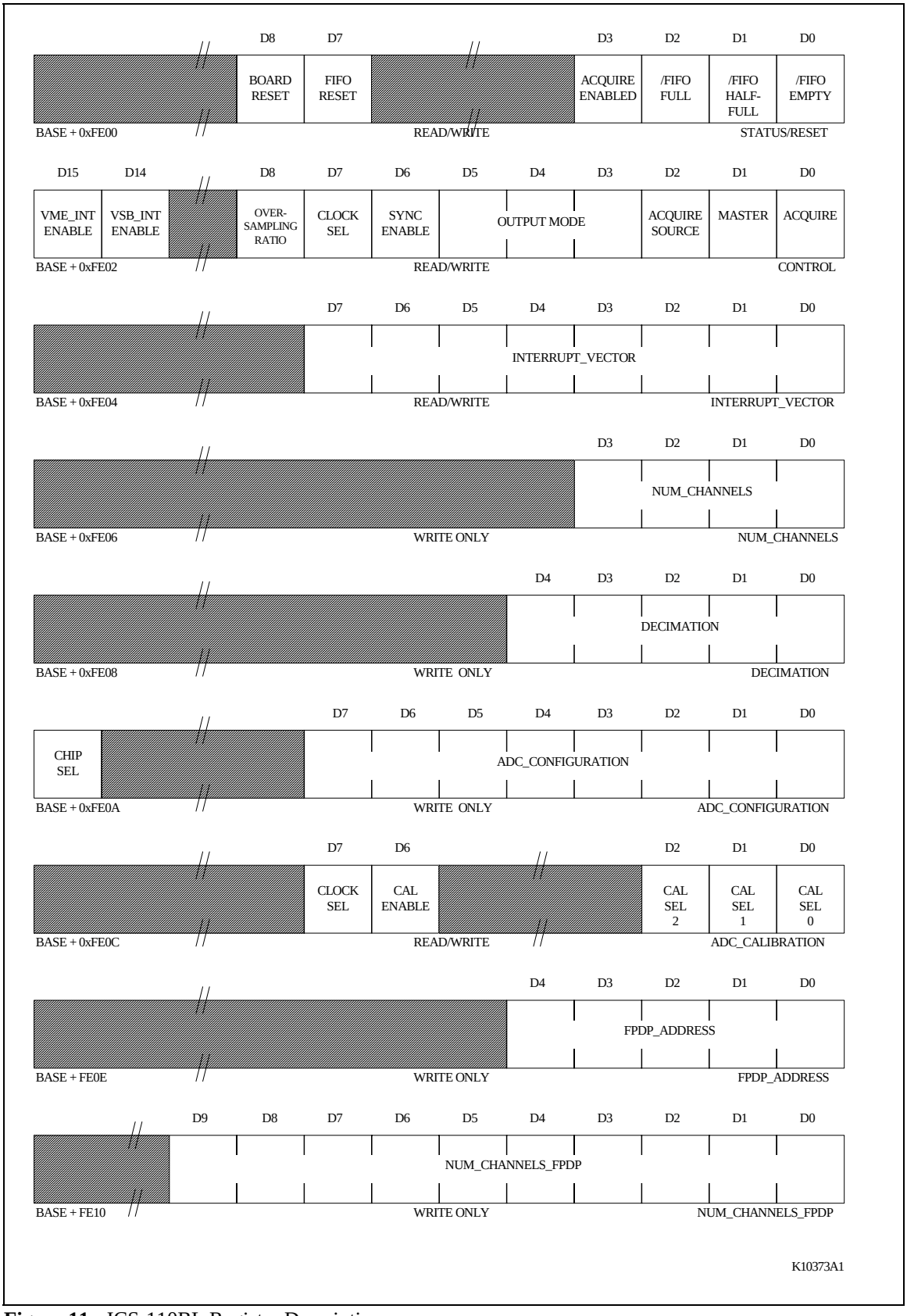

Figure 11 - ICS-110BL Register Description

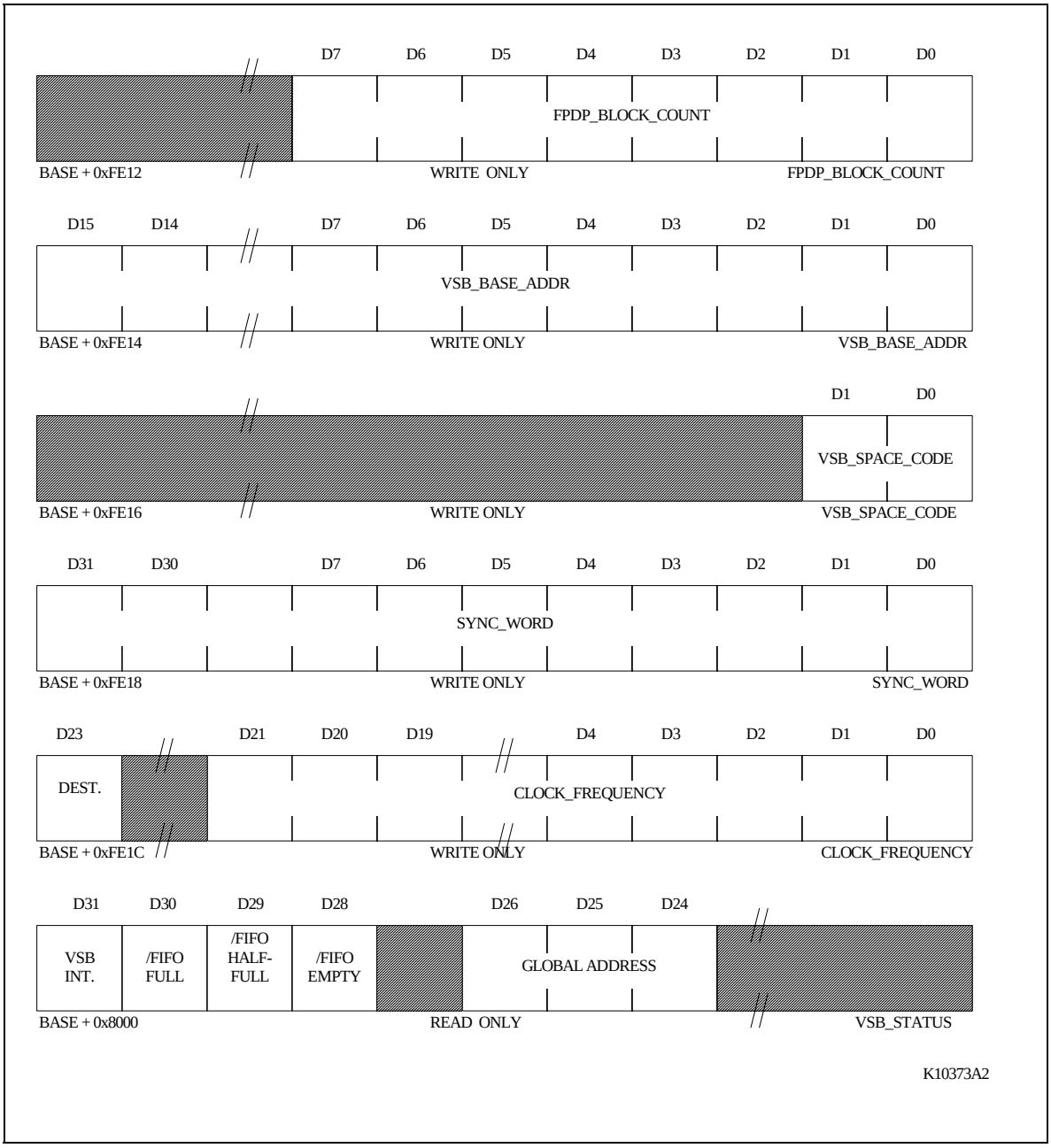

Figure 12 - ICS-110BL Register Descriptions (cont'd)

SOFTWARE DEVICE DRIVERS

A comprehensive software device driver for the VxWorks real-time operating system supports the ICS-110BL. The driver includes the following elements:

- A device driver conforming to the VxWorks model, including support for Open, Close, Read, Write and IOCTL functions, and device initialization and attachment.

- A comprehensive library of high-level functions, which may be included with the application programmer's code. They provide control of all aspects of the ICS-110BL. Programmers are advised to use the library in preference to direct use of the device driver interface, since this will reduce the need to understand the details of board operation and will speed up integration.

- Driver and library source code. For users who wish to port the driver to their own operating system, complete 'C' language source code is provided.

The following are examples of some of the library routines. Each function carries a list of parameters that are not described here:

ics110blSampleRateSet()	Sets the sampling frequency.
ics110blVmeInterruptWait()	Waits for interrupt or timeout to occur
ics110blDeviceReset()	Resets ICS-110BL to initial conditions
ics110blMasterSet()	Sets board as sampling master (for multiple board configurations)
ics110blAcqSrcSet()	Sets acquisition trigger as internal or external
int ics110blOutputModeSet()	Sets the output path as VMEbus, VSB or FPDP
ics110blOversamplingSet()	Sets the converter oversampling ratio
ics110blDecimationSet()	Set decimation ratio
ics110blIntVectorSet()	Load VMEbus interrupt vector
ics110blVsbBaseAddressSet()	Load VSB base address
ics110blStatusRead()	Read board status
ics110blFifoRead()	Read sample data
ics110blSampleRateSet()	Set frequency of onboard sampling clock
ics110blProgramAdc()	Set converter characteristics such as software initiated calibration, FIR filter coefficients
ics110blCalibrateAdc()	Calibrate ICS-110BL converters
ics110blGainSet()	Set signal conditioner gain
ics110blAcquireSet()	Start conversion