

NT5117405J

4,194,304-word X 4-bit

Dynamic RAM : Fast Page Mode with EDO

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## **NT 511740C5J Data Sheet**

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## 1. DESCRIPTION

The NT511740C5J is a 4,194,304-word x 4-bit dynamic RAM fabricated in NTC's CMOS silicon gate technology. The NT511740C5J achieves high integration , high-speed operation , and low-power consumption due to quadruple polysilicon double metal CMOS. The NT511740C5J is available in a 26/24-pin plastic SOJ.

## 2. FEATURES

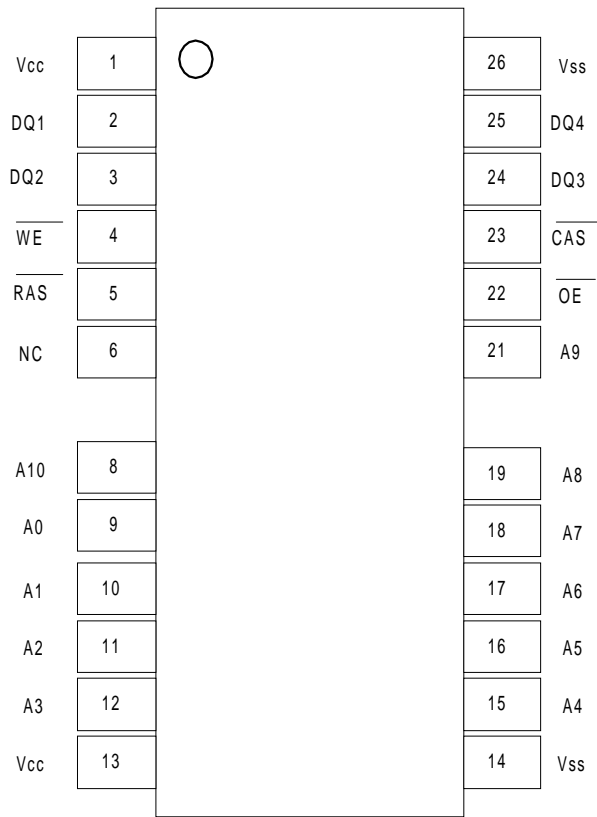
- 4,194,304-word x 4-bit configuration
- Single 5V power supply,+/-10% tolerance
- Input :TTL compatible , low input capacitance
- Output :TTL compatible , 3-state
- Refresh :2048 cycles/32 ms
- Fast page mode with EDO, read modify write capability
- /CAS before /RAS refresh, hidden refresh, /RAS-only refresh capability
- Multi-bit test mode capability
- Package options:

26/24-Pin 300 mil plastic SOJ (SOJ26/24-P300) (Product:NT511740C5J-XX)  
XX indicates speed rank.

## 3. PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEA</sub>		Operation(Max.)	Standby(Max.)
NT511740C5J-50	50ns	25ns	13ns	13ns	84ns	660mW	5.5 mW
NT511740C5J-60	60 ns	30 ns	15 ns	15 ns	104 ns	605mW	
NT511740C5J-70	70 ns	35 ns	20 ns	20 ns	124 ns	550 mW	

### 4. PIN CONFIGURATION (TOPVIEW)



26/24-Pin Plastic SOJ

Pin Name	Function
A0-A10	Adress input
$\overline{\text{RAS}}$	Row Adress Strobe
$\overline{\text{CAS}}$	Column Adress Strobe
DQ1-DQ4	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
Vcc	Power Supply (5v)
Vss	Ground(0V)
NC	No Connection

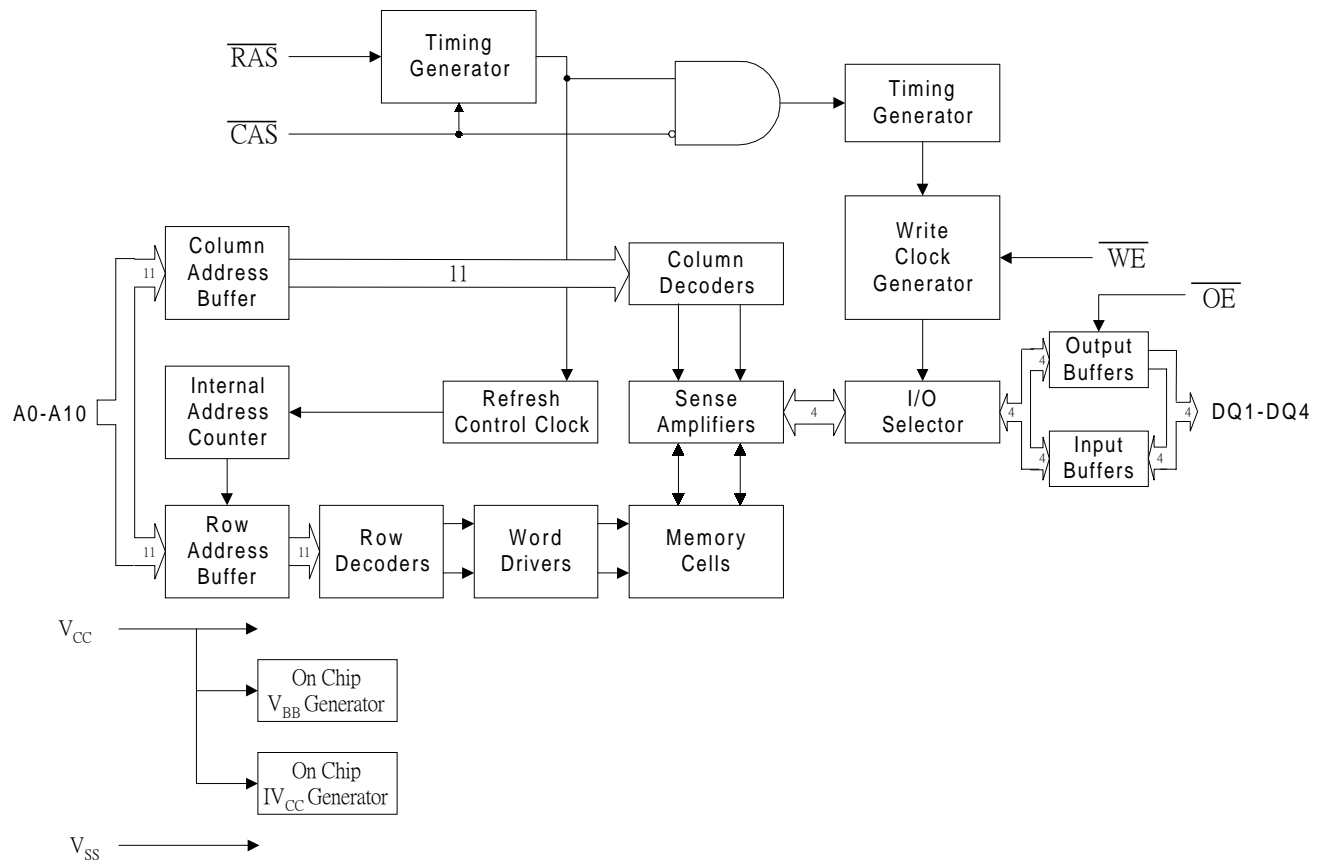
Note: The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

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## 5. BLOCK DIAGRAM



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## 6. ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to VSS	$V_{IN}, V_{OUT}$	-0.3 to $V_{CC}+0.3$	V
Voltage on $V_{CC}$ Supply Relative to VSS	$V_{CC}$	-0.5 to 7	V
Short Circuit Output Current	$I_{OS}$	50	mA
Po/WEr Dissipation	$P_D^*$	1	W
Operation Temperature	$T_{opr}$	0 to 70	$^{\circ}C$
Storage Temperature	$T_{stg}$	-55 to 150	$^{\circ}C$

\*: $T_a = 25^{\circ}C$

### Recommended Operating Conditions

( $T_a = 0^{\circ}C$  to  $70^{\circ}C$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Po/WEr Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V

### Capacitance

( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 25^{\circ}C$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0-A10)	$C_{IN1}$	-	5	pF
Input Capacitance (/RAS,/CAS,/WE,/OE)	$C_{IN2}$	-	7	pF
Output Capacitance (DQ1-DQ4)	$C_{IO}$	-	7	pF

## 7. DC Characteristics

(V<sub>CC</sub>=5V+/-10% , Ta=0 °C to 70 °C)

Parameter	Symbol	Condition	NT511740C 5J-50		NT511740C 5J-60		NT511740C 5J-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-5.0 mA	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	
Output LOW Voltage	V <sub>OL</sub>	I <sub>OL</sub> =4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I <sub>LI</sub>	0V<=V <sub>I</sub> <=6.5V; All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I <sub>LO</sub>	DQ disable 0V<=V <sub>O</sub> <=5.5V	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I <sub>CC1</sub>	/RAS,CAC cycling, tRC = Min.	-	120	-	110	-	100	mA	1,2
Power Supply Current (Standby)	I <sub>CC2</sub>	/RAS , /CAS=VIH	-	2	-	2	-	2	mA	1
		/RAS, /CAS >=V <sub>CC</sub> -0.2V	-	1	-	1	-	1		
Average Power Supply Current (/RAS-only Refresh)	I <sub>CC3</sub>	/RAS cycling, /CAS = VIH, tRC=Min.	-	120	-	110	-	110	mA	1,2
Power Supply Current (Standby)	I <sub>CC5</sub>	/RAS= VIH, /CAS= VIL, DQ = enable	-	5	-	5	-	5	mA	1
Average Power Supply Current (/CAS before /RAS Refresh)	I <sub>CC6</sub>	/RAS cycling, /CAS before /RAS	-	110	-	100	-	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I <sub>CC7</sub>	/RAS=VIL, /CAS cycling t <sub>pc</sub> =Min.	-	110	-	100	-	90	mA	1,3

- Notes G
1. ICC Max. is specified as I<sub>CC</sub> for output open condition.
  2. Address can be changed once or less while /RAS=V<sub>IL</sub>.
  3. Address can be changed once or less while /CAS=V<sub>IH</sub>.

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8. AC Characteristics (1/3)

(V<sub>cc</sub>=5V 10% ,T<sub>a</sub>=0 °C to 70 °C ) Note:1,2,3,12,13

Parameter	Symbol	NT511740C5J-50		NT511740C5J-60		NT511740C5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	84	-	104	-	124	-	ns	
Read Modify Write Cycle Time	t <sub>RWC</sub>	110	-	135	-	160	-	ns	
Fast Page Mode Cycle Time	t <sub>HPC</sub>	20	-	25	-	30	-	ns	
Fast Page Mode Read Modify Write Cycle Time	t <sub>PRWC</sub>	58	-	68	-	78	-	ns	
Access Time form /RAS	t <sub>RAC</sub>	-	50	-	60	-	70	ns	4,5,6
Access Time form /CAS	t <sub>CAC</sub>	-	13	-	15	-	20	ns	4,5
Access Time form Column Address	t <sub>AA</sub>	-	25	-	30	-	35	ns	4,6
Access Time form /CAS Precharge	t <sub>CPA</sub>	-	30	-	35	-	40	ns	4
Access Time form /OE	t <sub>OEa</sub>	-	13	-	15	-	20	ns	4
Output Low Impedance Time from /CAS	t <sub>CLZ</sub>	0	-	0	-	0	-	ns	4
Data Output Hold After /CAS Low	t <sub>DOH</sub>	5	-	5	-	5	-	ns	
/CAS to Data Output Buffer Turn-off Delay Time	t <sub>CEZ</sub>	0	13	0	15	0	20	ns	7,8
/RAS to Data Output Buffer Turn-off Delay Time	t <sub>REZ</sub>	0	13	0	15	0	20	ns	7,8
/OE to Data Output Buffer Turn-off Delay Time	t <sub>OEZ</sub>	0	13	0	15	0	20	ns	7
/WE to Data Output Buffer Turn-off Delay Time	t <sub>WEZ</sub>	0	13	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	1	50	1	50	1	50	ns	3
Refresh Period	t <sub>REF</sub>	-	32	-	32	-	32	ms	
/RAS Precharge Time	t <sub>RP</sub>	30	-	40	-	50	-	ns	
/RAS Pulse Width	t <sub>RAS</sub>	50	10,000	60	10,000	70	10,000	ns	
/RAS Pulse Width (Fast Page Mode with EDO)	t <sub>RASP</sub>	50	100,000	60	100,000	70	100,000	ns	



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AC Characteristics (2/3)

Parameter	Symbol	NT10511740C5J-50		NT511740C5J-60		NT511740C5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
/RAS Hold Time	$t_{RSH}$	7	-	10	-	13	-	ns	
/RAS Hold Time referenced to /OE	$t_{ROH}$	7	-	10	-	13	-	ns	
/CAS Precharge Time (Fast Page Mode with EDO)	$t_{CP}$	7	-	10	-	13	-	ns	
/CAS Pulse Width	$t_{CAS}$	7	10,000	10	10,000	13	10,000	ns	
/CAS Hold Time	$t_{CSH}$	35	-	40	-	45	-	ns	
/CAS to /RAS Precharge Time	$t_{CRP}$	5	-	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge Time	$t_{RHCP}$	30	-	35	-	40	-	ns	
/OE Hold Time from /CAS (DQ Disable)	$t_{CHO}$	5	-	5	-	5	-	ns	
/RAS to /CAS Delay Time	$t_{RCD}$	11	37	14	45	14	50	ns	5
/RAS to Column Address Delay Time	$t_{RAD}$	9	25	12	30	12	35	ns	6
Row Address Set-up Time	$t_{ASR}$	0	-	0	-	0	-	ns	
Row Address Hold Time	$t_{RAH}$	7	-	10	-	13	-	ns	
Column Address Set-up Time	$t_{ASC}$	0	-	0	-	0	-	ns	
Column Address Hold Time	$t_{CAH}$	7	-	10	-	13	-	ns	
Column Address to /RAS Lead Time	$t_{RAL}$	25	-	30	-	35	-	ns	
Read Command Set-up Time	$t_{RCS}$	0	-	0	-	0	-	ns	
Read Command Hold Time	$t_{RCH}$	0	-	0	-	0	-	ns	9
Read Command Hold Time referenced to /RAS	$t_{RRH}$	0	-	0	-	0	-	ns	9
Write Command Set-up Time	$t_{WCS}$	0	-	0	-	0	-	ns	10

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AC Characteristics (3/3)

(Vcc=5V +/-10% ,Ta=0 °C to 70 °C) Note 1,2,3,12,13

Parameter	Symbol	NT511740C5J-50		NT511740C5J-60		NT511740A5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time	t <sub>WCH</sub>	7	-	10	-	13	-	ns	
Write Command Pulse Width	t <sub>WP</sub>	7	-	10	-	10	-	ns	
/WE Pulse Width (DQ Disable)	t <sub>WPE</sub>	7	-	10	-	10	-	ns	
/OE Command Hold Time	t <sub>OEH</sub>	7	-	10	-	13	-	ns	
/OE Precharge Time	t <sub>OEP</sub>	7	-	10	-	10	-	ns	
/OE Command Hold Time	t <sub>OCH</sub>	7	-	10	-	10	-	ns	
Write Command to /RAS Lead Time	t <sub>RWL</sub>	7	-	10	-	13	-	ns	
Write Command to /CAS Lead Time	t <sub>CWL</sub>	7	-	10	-	13	-	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	-	0	-	0	-	ns	11
Data-in Hold Time	t <sub>DH</sub>	7	-	10	-	13	-	ns	11
/OE to Data-in Delay Time	t <sub>OED</sub>	13	-	15	-	20	-	ns	
/CAS to /WE Delay Time	t <sub>CWD</sub>	30	-	34	-	44	-	ns	10
Column Address to /WE Delay Time	t <sub>AWD</sub>	42	-	49	-	59	-	ns	10
/RAS to /WE Delay Time	t <sub>RWD</sub>	67	-	79	-	94	-	ns	10
/CAS Precharge /WE Delay Time	t <sub>CPWD</sub>	47	-	54	-	64	-	ns	10
/CAS Active Delay Time from /RAS Precharge	t <sub>RPC</sub>	5	-	5	-	5	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t <sub>CSR</sub>	5	-	5	-	5	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t <sub>CHR</sub>	10	-	10	-	10	-	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t <sub>WRP</sub>	10	-	10	-	10	-	ns	
/WE Hold Time /RAS (/CAS before /RAS)	t <sub>WRH</sub>	10	-	10	-	10	-	ns	
/RAS to /WE Set-up Time (Test Mode)	t <sub>WTS</sub>	10	-	10	-	10	-	ns	
/RAS to /WE Hold Time (Test Mode)	t <sub>WTH</sub>	10	-	10	-	10	-	ns	

## Notes:

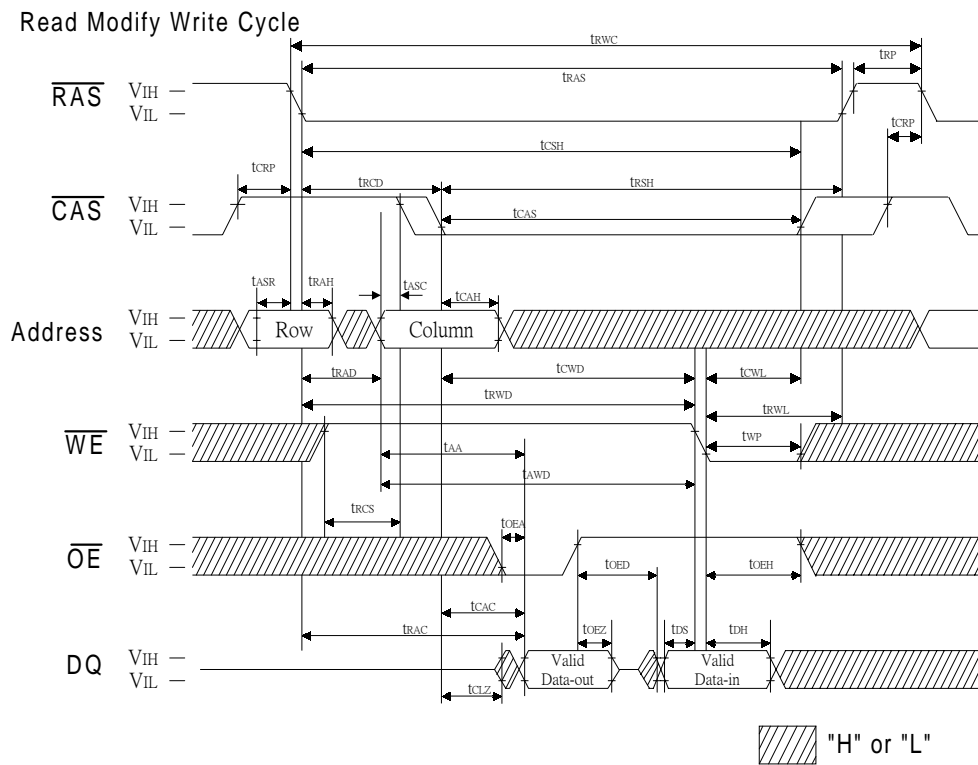
1. A start-up delay of 200  $\mu$ s is required after po/WEr-up,follo/WEd by a minimum of eight initialization cycles (/RAS-only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
2. The AC characteristics assume  $t_T=2$  ns.
3.  $V_{IH}(\text{Min.})$  and  $V_{IL}(\text{Max.})$  are reference levels for measuring input timing signals. Transition time ( $t_T$ ) are measured bet/WEen  $V_{IH}$  and  $V_{IL}$ .
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the  $t_{RCD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  
 $t_{RCD}(\text{Max.})$  is specified as a reference point only . If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{Max.})$  limit, access time is controlled by  $t_{CAC}$ .
6. Operation within the  $t_{RAD}(\text{Max.})$  limit ensures that  $t_{RAC}(\text{Max.})$  can be met.  
 $t_{RAD}(\text{Max.})$  is specified as a reference point only . If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{Max.})$  limit, access time is controlled by  $t_{AA}$ .
7.  $t_{CEZ}(\text{Max.})$ ,  $t_{REZ}(\text{Max.})$ ,  $t_{WEZ}(\text{Max.})$  and  $t_{OEZ}(\text{Max.})$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8.  $t_{CEZ}$  and  $t_{REZ}$  must be satisfied for open circuit condition .
9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$ , and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only . If  $t_{WCS} \geq t_{WCS}(\text{Min.})$ , the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{Min.})$  ,  $t_{RWD} \geq t_{RWD}(\text{Min.})$  ,  $t_{AWD} \geq t_{AWD}(\text{Min.})$  and  $t_{CPWD} \geq t_{CPWD}(\text{Min.})$ , the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to /CAS leading edge in an early write cycle, and to /WE leading edge in an /OE control write cycle or a read modify write cycle .
12. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 8-bit locations .Since all 4 DQ pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a /RAS-only refresh cycle or a /CAS before /RAS refresh cycle.
13. In a test mode read cycle , the value of access time parameters is delayed for 5 ns for the specified value . These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.



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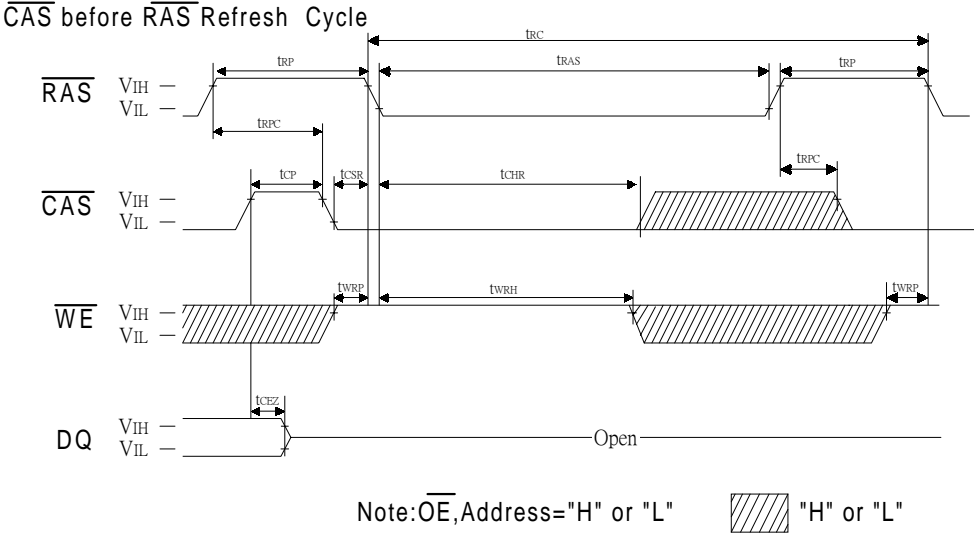
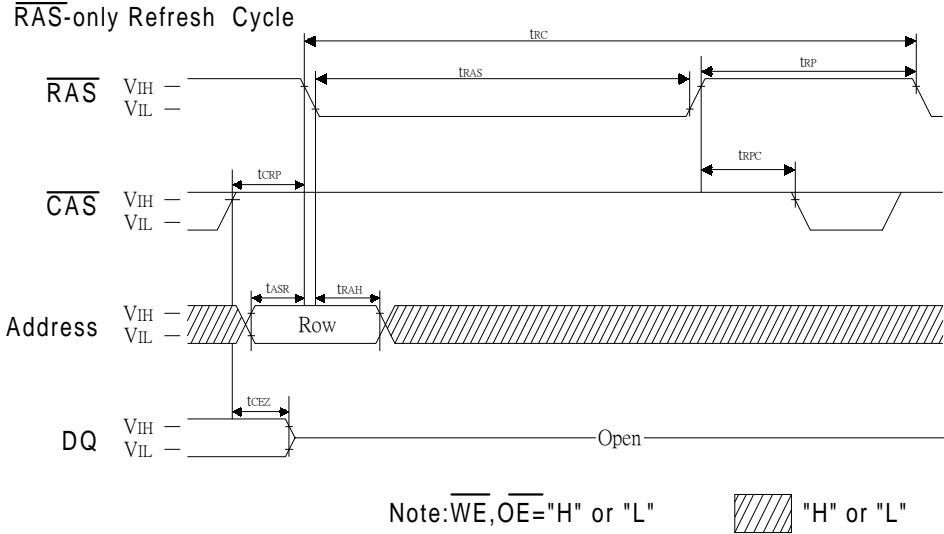




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