

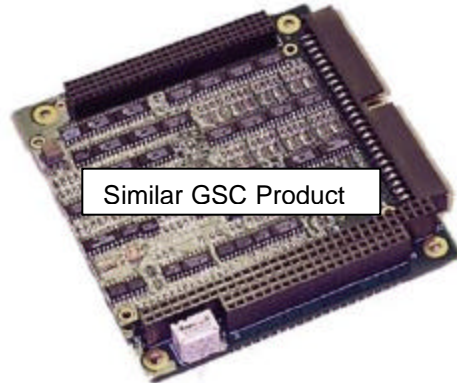
# General Standards Corporation

**High Performance Bus Interface Solutions**

## PC104P-16HSDI

### 16-Bit, Six-Channel Sigma-Delta Analog Input PMC Board

*With 1.1 MSPS Sample Rate per Channel, and Two Independent Clocks*



#### ***Features Include:***

- Sigma-Delta Conversion; No External Antialiasing Filters Required
- High Effective Sampling Rate; 16-32 Times the Effective Rate of Successive Approximation Converters Operating at the Same Conversion Rate
- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components
- Software-Selectable Ranges:  $\pm 1.25$  Volts,  $\pm 2.5$  Volts,  $\pm 5$  Volts or  $\pm 10$  Volts
- Six 16-Bit Analog Input Channels; Dedicated Sigma-Delta Converter per Channel
- Sample Rates Adjustable up to 1,100 K-Samples per Second per Channel
- Two Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution
- Low Noise; Less than  $130\mu\text{VRMS}$  on  $\pm 1.25$  Volt Input Range
- 64K-Sample FIFO Buffer. All Data is Channel-Tagged.
- Harmonic Sampling Supported, with Clocking Ratios Between Channels from 1 to 20
- Auto calibration Uses Hardware Correction; No missing Codes Introduced
- Integral Shield Assures Minimum Susceptibility to Radiated Noise in PMC Environments
- Single-width PMC Form Factor
- VxWorks™ and WinNT™ Drivers are available

#### ***Applications Include:***

- |                            |                       |                              |
|----------------------------|-----------------------|------------------------------|
| ✓ Acoustics Analysis       | ✓ Voltage Measurement | ✓ Automatic Test Equipment   |
| ✓ Analog Inputs            | ✓ Process Monitoring  | ✓ Audio Waveform Analysis    |
| ✓ Data Acquisition Systems | ✓ Industrial Robotics | ✓ Environmental Test Systems |

### **General Standards Corporation**

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## High Performance Bus Interface Solutions

### Overview:

The 6-channel PC104P-16HSDI analog input board provides high-density precision 16-bit analog input resources in a single-width PMC form factor. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements, to the analysis of complex audio signals and waveforms. Each of the six sigma-delta analog input channels can be controlled by either of two independent sample clocks, and multiple channels can be harmonically locked together. Sample rates are adjustable from 30 KSPS to 1.1 MSPS, and the input range is software selectable as  $\pm 1.25V$ ,  $\pm 2.5V$ ,  $\pm 5V$  or  $\pm 10V$ . Internal auto calibration networks permit periodic calibration to be performed without removing the board from the system.

### Functional Description:

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1). Each of the six input channels contains an input buffer, an adaptive digital-image filter, and a dedicated sigma-delta A/D converter (ADC). The inputs can be configured for either differential or single-ended operation, or an internal voltage reference can be applied to all channels to support self-test operations and auto calibration. Gain and offset trimming of the input channels is performed by calibration DAC's that are loaded with channel correction values during auto calibration. The use of calibration DAC's eliminates the missing codes that occur when analog input channels are calibrated exclusively in the digital domain.

Each ADC contains a digital antialiasing filter that rejects out-of-band signals above approximately 48 percent of the selected sample rate. Conversion data from all active channels is transferred to the PCI bus through a 64K-sample data buffer that has a software-controlled threshold for generating interrupt requests. Multiple channels can be synchronized to perform synchronous sampling, either by a software command, or by external hardware sync and clock input signals.

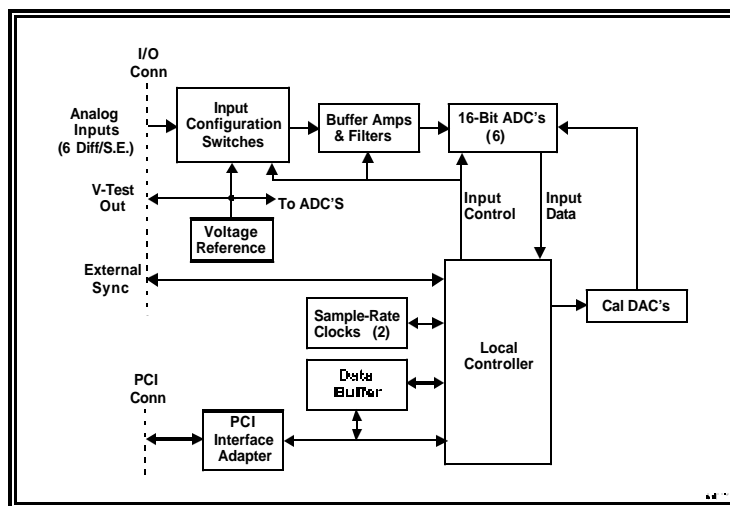


Figure 1. PC104P-16HSDI; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and supports the "plug-n-play" initialization concept. System input/output connections are made at the front panel through a high-density metal-shrouded 37-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

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### ELECTRICAL SPECIFICATIONS

At +25 °C, with specified operating voltages.

#### □ Input Channel Characteristics:

Configuration:	6 input channels, software controlled as differential or single-ended. Optional 2-channel and 4-channel configurations available.
Voltage Range:	Software Configurable as $\pm 1.25$ Volts, $\pm 2.5$ Volts, $\pm 5$ Volts or $\pm 10$ Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line.
Common Mode Rejection:	80 dB, DC-60 Hz (Differential mode)
Common Mode Range:	$\pm 10$ Volts with zero normal-mode input
Offset Voltage:	$\pm 0.6$ millivolts, maximum
Signal-to-Noise Ratio:	85dB at 30 KSPS, 80dB at 1100KSPS, typical.
Overvoltage Protection:	$\pm 30$ -Volt transient with power applied; $\pm 15$ Volts with power removed

#### □ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)															
Sample Rate:	30,000 to 1,100,000 samples per second per channel															
Oversampling Factor:	x64															
DC Accuracy: (Maximum composite error)	<table><thead><tr><th>Range</th><th>Midscale Accuracy</th><th><math>\pm</math>Fullscale Accuracy</th></tr></thead><tbody><tr><td><math>\pm 10V</math></td><td><math>\pm 1.2mV</math></td><td><math>\pm 5.2mV</math></td></tr><tr><td><math>\pm 5V</math></td><td><math>\pm 1.1mV</math></td><td><math>\pm 3.1mV</math></td></tr><tr><td><math>\pm 2.5V</math></td><td><math>\pm 0.9mV</math></td><td><math>\pm 2.2mV</math></td></tr><tr><td><math>\pm 1.25V</math></td><td><math>\pm 0.8mV</math></td><td><math>\pm 1.5mV</math></td></tr></tbody></table>	Range	Midscale Accuracy	$\pm$ Fullscale Accuracy	$\pm 10V$	$\pm 1.2mV$	$\pm 5.2mV$	$\pm 5V$	$\pm 1.1mV$	$\pm 3.1mV$	$\pm 2.5V$	$\pm 0.9mV$	$\pm 2.2mV$	$\pm 1.25V$	$\pm 0.8mV$	$\pm 1.5mV$
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$\pm 2.5V$	$\pm 0.9mV$	$\pm 2.2mV$														
$\pm 1.25V$	$\pm 0.8mV$	$\pm 1.5mV$														
Small Signal Bandwidth:	DC to approximately 48 percent of the selected sample rate															
Power Bandwidth:	DC to $2 \times 10^6$ Hz- $V_{pp}$ minimum. Accepts 100kHz input at 20 VPP.															
Crosstalk Rejection:	84 dB typical, DC-10 kHz															
Antialias Filtering:	Each ADC provides internal digital antialias filtering at approximately 48 percent of the selected sample rate. This digital filter is supported by a multi-pole analog filter that rejects interference at the harmonic images of the digital filter. The cutoff frequency of the analog filter in each channel is optimized automatically in response to the selected sample rate.															
Integral Nonlinearity:	$\pm 0.003$ percent of FSR, typical															
Differential Nonlinearity:	$\pm 0.0015$ percent of FSR, maximum															
Total Harmonic Distortion:	84 dB typical, from DC to 40 percent of sample rate															

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### □ Operating Modes and Controls

- Organization:** Two 3-channel analog input groups, and two sample rate generators. Each channel group can operate from either rate generator. The sample rate for each individual channel is selected by dividing the frequency of the assigned rate generator by any integer from 1 through 20.
- Sample Rate Generators:** Either of two independent internal rate generators can be assigned to any input channel group. Each generator is adjustable from 19.2 MHz to 38.4 MHz, and provides sample rates from 600 KSPS to 1200 KSPS after division by 32 (x16 oversampling), or from 300 KSPS to 600 KSPS after division by 64 (x32 oversampling). Subsequent division by an integer from 1 to 20 for each channel provides sample rates from 15 KSPS to 1200 KSPS. (Specified performance is guaranteed only within the range from 30 KSPS to 1100 KSPS). Settling time when changing frequencies is approximately 20 ms, and settling completion is selectable as an interrupt event. Setting resolution is 0.2 percent or less; accuracy is  $\pm 0.08$  percent.
- External Clock I/O:** An LVDS hardware output clock can be derived either from a 16-32 MHz LVDS external hardware input clock or from an internal rate generator. The external clock input can be selected as the rate generator for any or all channels. .
- Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. This requires a split I/O cable. As many as six boards can be daisy-chained together.
- Synchronization:** Sampling can be synchronized within each channel group through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize the sampling among multiple boards.
- Harmonic Sampling:** Harmonic sampling ratios are implemented by adjusting the sample rates of channels within a group to specific fractions of the assigned rate generator frequency. (See Sample Rate Generators).
- Data Format:** Software selected as either offset binary or two's complement
- Channel Tags:** Each input data value is appended with a 3-bit channel identification tag.
- Buffer Size Register:** Contains the total number of samples present in the input data buffer.
- Buffer Threshold Flags:** A threshold flag is asserted when the number of samples in the input data buffer equals or exceeds the selected threshold. The buffer threshold can be any integer from 0000 to FFFEh.

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## High Performance Bus Interface Solutions

### PCI INTERFACE

- Compatibility:** Conforms to PCI Specification 2.2, with D32 read/write transactions.  
Supports "plug-n-play" initialization.  
Provides a single multifunction interrupt.  
Supports FIFO DMA transfers as bus master.
  
- Board Control and Data Registers (D32 Access)**
  - Board Control/Status Register: Determines the principal operating mode.
  - Rate Generator Registers: Select rate generator frequencies.
  - Channel Control Registers: Control the clock sources and sample rates for all input channels.
  - Input Data Buffer: 64K by 18-Bit FIFO buffer.
  - Buffer Threshold: Selects the input data buffer threshold.
  - Interrupt Control: Interrupt source control and status.

- Analog Input Buffer**

Analog input data is read through a 64K-sample FIFO buffer as a 19-Bit data field for each input sample. The data field contains a 16-Bit conversion value and a 2-Bit channel tag. A threshold flag occurs when the associated buffer contains a number of data samples that exceeds a software-selected threshold from 0000h to FFFEh, and can be used to generate empty and full flags.

### MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

- Power Requirements**

+5VDC  $\pm$ 0.2 VDC at 1.5 Amps maximum  
Power Dissipation: 6.0 Watts, Side 1  
1.5 Watts, Side 2

- Physical Characteristics**

Height: 13.5 mm (0.53 in)  
Depth: 149.0 mm (5.87 in)  
Width: 74.0 mm (2.91 in)  
Shield: Side 1 is protected by an EMI shield.

- Environmental Specifications**

Ambient Temperature Range: Operating: 0 to +55 degrees Celsius  
Storage: -40 to +85 degrees Celsius  
Relative Humidity: Operating: 0 to 80%, non-condensing  
Storage: 0 to 95%, non-condensing  
Altitude: Operation to 10,000 ft.

- Cooling Requirements**

Conventional air cooling; 200 LPFM (typical mezzanine environment).

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### ORDERING INFORMATION

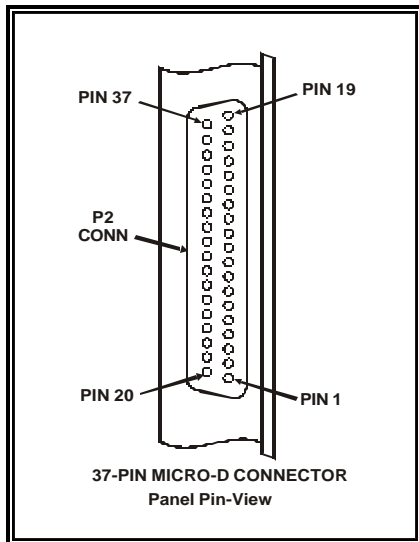
Specify the basic product model number (PC104P-16HSDI), followed by an option suffix "-A", as indicated below. For example, model number PC104P-16HSDI-6 describes a board with 6 input channels.

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	2 Channels	A = 2
	4 Channels	A = 4
	6 Channels	A = 6

### SYSTEM I/O CONNECTIONS

**Table 1. System Connector Pin Functions**

PIN	SIGNAL	PIN	SIGNAL
1	INPUT RETURN	20	INPUT CHAN 00 HI
2	INPUT RETURN	21	INPUT CHAN 00 LO
3	INPUT RETURN	22	INPUT CHAN 01 HI
4	INPUT RETURN	23	INPUT CHAN 01 LO
5	INPUT RETURN	24	INPUT CHAN 02 HI
6	INPUT RETURN	25	INPUT CHAN 02 LO
7	INPUT RETURN	26	INPUT CHAN 03 HI
8	INPUT RETURN	27	INPUT CHAN 03 LO
9	INPUT RETURN	28	INPUT CHAN 04 HI
10	INPUT RETURN	29	INPUT CHAN 04 LO
11	INPUT RETURN	30	INPUT CHAN 05 HI
12	VTEST	31	INPUT CHAN 05 LO
13	VTEST RETURN	32	INPUT RETURN
14	DIGITAL RETURN	33	DIGITAL RETURN
15	DIGITAL RETURN	34	SYNC INPUT HI
16	CLOCK INPUT HI	35	SYNC INPUT LO
17	CLOCK INPUT LO	36	SYNC OUTPUT HI
18	CLOCK OUTPUT HI	37	SYNC OUTPUT LO
19	CLOCK OUTPUT LO		



**Figure 2. System Input/Output Connector**

**System Mating Connector:**

Rugged 37-pin 0.050" dual-row connector with metal shell. Board connector mates with cable connector type (includes prewired 36-inch pigtail wires):

Min-E-Con MCE-37PCBRPT

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