General Standards Corporation

High Performance Bus Interface Solutions

PMC-16VSDI2

16-Bit, Two-Channel Sigma-Delta Analog Input PMC

With 10.0 MSPS Sample Rate per Channel, and Two Independent Clocks

PRELIMINARY

Features Include:

- Two-Channel Sigma-Delta Conversion with Per-Channel Rates to 10 MSPS
- High Effective Sampling Rate; 2-8 Times the Effective Rate of Successive Approximation Converters Operating at the Same Conversion Rate
- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components
- External Antialiasing Filters Not Required for Most Applications
- Software-Selectable Ranges: ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
- Sample Rates from 1.0 KSPS to 10.0 MSPS (Megasamples per Second) per Channel
- Two Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution
- 64K-Sample FIFO Buffer with Tagged Synchronous or Asynchronous Data
- Optional Packed Synchronous Data Format
- Harmonic Sampling Supported, with Adjustable Clocking Ratios Between Channels
- Autocalibration Uses Hardware Correction; No missing Codes Introduced
- Integral Shield Minimizes Susceptibility to Radiated Noise in PMC Environments
- Single-width PMC Form Factor
- VxWorks™ and WinNT™ Drivers are available

Applications Include:

- ✓ Waveform Analysis
- ✓ Wideband Analog Inputs
- ✓ Data Acquisition
- ✓ Communications
- ✓ Acoustics
- ✓ Environmental Test Systems

REV 020202

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256)880-8787 or (800)653-9970
FAX: (256)880-8788
Email: sales@generalstandards.com

Overview:

The two-channel PMC-16VSDI2 analog input board provides wideband precision 16-bit analog input resources in a single-width PMC form factor. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements, to the analysis of complex acoustic signals and waveforms. Each input channel can be clocked from either of two independent sample clocks, or both channels can be harmonically locked together. Sample rates are adjustable from 1.0 KSPS to 10.0 MSPS, and the input range is software selectable as ±1.25V, ±2.5V, ±5V or ±10V. Internal auto calibration networks permit periodic calibration to be performed without removing the board from the system.

Functional Description:

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1). Each input channel contains an input buffer, an adaptive digital-image filter, and a dedicated sigma-delta A/D converter. A digital antialiasing filter rejects out-of-band signals above approximately 45 percent of the selected sample rate. The inputs can be configured for differential or single-ended operation, or an internal voltage reference can be applied to both channels to support selftest operations and autocalibration. Calibration DAC's provide gain and offset trimming of both input channels.

Conversion data is transferred to the PCI bus through a 64K-sample data buffer that is supported with a software-controlled threshold flag. Both channels can be synchronized to perform synchronous sampling, either from an internal rate generator or with external hardware clock, trigger and sync I/O signals. Optional data packing provides a second 64K buffer to pack two synchronous 16-Bit data values into a single D32 transaction.

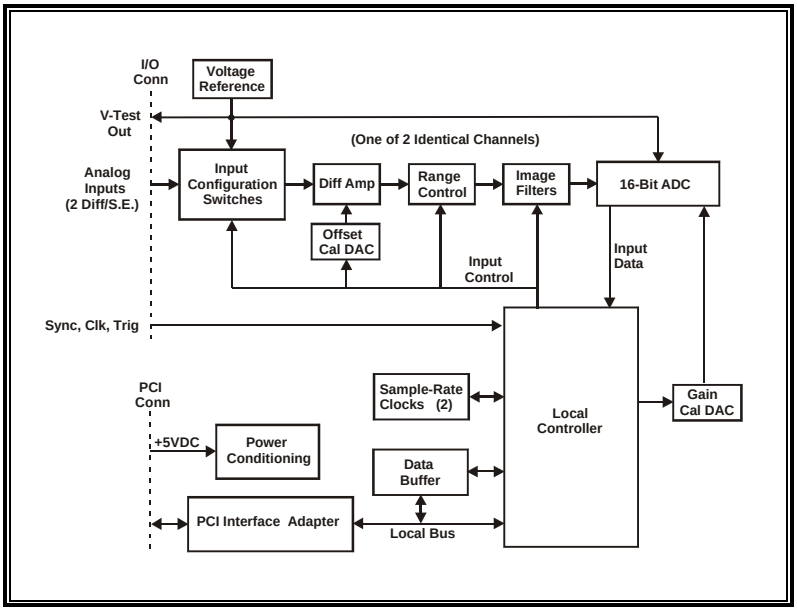

Figure 1. PMC-16VSDI2; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and supports the "plug-n-play" initialization concept. System input connections are made at the front panel through standard SMB connectors. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages.

❑ Input Channel Characteristics:

Configuration:	Two input channels, software controlled as differential or single-ended. 50-Ohm SMB connectors, insulated from panel. Optional one-channel version available.
Voltage Range:	Software-configurable as ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line. Optional 50-Ohm line-line input termination available, with a corresponding amplitude limitation of 3.0VRMS.
Common Mode Rejection:	80 dB, DC-60 Hz (Differential mode)
Common Mode Range:	±10 Volts with zero normal-mode input
Overvoltage Protection:	±30-Volt transient with power applied; ±15 Volts with power removed. With standard 1.0 Megohm inputs (See Input Impedance).

❑ Transfer Characteristics:

Resolution: 16 Bits (0.0015 percent of FSR)

Sample Rate: 1,000 to 10,000,000 samples per second per channel *

Oversampling Factor: DC-2.5MSPS: x8, 2.5-5.0MSPS: x4, 5.0-10.0MSPS: x2.

DC Accuracy:
(Maximum composite error)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±1.5mV	±5.2mV
±5V	±1.1mV	±3.1mV
±2.5V	±0.9mV	±2.2mV
±1.25V	±0.8mV	±1.5mV

Small Signal Bandwidth: DC to approximately 45 percent of the selected sample rate; DC to 4.5MHz.

Power Bandwidth: DC to 30 MHz-Vpp typical. E.g.: 10 VPK-PK at 3.0 MHz.

Dynamics: Typical at -0.5dBFS, Fsig = 0.3*Fsamp. (Tsamp = sample period = 1/Fsamp)

Sample Rate	Settling Time, 1LSB	SFDR	THD	SNR
1KSPS-2.5MSPS	61*Tsamp	94dB	-91dB	80dB
2.5MSPS-5.0MSPS	25*Tsamp	91dB	-87dB	75dB
5.0MSPS-10MSPS	14*Tsamp	75dB	-74dB	70dB

Crosstalk Rejection: 86 dB typical, DC-10 kHz; 74dB DC-1MHz; 70dB DC-4MHz

Antialias Filtering: Digital antialias filtering at approximately 45 percent of the selected sample rate. The digital filter is supported by a simple analog filter that rejects interference at harmonic images of the digital filter, and that is optimized automatically for the selected sample rate.

* Contact factory for the availability of a 12-Bit 20 MSPS version of this board.

DC Integral Nonlinearity:	±0.003 percent of FSR, typical
DC Differential Nonlinearity:	±0.0015 percent of FSR, maximum

❑ Operating Modes and Controls

Sample Rate Generators:	Either of two independent internal rate generators can be assigned to either input channel. Each generator is adjustable from 20 MHz to 40 MHz, and provides sample rates from 1.25 MSPS to 2.5 MSPS after division by 16 (x8 oversampling), 2.5-5.0 MSPS after division by 8 (x4 oversampling), or 5.0-10.0 MSPS after division by 4 (x2 oversampling). Subsequent division by an integer from 1 to 1250 for each channel provides a wide range of sample rates from 1.0 KSPS to 10.0 MSPS. Setting resolution is 0.2 percent or less; accuracy is ±0.08 percent. Rate generator frequencies are divided by two to ensure a 50% duty cycle
External Clock:	The internal rate generators can be replaced by an external 20-40 MHz external hardware clock. The external clock is divided internally by two to ensure a 50% duty cycle, and can be selected as the rate generator for either channel.
Synchronization:	Sampling can be synchronized (deskewed) between channels through software, or by an external hardware TTL sync input.
Triggering:	Although the sigma-delta process is essentially continuous, data acquisition can be initiated and terminated externally through a TTL trigger input. In this burst-acquisition mode, the data from either or both input channels is ignored until a trigger occurs. A trigger initiates the accumulation of input data in the input buffer. Data acquisition can be stopped either by defining a specific block size, or by specifying "stop-on-second-trigger."
Harmonic Sampling:	Harmonic sampling ratios are implemented by adjusting the sample rates of both channels to specific fractions of a common rate generator frequency. (See Sample Rate Generators).
Data Coding:	Software selected as either offset binary or two's complement
Data Format:	17-Bit data value, with 16-Bit data field and single-bit channel tag. Optional packed-data configuration is 32-Bits wide with two 16-Bit data values; (D31:16 = Chan-B data, D15:00 = Chan-A data).
Buffer Configuration:	64K deep by 17-Bits wide. Optional packed-data configuration buffer is 64K deep by 32-Bits wide. (2-Channel boards only)
Buffer Size Register:	Contains the total number of samples present in the input data buffer.
Buffer Threshold Flags:	A threshold flag is asserted when the number of samples in the input data buffer equals or exceeds the selected threshold. The buffer threshold can be any integer from 0000 to FFFEh.

PCI INTERFACE

❑ **Compatibility:** Conforms to PCI Specification 2.2, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Single multifunction interrupt.
FIFO DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5VDC ±0.2 VDC at 1.4 Amps maximum, 1.1 Amps typical

Maximum Power Dissipation: 6.0 Watts, Side 1
1.5 Watts, Side 2

❑ Physical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side 1 is protected by an EMI shield.

❑ Environmental Specifications

Ambient Temperature Range: Operating: 0 to +70 degrees Celsius *
Storage: -40 to +85 degrees Celsius
* Board inlet air temperature.

Relative Humidity: Operating: 0 to 80%, non-condensing
Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

❑ Cooling Requirements

Conventional air cooling; 200 LPFM (typical mezzanine environment).

ORDERING INFORMATION

Specify the basic product model number (PMC-16VSDI2), followed by an option suffix "-A-B-C", as indicated below. For example, model number PMC-16VSDI2-2-DP-1M describes a 2-Channel board with data packing and 1-Megohm input impedance.

Optional Parameter *	Description	Specify Option As:
Number of Input Channels:	One Input Channel	A = 1
	Two Input Channels	A = 2
Data Packing	No Packing; 16-Bit Data plus Channel Tag	B = NP
	Data Packing: 32-Bit Data (Two 16-Bit channels)	B = DP **
Input Impedance::	1.0 Megohm Inputs	C = 1M
	50 Ohms Inputs (3VRMS max input level)	C = 50

* Contact factory for the availability of a 12-Bit 20 MSPS version of this board.

** Available only with 2-Channel boards.

SYSTEM I/O CONNECTIONS

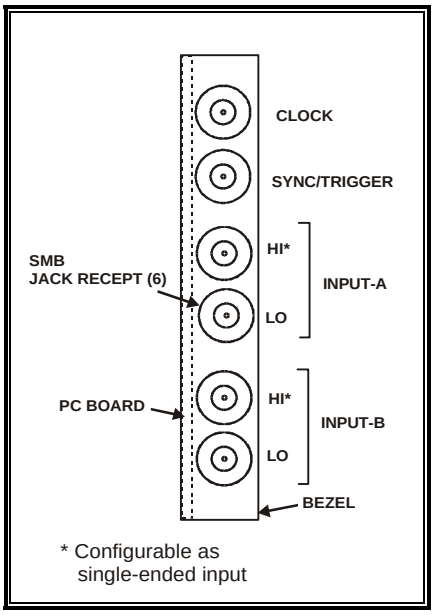

Figure 2. System Connectors

System Mating Connector:

Standard SMB, coaxial plug receptacle:

Cable Type	Connector*
0.086 semi-rigid	131-3693-001
RG-178/U,196	131-3402-001
RG-161/U	131-3403-001
RG-316DS	131-3404-001

* Johnson Components

General Standards Corp.
8302A Whitesburg Drive
Huntsville, AL 35802