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MM-6326 Data Sheet

A 64 Mbyte, Super Fast, Dual Port, VME/VSB Compatible DRAM Memory Module

FEATURES:

- **Capacity:** 8M, 16M, 32M 64M bytes
- **Cycle/Access Time (nsec):** Read 125/75, Write 125/50 (Block Transfer-BLT, Page Mode and Bank-Interleave)
- **Compatible with** VMEbus Rev C1 and VSBbus Rev C with A32/A24/D16/D8 (UAT) for VME and A32/D32 for VSB
- **Block transfer** for sequential access for both ports
- **Parity** generation and checking for error detection on each byte
- **Module selection** on 1 Mbyte boundaries, jumper-selectable for lower and upper limits on each bus
- **VMEbus Control Status Register** (CSR) for parity reporting and control
- **Write-Wrong parity** for diagnostics
- **Lifetime Warranty**

DESCRIPTION:

The MM-6326D is a high speed, dual-port, single card slot, high density memory module that provides up to 64 Mbytes for VME/VSB systems. It is intended for high performance applications employing Bank-Interleave, Page Mode and Block Transfer at data rates greater than 30 Mbytes/sec. It also supports sequential access (BLT) of 256 bytes on the VME and 64 Kbytes on the VSB bus.

The MM-6326D is compatible with MVME130/131, MVME135/136, MVME141 and Delta Series systems.

The Control Status Register (CSR), located in the short I/O address space, stores and reads byte-wide parity errors detected on the VME/VSB buses. The other bits enable Write-Wrong parity for diagnostics, disable VME-port and determine whether the memory is CACHEable on the VSB bus. Parity generation and checking are provided for each byte; parity status is stored and transmitted via BERR*.

Reliability is ensured by burn-in and running memory diagnostics that check operation for 48 hours while temperature-cycling boards from 0 to 60 degrees (Celsius). Also, reliability is backed up by Micro Memory, Inc's. **Lifetime Warranty.**

SPECIFICATIONS:

Capacity

8M, 16M, 32M, 64M bytes

Cycle/Access Time (nsec)

Read: 125/75, Write: 125/50 (Block Transfer-BLT, Page Mode and Bank-Interleave)
Read: 200/150, Write: 200/90 (Bank-Interleave)

Address

32 bits for VMEbus
32 bits multiplexed with 32 data bits for the VSB bus

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Data In/Data Out

8, 16, 32 bits (UAT) for VMEbus
32 bits for VSB bus

Sequential Access

Block Transfer (BLT) of 256 bytes on VMEbus
64K bytes on VSB bus

Address Modifiers

AM0-AM5 are decoded by socketed IFL with the following codes:
A24: 39, 3A, 3D and 3E
A32: 09, 0A, 0D and 0E
A24 with BLT: 38, 3F
A32 with BLT: 0B, 0F

Parity Checking

Byte-wide parity generation and checking; parity output stored and transmitted via CSR;
Write-Wrong parity for diagnostics

Control Status Register (CSR)

Read/Write, 8 bits wide, jumper-selectable, occupies one location in VME I/O space (A16)

CSR Format

D0 Enable Parity Out
D1 Write-Wrong Parity
D2 Memory CACHEable for VSB
D6 VMEbus Disable
D7 Parity Error
Others: Don't Care

Interface

VME Rev C1 and VSB Rev C

Modes of Operation

Read, write, read-modify-write, Page Mode in BLT, and refresh

Memory Selection

Two independent memory banks, jumper-selectable on 1 Mbyte (100000H) boundaries for each port by setting the upper and lower limits

Operating Temperatures

0 to +60 degrees (Celsius)

Storage Temperature

-40 to +85 degrees (Celsius)

Relative Humidity

Up to 95% without condensation

Power Requirements:

5V at 5.5A

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