



Features

- Superior voice solution with low noise and excellent part-to-part gain accuracy
- 3 kV_{RMS} line isolation
- Simultaneous ringing detection and CID monitoring for worldwide applications
- Provides both full-wave ringing detect and half-wave ringing detect for maximum versatility
- Transmit power of up to +10 dBm into 600 Ω
- Data access arrangement (DAA) solution for modem speeds up to V.92
- 3.3V or 5 V power supply operation
- Easy interface with modem ICs and voice CODECs
- Worldwide dial-up telephone network compatibility
- CPC5622 can be used in circuits that comply with the requirements of TIA/EIA/IS-968 (FCC part 68), UL60950 (UL1950), EN/IEC 60950-1 Supplementary Isolation Compliant, IEC60950, EN55022B, CISPR22B, EN55024, and TBR-21
- Line-side circuit powered from telephone line
- Compared to other silicon DAA solutions, LITELINK:
 - Uses fewer passive components
 - Takes up less printed-circuit board space
 - Uses less telephone line power
 - Is a single-IC solution

Applications

- Computer telephony and gateways, such as VoIP
- PBXs
- Satellite and cable set-top boxes
- V.92 (and other standard) modems
- Fax machines
- Voicemail systems
- Embedded modems for POS terminals, automated banking, remote metering, vending machines, security, and surveillance



Description

LITELINK III is a single-package silicon phone line interface (PLI) DAA used in voice and data communication applications to make connections between low-voltage equipment and high-voltage telephone networks.

LITELINK uses on-chip optical components and a few inexpensive external components to form the required high voltage isolation barrier. LITELINK eliminates the need for large isolation transformers or capacitors used in other phone line interface configurations.

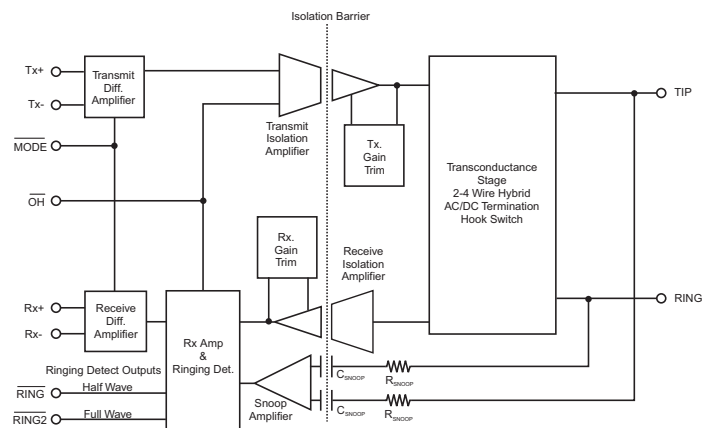
LITELINK also provides AC and DC phone line terminations, switchhook, 2-wire to 4-wire hybrid, ringing detection, and full time receive on-hook transmission capability.

The CPC5622 is a member of, and builds upon, IXYS Integrated Circuits Division's third generation of LITELINK products with improved insertion loss performance and lower minimum current draw from the phone line. The CPC5622 version of LITELINK III provides concurrent ringing detection and CID monitoring for world wide applications. Both half-wave and full-wave ringing detection are provided for maximum versatility.

Ordering Information

| Part Number | Description |
|-------------|--|
| CPC5622A | 32-Pin SOIC Phone Line Interface, 50/tube |
| CPC5622ATR | 32-Pin SOIC Phone Line Interface, tape and reel, 1000/reel |

CPC5622 Block Diagram



| | |
|---|-----------|
| 1. Electrical Specifications | 3 |
| 1.1 Absolute Maximum Ratings | 3 |
| 1.2 Performance | 4 |
| 1.3 Pin Description | 5 |
| 2. Application Circuits | 6 |
| 2.1 Resistive Termination Application Circuit | 6 |
| 2.1.1 Resistive Termination Application Circuit Part List | 7 |
| 2.2 Reactive Termination Application Circuit | 8 |
| 2.2.1 Reactive Termination Application Circuit Part List | 9 |
| 3. Using LITELINK | 10 |
| 3.1 Switch Hook Control (On-hook and Off-hook States) | 10 |
| 3.2 On-hook Operation: $\overline{OH}=1$ | 10 |
| 3.2.1 Ringing Signal Reception via the Snoop Circuit | 10 |
| 3.3 Off-Hook Operation: $\overline{OH}=0$ | 12 |
| 3.3.1 Receive Signal Path | 12 |
| 3.3.2 Transmit Signal Path | 12 |
| 3.4 Initialization Requirement Following Power-up | 13 |
| 3.5 DC Characteristics | 13 |
| 3.5.1 Setting a Current Limit | 13 |
| 3.6 AC Characteristics | 13 |
| 3.6.1 Resistive Termination Applications | 13 |
| 3.6.2 Reactive Termination Applications | 13 |
| 3.6.3 Mode Pin Usage | 13 |
| 4. Regulatory Information | 14 |
| 5. LITELINK Design Resources | 14 |
| 6. LITELINK Performance | 15 |
| 7. Manufacturing Information | 17 |
| 7.1 Mechanical Dimensions | 18 |

1. Electrical Specifications

1.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|--|---------|----------------|-------------|
| V_{DD} | -0.3 | 6 | V |
| Logic Inputs | -0.3 | $V_{DD} + 0.3$ | V |
| Continuous Tip to Ring Current ($R_{ZDC} = 5.2\Omega$) | - | 150 | mA |
| Total Package Power Dissipation | - | 1 | W |
| Isolation Voltage | - | 3000 | V_{rms} |
| Operating temperature | -40 | +85 | $^{\circ}C$ |
| Storage temperature | -40 | +125 | $^{\circ}C$ |

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Unless otherwise specified all specifications are at 25 $^{\circ}C$ and $V_{DD}=5.0V$.

1.2 Performance

| Parameter | Minimum | Typical | Maximum | Unit | Conditions |
|---|----------------|---------|---------|------------------|---|
| DC Characteristics | | | | | |
| Operating Voltage V_{DD} | 3.0 | - | 5.5 | V | Low-voltage side |
| Operating Current I_{DD} | - | 9 | 13 | mA | Low-voltage side |
| Operating Voltage V_{DDL} | 2.8 | - | 3.2 | V | Line side, derived from tip and ring |
| Operating Current I_{DDL} | - | 7 | 8 | mA | Line side, drawn from tip and ring while off-hook |
| On-hook Characteristics | | | | | |
| Metallic DC Resistance | 10 | - | - | M Ω | Tip to ring, 100 Vdc applied |
| Longitudinal DC Resistance | 10 | - | - | M Ω | 150 Vdc applied from tip and ring to Earth ground |
| Ringing Signal Detect Level | 5 | - | - | V _{rms} | 68 Hz ringing signal applied across tip and ring |
| Ringing Signal Detect Level | 28 | - | - | V _{rms} | 15 Hz ringing signal applied across tip and ring |
| Snoop Circuit Frequency Response | 166 | - | >4000 | Hz | -3 dB corner frequency @ 166 Hz, in IXYS Integrated Circuits Division application circuit |
| Snoop Circuit CMRR ¹ | - | 40 | - | dB | 120 V _{RMS} 60 Hz common-mode signal across tip and ring |
| Ringer Equivalence | - | 0.01B | - | REN | |
| Longitudinal Balance ¹ | 60 | - | - | dB | Per FCC part 68 |
| Off-Hook Characteristics | | | | | |
| AC Impedance | - | 600 | - | Ω | Tip to ring, using resistive termination application circuit |
| Longitudinal Balance ¹ | 60 | - | - | dB | Per FCC part 68 |
| Return Loss | - | 26 | - | dB | Into 600 Ω at 1800 Hz |
| Transmit and Receive Characteristics | | | | | |
| Frequency Response | 30 | - | 4000 | Hz | -3 dB corner frequency 30 Hz |
| Transhybrid Loss | - | 36 | - | dB | Into 600 Ω at 1800 Hz, with C18 in the resistive termination application circuit |
| Transmit and Receive Insertion Loss | -0.4 | 0 | 0.4 | dB | 30 Hz to 4 kHz, Resistive termination application circuit with \overline{MODE} de-asserted. Reactive termination application circuit with \overline{MODE} asserted. |
| Average In-band Noise | - | -126 | - | dBm/Hz | 4 kHz flat bandwidth |
| Harmonic Distortion | - | -80 | - | dB | -3 dBm, 600 Hz, 2 nd harmonic |
| Transmit Level | - | - | 2.2 | V _{P-P} | Single-tone sine wave. Or 0 dBm into 600 Ω . |
| Receive Level | - | - | 2.2 | V _{P-P} | Single-tone sine wave. Or 0 dBm into 600 Ω . |
| RX+/RX- Output Drive Current | - | - | 0.5 | mA | Sink and source |
| TX+/TX- Input Impedance | 60 | 90 | 120 | k Ω | |
| Isolation Characteristics | | | | | |
| Isolation Voltage | 3000 | - | - | V _{rms} | Line side to Low-voltage side, one minute duration |
| Surge Rise Time | 2000 | - | - | V/ μ S | No damage via tip and ring |
| MODE and OH Control Logic Inputs | | | | | |
| Input Low Voltage | - | - | 0.8 | V _{IL} | |
| Input High Voltage | 2.0 | - | - | V _{IH} | |
| High Level Input Current | - | - | -120 | μ A | $V_{IN} \leq V_{DD}$ |
| Low Level Input Current | - | - | -120 | μ A | $V_{IN} = GND$ |
| RING and RING2 Output Logic Levels | | | | | |
| Output High Voltage | $V_{DD} - 0.4$ | - | - | V | $I_{OUT} = -400 \mu A$ |
| Output Low Voltage | - | - | 0.4 | V | $I_{OUT} = 1 \text{ mA}$ |

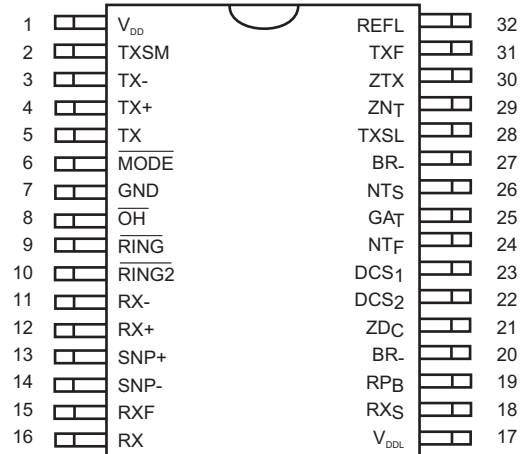
Specifications subject to change without notice. All performance characteristics based on the use of IXYS Integrated Circuits Division application circuits. Functional operation of the device at conditions beyond those specified here is not implied.

NOTES: 1) This parameter is layout and component tolerance dependent.

1.3 Pin Description

| Pin | Name | Function |
|-----|------------------|---|
| 1 | V _{DD} | Low-voltage (CPE) side power supply |
| 2 | TXSM | Transmit summing junction |
| 3 | TX- | Negative differential transmit signal to DAA from low-voltage side |
| 4 | TX+ | Positive differential transmit signal to DAA from low-voltage side |
| 5 | TX | Transmit differential amplifier output |
| 6 | MODE | When asserted low, changes gain of TX path (-7 dB) and RX path (+7 dB) to accommodate reactive termination networks |
| 7 | GND | Low-voltage (CPE) side analog ground |
| 8 | OH | Assert logic low for off-hook operation |
| 9 | RING | Half wave ringing detect output signal |
| 10 | RING2 | Full wave ringing detect output signal |
| 11 | RX- | Negative differential analog signal received from the telephone line. Must be AC coupled with 0.1 μF. |
| 12 | RX+ | Positive differential analog signal received from the telephone line. Must be AC coupled with 0.1 μF. |
| 13 | SNP+ | Positive differential snoop input |
| 14 | SNP- | Negative differential snoop input |
| 15 | RXF | Receive photodiode amplifier output |
| 16 | RX | Receive photodiode summing junction |
| 17 | V _{DDL} | Power supply for line side, regulated from tip and ring. |
| 18 | RXS | Receive isolation amp summing junction |
| 19 | RPB | Receive LED pre-bias current set |
| 20 | BR- | Bridge rectifier return |
| 21 | ZDC | Electronic inductor DCR/current limit |
| 22 | DCS2 | DC feedback output |
| 23 | DCS1 | V to I slope control |
| 24 | NTF | Network amplifier feedback |
| 25 | GAT | External MOSFET gate control |
| 26 | NTS | Receive signal input |
| 27 | BR- | Bridge rectifier return |
| 28 | TXSL | Transmit photodiode summing junction |
| 29 | ZNT | Receiver impedance set |
| 30 | ZTX | Transmit transconductance gain set |
| 31 | TXF | Transmit photodiode amplifier output |
| 32 | REFL | 1.25 V _{DC} reference |

Figure 1. Pinout



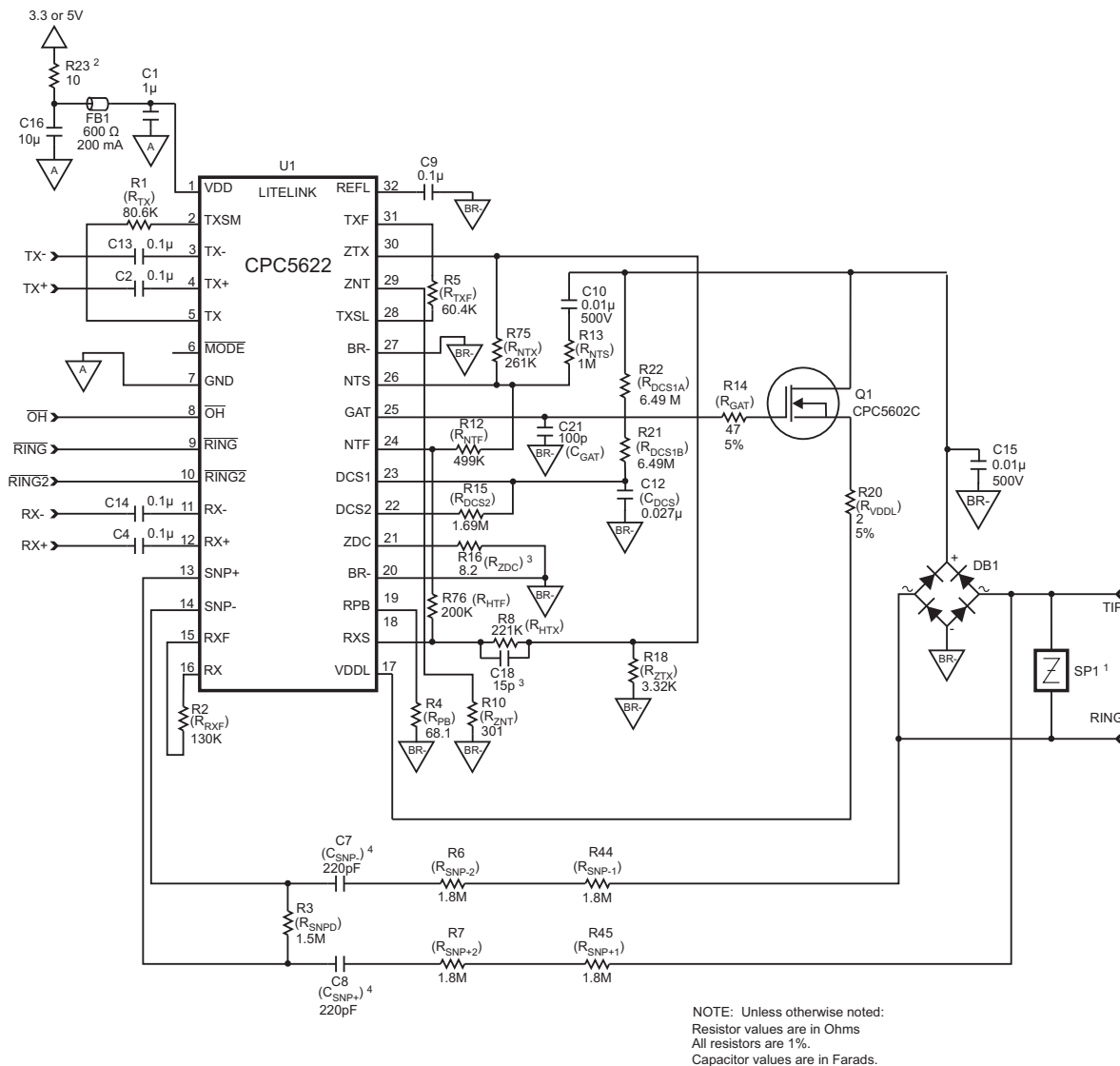
2. Application Circuits

LITELINK can be used with telephone networks worldwide. Some public telephone networks, notably in North America and Japan require a resistive line termination. Other telephone networks, such as in Europe, China and elsewhere, require a reactive line termination.

The application circuits that follow address both types of line termination models. A reactive termination application circuit that describes the TBR-21 implementation is shown in **Figure 3 on page 8**. This circuit can be easily adapted for other reactive termination needs.

2.1 Resistive Termination Application Circuit

Figure 2. Resistive Termination Application Circuit Schematic



NOTE: Unless otherwise noted:
Resistor values are in Ohms
All resistors are 1%.
Capacitor values are in Farads.

¹This design was tested and found to comply with FCC Part 68 with this Sidactor. Other compliance requirements may require a different part.
²Higher-noise power supplies may require substitution of a 220 μ H inductor, Toko 380HB-2215 or similar. See the Power Quality section of IXYS Integrated Circuits Division application note AN-146, **Guidelines for Effective LITELINK Designs** for more information.

³Optional for enhanced transhybrid loss.
⁴Use voltage ratings based on the isolation requirements of your application.

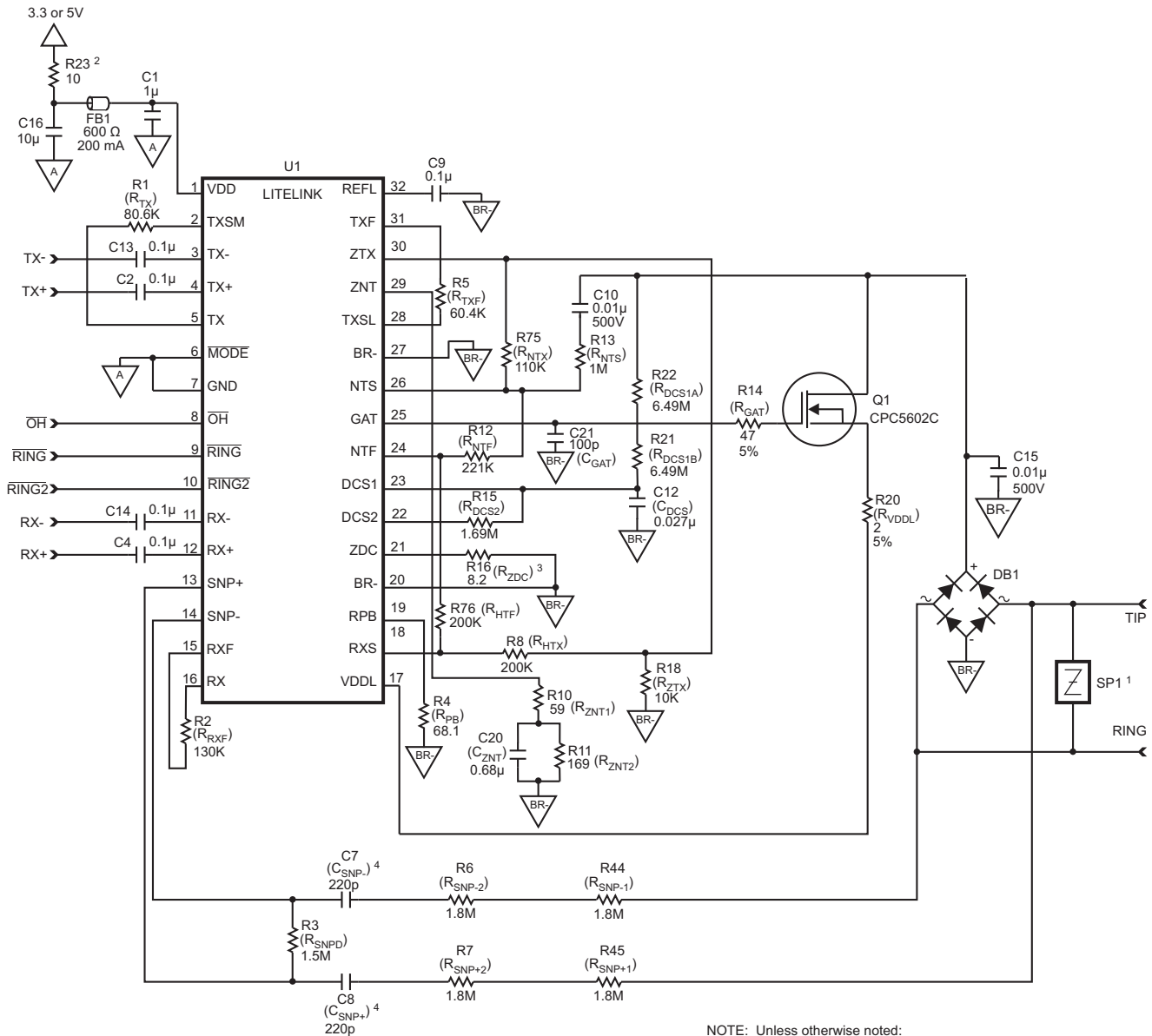
2.1.1 Resistive Termination Application Circuit Part List

| Quantity | Reference Designator | Description | Supplier(s) |
|----------|-------------------------------|---|---|
| 1 | C1 | 1 μ F, 16 V, \pm 10% | AVX, Murata, Novacap, Panasonic, SMEC, Tecate, etc. |
| 5 | C2, C4, C9, C13, C14 | 0.1 μ F, 16 V, \pm 10% | |
| 2 | C7, C8 ¹ | 220 pF, \pm 5% | |
| 2 | C10, C15 | 0.01 μ F, 500 V, \pm 10% | |
| 1 | C12 | 0.027 μ F, 16 V, \pm 10% | |
| 1 | C16 | 10 μ F, 16 V, \pm 10% | |
| 1 | C18 (optional) | 15 pF, 16 V, \pm 10% | |
| 1 | C21 | 100 pF, 16 V, 10% | |
| 1 | R1 | 80.6 k Ω , 1/16 W, \pm 1% | Panasonic, Electro Films, FMI, Vishay, etc. |
| 1 | R2 | 130 k Ω , 1/16 W, \pm 1% | |
| 1 | R3 | 1.5 M Ω , 1/16 W, \pm 1% | |
| 1 | R4 | 68.1 Ω , 1/16 W, \pm 1% | |
| 1 | R5 | 60.4 k Ω , 1/16 W, \pm 1% | |
| 4 | R6, R7, R44, R45 ² | 1.8 M Ω , 1/10 W, \pm 1% | |
| 1 | R8 | 221 k Ω , 1/16 W, \pm 1% | |
| 1 | R10 | 301 Ω , 1/16 W, \pm 1% | |
| 1 | R12 | 499 k Ω , 1/16 W, \pm 1% | |
| 1 | R13 | 1 M Ω , 1/16 W, \pm 1% | |
| 1 | R14 | 47 Ω , 1/16 W, \pm 5% | |
| 1 | R15 | 1.69 M Ω , 1/16 W, \pm 1% | |
| 1 | R16 | 8.2 Ω , 1/8 W, \pm 1% | |
| 1 | R18 | 3.32 k Ω , 1/16 W, \pm 1% | |
| 1 | R20 | 2 Ω , 1/16 W, \pm 5% | |
| 1 | R21, R22 | 6.49 M Ω , 1/16 W, \pm 1% | |
| 1 | R23 | 10 Ω , 1/16 W, \pm 5%, or 220 μ H inductor | |
| 1 | R75 | 261 k Ω , 1/16 W, \pm 1% | |
| 1 | R76 | 200 k Ω , 1/16 W, \pm 1% | |
| 1 | FB1 | 600 Ω , 200 mA ferrite bead | Murata BLM11A601S or similar |
| 1 | DB1 | S1ZB60 bridge rectifier | Shindengen, Diodes, Inc. |
| 1 | SP1 | 350 V | Bourns (TISP4350H3) or Teccor (P3100SC) |
| 1 | Q1 | CPC5602 FET | IXYS Integrated Circuits Division |
| 1 | U1 | CPC5622 LITELINK | |

¹Use voltage ratings based on the isolation requirements of your application. Typical applications will require 2kV to safely hold off the isolation voltage.
²Use components that allow enough space to account for the possibility of high-voltage arcing.

2.2 Reactive Termination Application Circuit

Figure 3. Reactive Termination Application Circuit Schematic



NOTE: Unless otherwise noted:
Resistor values are in Ohms
All resistors are 1%.
Capacitor values are in Farads.

¹This design was tested and found to comply with FCC Part 68 with this Sidactor. Other compliance requirements may require a different part.
²Higher-noise power supplies may require substitution of a 220 μH inductor, Toko 380HB-2215 or similar. See the Power Quality section of IXYS Integrated Circuits Division application note AN-146, [Guidelines for Effective LITELINK Designs](#) for more information.

³R_{ZDC} sets the loop-current limit, see [“Setting a Current Limit” on page 13](#). Also see IXYS Integrated Circuits Division application note AN-146 for heat sinking recommendations for the CPC5602C FET.

⁴Use voltage ratings based on the isolation requirements of your application.

2.2.1 Reactive Termination Application Circuit Part List

| Quantity | Reference Designator | Description | Supplier | |
|----------|-------------------------------|---|---|---|
| 1 | C1 | 1 μ F, 16 V, \pm 10% | AVX, Murata, Novacap, Panasonic, SMEC, Tecate, etc. | |
| 5 | C2, C4, C9, C13, C14 | 0.1 μ F, 16 V, \pm 10% | | |
| 2 | C7, C8 ¹ | 220 pF, \pm 5% | | |
| 2 | C10, C15 | 0.01 μ F, 500 V, \pm 10% | | |
| 1 | C12 | 0.027 μ F, 16 V, \pm 10% | | |
| 1 | C16 | 10 μ F, 16 V, \pm 10% | | |
| 1 | C20 | 0.68 μ F, 16 V, \pm 10% | | |
| 1 | C21 | 100 pF, 16 V, 10% | | |
| 1 | R1 | 80.6 k Ω , 1/16 W, \pm 1% | | Panasonic, Electro Films, FMI, Vishay, etc. |
| 1 | R2 | 130 k Ω , 1/16 W, \pm 1% | | |
| 1 | R3 | 1.5 M Ω , 1/16 W, \pm 1% | | |
| 1 | R4 | 68.1 Ω , 1/16 W, \pm 1% | | |
| 1 | R5 | 60.4 k Ω , 1/16 W, \pm 1% | | |
| 4 | R6, R7, R44, R45 ² | 1.8 M Ω , 1/10 W, \pm 1% | | |
| 1 | R8 | 200 k Ω , 1/16 W, \pm 1% | | |
| 1 | R10 | 59 Ω , 1/16 W, \pm 1% | | |
| 1 | R11 | 169 Ω , 1/16 W, \pm 1% | | |
| 1 | R12 | 221 k Ω , 1/16 W, \pm 1% | | |
| 1 | R13 | 1 M Ω , 1/16 W, \pm 1% | | |
| 1 | R14 | 47 Ω , 1/16 W, \pm 5% | | |
| 1 | R15 | 1.69 M Ω , 1/16 W, \pm 1% | | |
| 1 | R16 | 8.2 Ω , 1/8 W, \pm 1% | | |
| 1 | R18 | 10 k Ω , 1/16 W, \pm 1% | | |
| 1 | R20 | 2 Ω , 1/16 W, \pm 5% | | |
| 1 | R21, R22 | 6.49 M Ω , 1/16 W, \pm 1% | | |
| 1 | R23 | 10 Ω , 1/16 W, \pm 5%, or 220 μ H inductor | | |
| 1 | R75 | 110 k Ω , 1/16 W, \pm 1% | | |
| 1 | R76 | 200 k Ω , 1/16 W, \pm 1% | | |
| 1 | FB1 | 600 Ω , 200 mA ferrite bead | Murata BLM11A601S or similar | |
| 1 | DB1 | S1ZB60 bridge rectifier | Shindengen, Diodes, Inc. | |
| 1 | SP1 | 350 V | Bourns (TISP4350H3) or Teccor (P3100SC) | |
| 1 | Q1 | CPC5602 FET | IXYS Integrated Circuits Division | |
| 1 | U1 | CPC5622 LITELINK | IXYS Integrated Circuits Division | |

¹Use voltage ratings based on the isolation requirements of your application. Typical applications will require 2kV to safely hold off the isolation voltage.
²Use components that allow enough space to account for the possibility of high-voltage arcing.

3. Using LITELINK

As a full-featured telephone line interface, LITELINK performs the following functions:

- DC termination and V/I slope control
- AC impedance control
- 2-wire to 4-wire conversion (hybrid)
- Current limiting
- Ringing detect signalling reception
- Caller ID signalling reception
- Switch hook

LITELINK can accommodate specific application features without sacrificing basic functionality or performance. Application features include, but are not limited to:

- High transmit power operation
- Pulse dialing
- Ground start
- Loop start
- Parallel telephone off-hook detection (line intrusion)
- Battery reversal detection
- Line presence detection
- World-wide programmable operation

This section of the data sheet describes LITELINK operation in standard configuration for usual operation. IXYS Integrated Circuits Division offers additional application information on-line (see Section 5 on page 14) for the following topics:

- Circuit isolation considerations
- Optimizing LITELINK performance
- Data Access Arrangement architecture
- LITELINK circuit descriptions
- Surge protection
- EMI considerations

Other specific application materials are also referenced in this section as appropriate.

3.1 Switch Hook Control (On-hook and Off-hook States)

LITELINK operates in one of two conditions, on-hook and off-hook. In the on-hook condition the telephone line is available for calls. In the off-hook condition the telephone line is engaged. The \overline{OH} control input is used to place LITELINK in one of these two states.

With \overline{OH} high, LITELINK is on-hook and ready to make or receive a call. Also while on-hook,

LITELINK's ringing detector and CID amplifiers are both active.

Asserting \overline{OH} low causes LITELINK to answer or originate a call by entering the off-hook state. In the off-hook state, loop current flows through LITELINK.

3.2 On-hook Operation: $\overline{OH}=1$

The LITELINK application circuit leakage current is less than 10 μA with 100 V across ring and tip, equivalent to greater than 10 M Ω on-hook resistance.

3.2.1 Ringing Signal Reception via the Snoop Circuit

In the on-hook state (\overline{OH} not asserted), an internal multiplexer engages the snoop circuitry. This circuit simultaneously monitors the telephone line for two conditions; incoming ringing signal and caller ID data bursts.

Refer to the application schematic diagram (see Figure 2 on page 6). C7 ($C_{\text{SNP-}}$) and C8 ($C_{\text{SNP+}}$) provide a high-voltage isolation barrier between the telephone line and SNP- and SNP+ input pins of the LITELINK while coupling AC signals to the snoop amplifier. The snoop circuit "snoops" the telephone line continuously while drawing no dc current. In the LITELINK, the incoming ringing signals are compared to a reference level. When the ringing signal exceeds the preset threshold, the internal comparators generate the \overline{RING} and $\overline{RING2}$ signals which are output from LITELINK at pins 9 and 10, respectively. Selection of which output to use is dependent upon the support logic responsible for monitoring and filtering the ringing detect signals. To reduce or eliminate false ringing detects this signal should be digitally filtered and qualified by the system as a valid ringing signal. A logic low output on \overline{RING} or $\overline{RING2}$ indicates that the LITELINK ringing signal detect threshold has been exceeded. In the absence of any incoming ac signal the \overline{RING} and $\overline{RING2}$ outputs are held high.

The CPC5622 \overline{RING} output signal is generated by a half-wave ringing detector while the $\overline{RING2}$ output is generated by a full-wave ringing detector. A half-wave ringing detector's output frequency follows the frequency of the incoming ringing signal from the Central Office (CO) while a full-wave ringing detector's output frequency is twice that of the incoming signal. Because \overline{RING} is the output of a half-wave detector, it

will output **one** logic low pulse per cycle of the ringing frequency. Also, because the $\overline{\text{RING2}}$ is the output of a full-wave detector it will output **two** logic low pulses per cycle of the ringing frequency. Hence, the nomenclature $\overline{\text{RING2}}$ for twice the output pulses.

The set-up of the ringing detector comparator causes the $\overline{\text{RING}}$ output pulses to remain low for most of one half-cycle of the ringing signal and remains high for the entire second half-cycle of the ringing signal. For the $\overline{\text{RING2}}$ output, the pulses remain low during most of both halves of the ringing cycle and returns high for only a short period near the zero-crossing of the ringing signal. Both of the ringing outputs remain high during the silent interval between ringing bursts. Hysteresis is employed in the LITELINK ringing detector circuit to improve noise immunity.

The ringing detection threshold depends on the values of R3 (R_{SNPD}), R6 & R44 ($R_{\text{SNP-}}$), R7 & R45 ($R_{\text{SNP+}}$), C7 ($C_{\text{SNP-}}$), and C8 ($C_{\text{SNP+}}$). The value of these components shown in the application circuits are recommended for typical operation. The ringing detection threshold can be changed according to the following formula:

$$V_{\text{RINGPK}} = \left(\frac{750mV}{R_{\text{SNPD}}} \right) \sqrt{ \left[(R_{\text{SNP}_{\text{TOTAL}}} + R_{\text{SNPD}})^2 + \frac{1}{(\pi f_{\text{RING}} C_{\text{SNP}})^2} \right]}$$

Where:

- R_{SNPD} = R3 in the application circuits shown in this data sheet.
- $R_{\text{SNP}_{\text{TOTAL}}}$ = the total of R6, R7, R44, and R45 in the application circuits shown in this data sheet.
- C_{SNP} = C7 = C8 in the application circuits shown in this data sheet.
- And f_{RING} is the frequency of the ringing signal.

IXYS Integrated Circuits Division Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the ringing detection threshold will also change the caller ID gain and the timing of the polarity reversal detection pulse, if used.

3.2.2 Polarity Reversal Detection in On-hook State

The full-wave ringing detector in the CPC5622 makes it possible to detect an on-hook tip and ring battery polarity reversal using the $\overline{\text{RING2}}$ output. When the polarity of the battery voltage applied to tip and ring reverses, a pulse on $\overline{\text{RING2}}$ indicates the event. The system logic must be able to discriminate a single pulse of approximately 1 msec when using the recommended external snoop circuit components from a valid ringing signal.

3.2.3 On-hook Caller ID Signal Reception

On-hook Caller IDentity (CID) data burst signals are coupled through the snoop components, buffered through LITELINK and output at the RX+ and RX- pins.

In North America, CID data signals are typically sent between the first and second ringing signal while in other countries the CID information may arrive prior to any other signalling state.

In applications that transmit CID after the first ringing burst such as in North American, follow these steps to receive on-hook caller ID data via the LITELINK RX outputs:

1. Detect the first full ringing signal burst on $\overline{\text{RING}}$ or $\overline{\text{RING2}}$.
2. Monitor and process the CID data from the RX outputs.

For applications as in China and Brazil where CID may arrive prior to ringing, follow these steps to receive on-hook caller ID data via the LITELINK RX outputs:

1. Simultaneously monitor for CID data from the RX outputs and for ringing on $\overline{\text{RING}}$ or $\overline{\text{RING2}}$.
2. Process the appropriate signalling data.

Note: Taking LITELINK off-hook (via the $\overline{\text{OH}}$ pin) disconnects the snoop path from the receive outputs and disables the ringing detector outputs $\overline{\text{RING}}$ and $\overline{\text{RING2}}$.

CID gain from tip and ring to RX+ and RX- is determined by:

$$GAIN_{CID}(dB) = 20\log \left[\frac{6R_{SNPD}}{\sqrt{(R_{SNP_{TOTAL}} + R_{SNPD})^2 + \frac{1}{(\pi f C_{SNP})^2}}} \right]$$

Where:

- R_{SNPD} = R3 in the application circuits in this data sheet.
- $R_{SNP_{TOTAL}}$ = the total of R6, R7, R44, and R45 in the application circuits in this data sheet.
- C_{SNP} = C7 = C8 in the application circuits in this data sheet.
- and f is the frequency of the CID signal

The recommended components in the application circuits yield a gain 0.26 dB at 2000 Hz. IXYS Integrated Circuits Division Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the CID gain will also change the ringing detection threshold and the timing of the polarity reversal detection pulse, if used.

For single-ended receive applications where only one RX output is used, the snoop circuit gain can be adjusted back to 0 dB by changing the value of the snoop series resistors R6, R7, R44 and R45 from 1.8MΩ to 715kΩ. This change results in negligible modification to the ringing detect threshold.

3.3 Off-Hook Operation: $\overline{OH}=0$

3.3.1 Receive Signal Path

Signals to and from the telephone network appear on the tip and ring connections of the application circuit. Receive signals are extracted from transmit signals by the LITELINK two-wire to four-wire hybrid then converted to infrared light by the receive path LED. The intensity of the light is modulated by the receive signal and coupled across the electrical isolation barrier by a reflective dome.

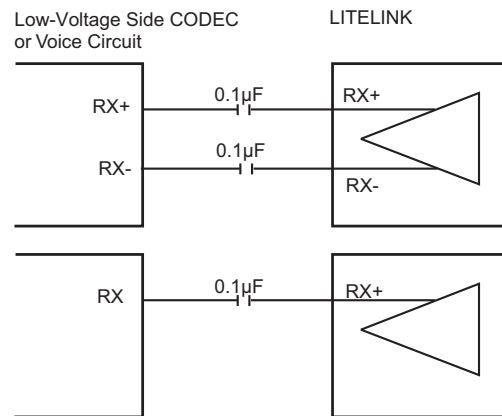
On the low voltage side of the barrier, the receive signal is converted by a photodiode into photocurrent. The photocurrent, a linear representation of the receive signal, is amplified and converted to a differential voltage output on RX+ and RX-.

Variations in gain are controlled to within ±0.4 dB by factory gain trim, which sets the output to unity gain.

To accommodate single-supply operation, LITELINK includes a small DC bias on the RX+ and RX- outputs of 1.0 Vdc. Most applications should AC couple the receive outputs as shown in Figure 4.

LITELINK may be used for differential or single-ended output as shown in Figure 4. Single-ended use will produce 6 dB less signal output amplitude. Do not exceed 0 dBm referenced to 600 Ω (2.2 V_{P-P}) signal output level with the standard application circuits. See application note AN-157, **Increased LITELINK III Transmit Power** for more information.

Figure 4. Differential and Single-ended Receive Path Connections to LITELINK



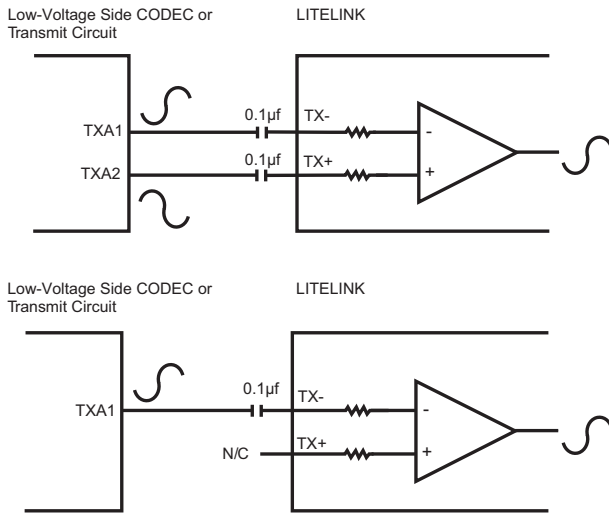
3.3.2 Transmit Signal Path

Transmit signals from the CODEC to the TX+ and TX- pins of LITELINK should be coupled through capacitors as shown in Figure 5 to minimize dc offset errors. Differential transmit signals are converted to single-ended signals within LITELINK then coupled to the optical transmit amplifier in a manner similar to the receive path.

The output of the optical amplifier is coupled to a voltage-to-current converter via a transconductance stage where the transmit signal modulates the telephone line loop current. As in the receive path, the transmit gain is calibrated at the factory, limiting insertion loss to 0 ±0.4 dB.

Differential and single-ended transmit signals into LITELINK should not exceed a signal level of 0 dBm referenced to 600 Ω (or 2.2 V_{P-P}). For output power levels above 0dBm consult the application note AN-157, **Increased LITELINK III Transmit Power** for more information.

Figure 5. Differential and Single-ended Transmit Path Connections to LITELINK



3.4 Initialization Requirement Following Power-up

$\overline{\text{OH}}$ must be de-asserted (set logic high) once after power-up for at least 50ms to transfer internal gain trim values within LITELINK. This would be normal operation in most applications. Failure to comply with this requirement will result in transmission gain errors and possibly distortion.

3.5 DC Characteristics

The CPC5622 is designed for worldwide applications. Modification of the values of the components at the ZDC, DCS1, and DCS2 pins allow for control of the VI slope characteristics of LITELINK. Selecting appropriate resistor values for R_{ZDC} (R16) and R_{DCS2} (R15) in the provided application circuits enable compliance with various DC requirements.

3.5.1 Setting a Current Limit

LITELINK includes a telephone line current limit feature that is selectable by choosing the desired value for R_{ZDC} (R16) using the following formula:

$$I_{CL} \text{ Amps} = \frac{1V}{R_{ZDC}} + 0.008A$$

IXYS Integrated Circuits Division recommends using 8.2Ω for R_{ZDC} for most applications, limiting telephone line current to 130 mA.

Whether using the recommended value above or when setting R_{ZDC} higher for a lower loop current limit refer to the guidelines for FET thermal management provided in AN-146, [Guidelines for Effective LITELINK Designs](#).

3.6 AC Characteristics

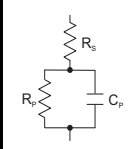
3.6.1 Resistive Termination Applications

North American and Japanese telephone line AC termination requirements are met with a resistive 600Ω ac 2-wire termination. For these applications LITELINK's 2-wire network termination impedance is set by the resistor R_{ZNT} (R10) located at the ZNT pin, pin 29, with a value of 301Ω .

3.6.2 Reactive Termination Applications

Many countries use a single-pole complex impedance to model the telephone network transmission line characteristic impedance as shown in the table below.

Line Impedance Model

| | Australia | China | TBR 21 |
|---|-----------|------------------|------------------|
|  | R_S | 220Ω | 200Ω |
| | R_P | 820Ω | 680Ω |
| | C_P | 120 nF | 100 nF |

Proper gain and termination impedance circuits for a complex impedance requires the use of complex network on ZNT as shown in the [“Reactive Termination Application Circuit”](#) on page 8.

3.6.3 $\overline{\text{MODE}}$ Pin Usage

Asserting the $\overline{\text{MODE}}$ pin low ($\overline{\text{MODE}} = 0$) introduces a 7 dB pad into the transmit path and adds 7 dB of gain to the receive path. These changes compensate for the gain changes made to the transmit and receive paths necessary for reactive termination implementations. Overall insertion loss with the reactive termination application circuit and $\overline{\text{MODE}}$ asserted is 0 dB.

Overall insertion loss with $\overline{\text{MODE}}$ de-asserted ($\overline{\text{MODE}} = 1$) for the resistive termination application circuit is 0 dB.

4. Regulatory Information

LITELINK III can be used to build products that comply with the requirements of TIA/EIA/IS-968 (formerly FCC part 68), FCC part 15B, TBR-21, EN60950, UL1950, EN55022B, IEC950/IEC60950, CISPR22B, EN55024, and many other standards. LITELINK provides supplementary isolation. Metallic surge requirements are met through the inclusion of a crow bar protection device in the application circuit. Longitudinal surge protection is provided by LITELINK's optical-across-the-barrier technology and the use of high-voltage components in the application circuit as needed.

The information provided in this document is intended to inform the equipment designer but it is not sufficient to assure proper system design or regulatory compliance. Since it is the equipment manufacturer's responsibility to have their equipment properly designed to conform to all relevant regulations, designers using LITELINK are advised to carefully verify that their end-product design complies with all applicable safety, EMC, and other relevant standards and regulations. Semiconductor components are not rated to withstand electrical overstress or electrostatic discharges resulting from inadequate protection measures at the board or system level.

5. LITELINK Design Resources

The IXYS Integrated Circuits Division web site has a wealth of information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. LITELINK data sheets also contains additional application and design information. See the following links:

LITELINK datasheets and reference designs

Application note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold**

Application note AN-146, **Guidelines for Effective LITELINK Designs**

Application note AN-155 **Understanding LITELINK Display Feature Signal Routing and Applications**

6. LITELINK Performance

The following graphs show LITELINK performance using the North American application circuit shown in this data sheet.

Figure 6. Receive Frequency Response at RX

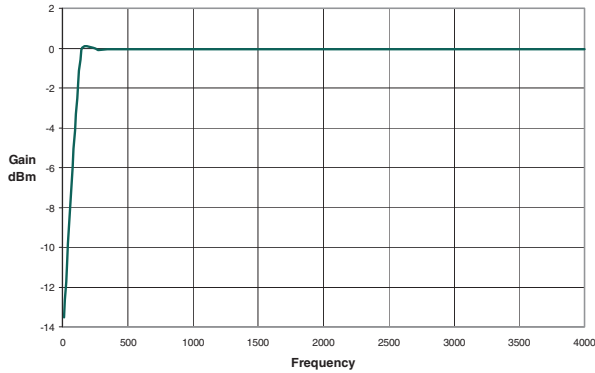


Figure 9. Transmit THD on Tip and Ring

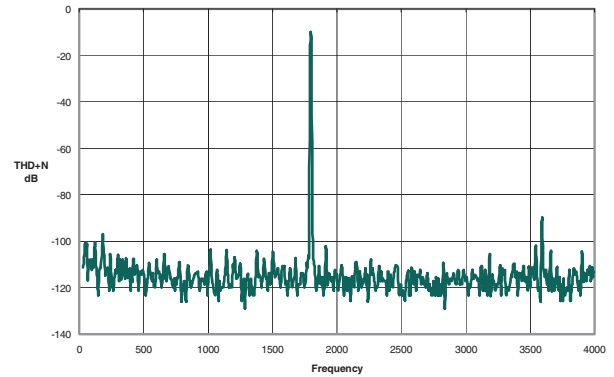


Figure 7. Transmit Frequency Response at TX

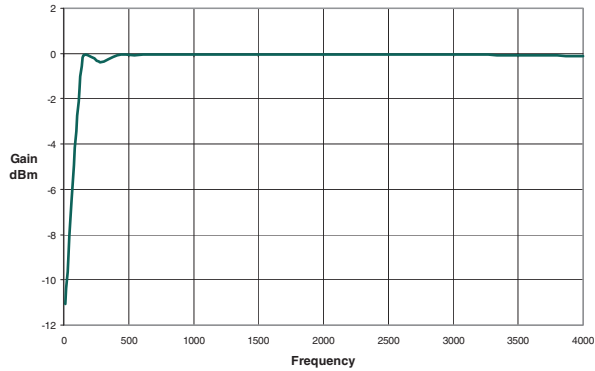


Figure 10. Transhybrid Loss

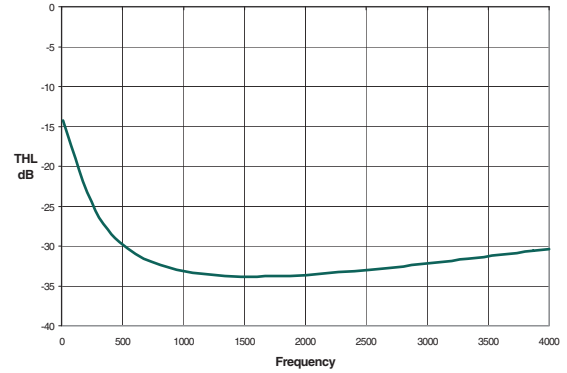


Figure 8. Receive THD on RX

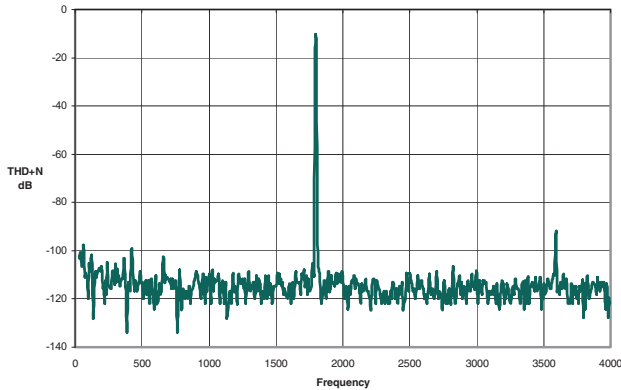


Figure 11. Return Loss

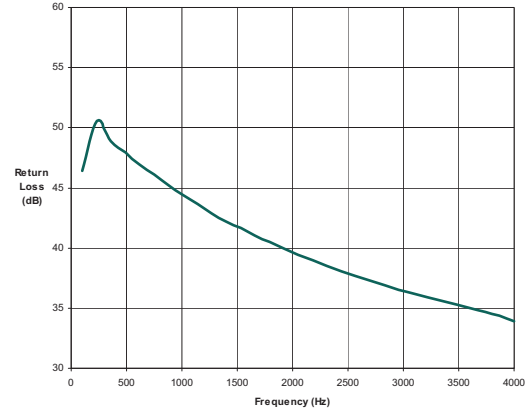


Figure 12. Snoop Circuit Frequency Response

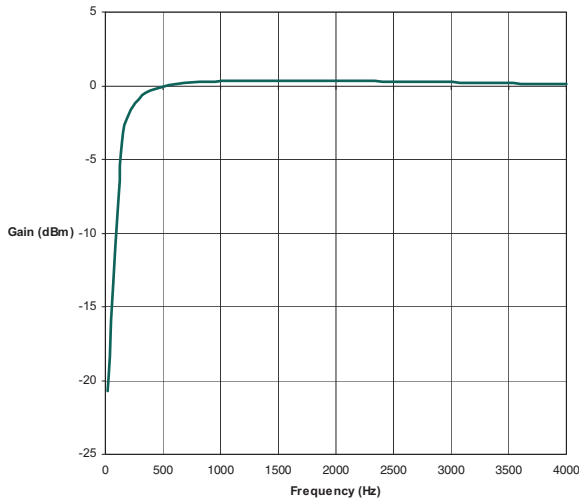


Figure 13. Snoop Circuit THD + N

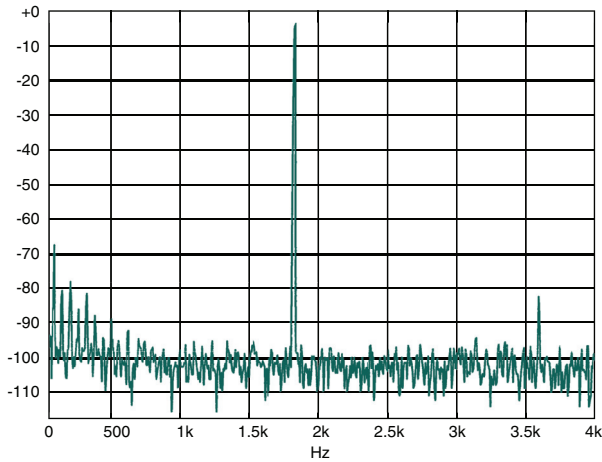
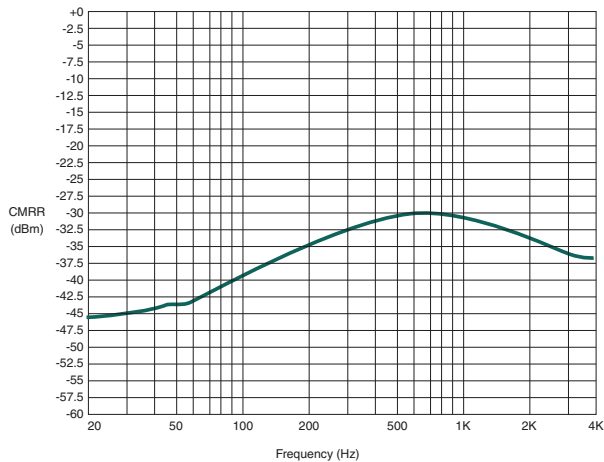


Figure 14. Snoop Circuit Common Mode Rejection



7. Manufacturing Information

7.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device | Moisture Sensitivity Level (MSL) Rating |
|----------|---|
| CPC5622A | MSL 3 |

7.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

7.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

| Device | Maximum Temperature x Time |
|----------|----------------------------|
| CPC5622A | 260°C for 30 seconds |

7.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since IXYS Integrated Circuits Division employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake could be necessary if a wash is used after solder reflow processes. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used



7.5 Mechanical Dimensions

Figure 15. CPC5622A Package Dimensions

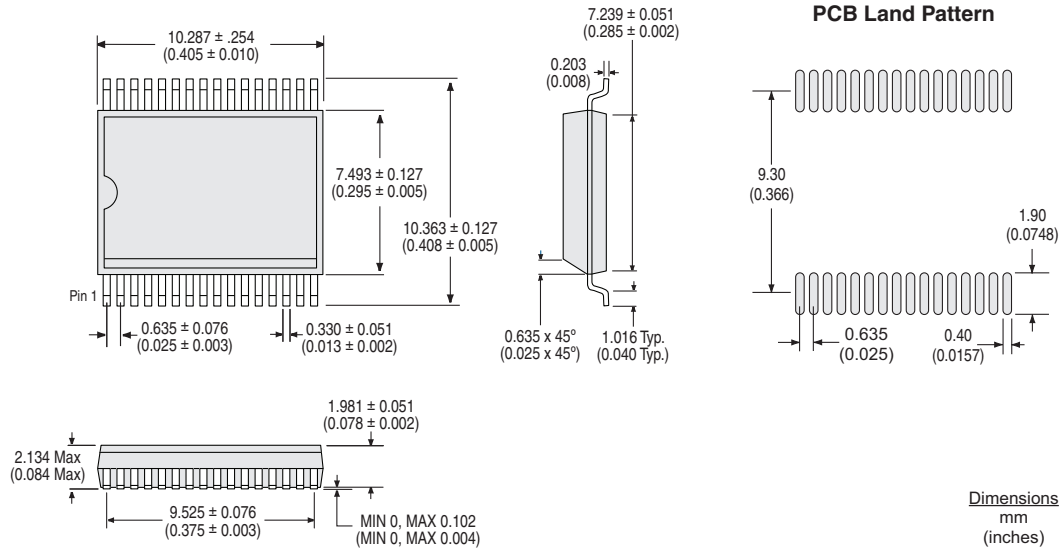
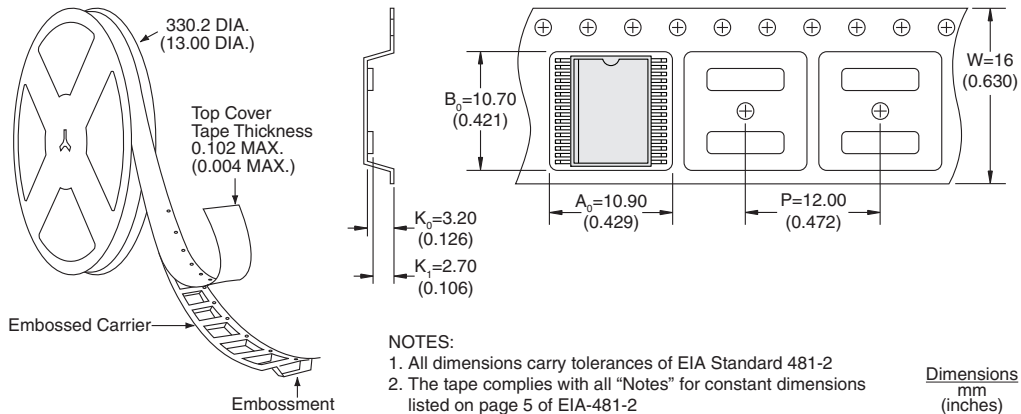


Figure 16. CPC5622ATR Tape and Reel Dimensions



For additional information please visit www.ixysic.com

IXYS Integrated Circuits Division makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses nor indemnity are expressed or implied. Except as set forth in IXYS Integrated Circuits Division's Standard Terms and Conditions of Sale, IXYS Integrated Circuits Division assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

The products described in this document are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of IXYS Integrated Circuits Division's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. IXYS Integrated Circuits Division reserves the right to discontinue or make changes to its products at any time without notice.

Specification: DS-CPC5622-R03
 Copyright © 2012, IXYS Integrated Circuits Division
 LITELINK® is a registered trademark of IXYS Integrated Circuits Division
 All rights reserved. Printed in USA.
 12/22/2012