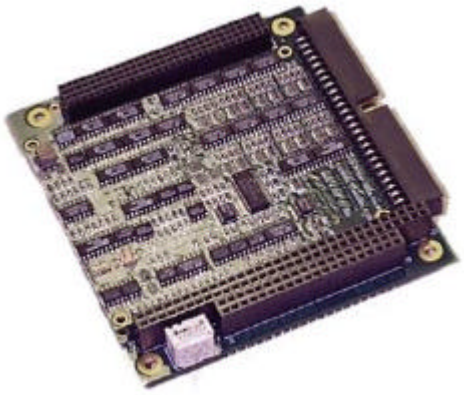
General Standards Corporation

High Performance Bus Interface Solutions

PC104P-16AIO

16-Bit Analog Input/Output PC104-Plus Board

With 32 Input Channels and 4 Output Channels



Features Include:

- 32 Single-Ended or 16 Differential 16-Bit Scanned Analog Input Channels
- 4 Analog Output Channels, 16-Bit D/A Converter per Channel
- Software-Selectable Analog Input/Output Ranges of ±10V, ±5V or ±2.5V
- Independent 32K-Sample Analog Input and Output FIFO Buffers?
- 300K Samples per Second Aggregate Analog Input Sample Rate
- Multiple-Channel and Single-Channel Input Scanning Modes
- Low Crosstalk, Noise and Input Bias Current; Buffer Amplifiers on all Analog Input Lines
- 300K Samples per Second per Channel Analog Output Clocking Rate (1200 KSPS Aggregate Rate)
- Supports Waveform and Arbitrary Function Generation; Continuous and One-shot Modes
- Internal Rate Generator Controls Input Sampling, Output Sampling, or Both Simultaneously
- Supports Multiboard Synchronization of Analog Inputs and Outputs
- Internal Auto calibration of Analog Input and Output Channels
- Continuous and Burst (One-Shot) Input and Output Modes
- DMA Engine Minimizes Host I/O Overhead

Applications:

- ❑ Data Acquisition Systems
- ❑ Industrial Robotics
- ❑ Precision Voltage Sourcing and Measurement
- ❑ Automatic Test Equipment
- ❑ Function and Waveform Generation
- ❑ Research Instrumentation

PRELIMINARY

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Functional Description:

The PMC-16AIO board provides cost effective high-speed 16-bit analog input/output resources in a standard PC104-Plus module. Four analog output channels can be updated either synchronously or asynchronously, and support waveform generation. Internal autocalibration networks permit calibration of all analog input and output channels to be performed without removing the board from the system. Software-controlled test configurations include a loopback mode for monitoring all analog output channels. Gain and offset correction of the analog input and output channels is performed by calibration DAC's that are loaded with channel correction values during autocalibration. Trigger input and output connections support external triggering and multiboard synchronization.

The analog inputs are software-configurable either as 32 single-ended channels or as 16 differential signal pairs. Buffer amplifiers on all input lines eliminate multiplexer input switching noise, and minimize crosstalk and input bias currents. Analog input data accumulates in a 32K-sample buffer until retrieved by the PCI bus. Each of the four analog output channels contains a dedicated 16-bit D/A converter and an output range control network. The board receives analog output data from the PCI bus through a 32K-sample FIFO buffer.

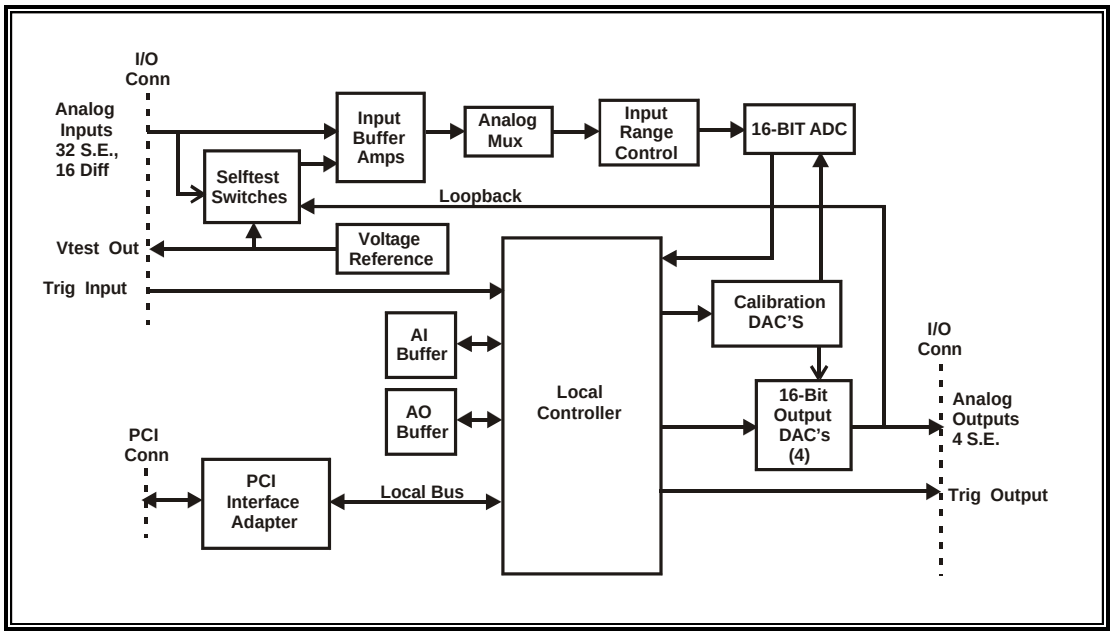

Figure 1. PMC-16AIO; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and the PC/104-Plus Specification, Version 1.1. System input/output connections are made at the panel bracket through a standard 50-pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

ANALOG INPUT CHANNELS

- **Input Characteristics:**

Configuration:	32 input lines, configurable as 32 single-ended or 16 differential channels
Voltage Ranges:	Software configurable as ±10, ±5 or ±2.5 Volts
Input Impedance:	1.0 Megohms line-to-ground, 2.0 Megohms line-to-line, in parallel with 100Pfd. Independent of scan rate.
Bias Current:	80 nanoamps maximum
Noise:	3.0 LSB-RMS typical
Common Mode Rejection:	60 dB typical, DC-60 Hz, differential input mode
Common Mode Range:	±10 Volts; differential input configuration
Overvoltage Protection:	Standard: ±30 Volts with power applied; ±15 Volts with power removed

- **Transfer Characteristics:**

Resolution:	16 Bits; 0.0015 percent of FSR
Maximum Conversion Rate:	300K conversions per second, minimum
Channels per scan:	2, 4, 8, 16, or 32 Channels per scan (32 channels available only in single-ended mode)
Maximum Scan Rate:	75K scans per second in multiple-channel mode. 150 KSPS in 2-Channel mode. 300KSPS in single-channel mode. Scan rate equals the conversion rate divided by the number of channels per scan.
Minimum Scan Rate:	400 scans per second, using a single internal rate generator; 0.007SPS using both generators. Zero, using a software sync flag or an externally supplied sync input.

DC Accuracy:
(Maximum composite error, referred to inputs)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±3.2mV	±4.2mV
±5V	±2.3mV	±2.8mV
±2.5V	±1.6mV	±2.0mV

Crosstalk Rejection:	85dB, DC-10kHz
Integral Nonlinearity:	±0.003 percent of FSR, maximum
Differential Nonlinearity:	±0.0015 percent of FSR, maximum

- **Analog Input Operating Modes and Controls**

Analog Input Modes:	Single Scan:	A software or hardware sync initiates a single scan of all active channels at the maximum conversion rate. As many as three target boards can be synchronized to a single initiator board.

	Continuous Scan:	Inputs are scanned continuously at the selected scan rate.
	Selftest:	Reference and loopback tests; autocalibration
	Multiple-Channel:	4, 8, 16 or 32 channels per scan
	Single-Channel:	Any single channel can be selected for digitizing at the maximum conversion rate.
	Two-Channel:	2-Channel scan size.
Input Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported	

ANALOG OUTPUT CHANNELS

- **Output Characteristics:**

Configuration:	Four single-ended output channels. (Ordering option)
Voltage Ranges:	Same as selected for analog inputs; ±10, ±5 or ±2.5 Volts
Output Resistance:	1.0 Ohm, maximum
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to ±5ma per individual channel
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	5 nV-Sec typical, ±2.5V range

- **Transfer Characteristics:**

Resolution:	16 Bits (0.0015 percent of FSR)
Output Sample Rate:	Software adjustable from 400SPS to 300KSPS per channel; 0.006SPS to 300KSPS using both internal rate generators. DC to 300KSPS with hardware or software sync.

DC Accuracy: (Maximum composite error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±2.7mV	±3.0mV
±5V	±1.9mV	±2.2mV
±2.5V	±1.3mV	±1.7mV

Settling Time:	8us to 1LSB, typical with 50-percent fullscale step
Crosstalk Rejection:	85 dB minimum, DC-1000Hz
Integral Nonlinearity:	±0.004 percent of FSR, maximum
Differential Nonlinearity:	±0.0015 percent of FSR, maximum

- **Analog Output Operating Modes and Controls**

Clocking Modes: Simultaneous Continuous Mode: Channel values in a designated channel group are stored in an intermediate buffer, and then are transferred to the output DAC's when an output clock occurs. The clock can be generated either by the internal rate generator, by a software flag, or by an external hardware trigger. As many as three target boards can be clock-synchronized to a single initiator board.

Simultaneous Burst Mode: A single function (i.e.: burst) is initiated by a software or hardware sync. During a burst, channel values in a designated channel group are stored in a transfer buffer, and then are transferred to the output DAC's each time a clock pulse is generated by the internal rate generator. The burst terminates when a Burst End flag is encountered

Channel-Sequential Modes: Same as simultaneous modes, except each value in the data buffer is written immediately to the associated output DAC. The group-end flag is ignored in this mode.

Channel Assignment:	A 2-bit field in the output buffer assigns the associated data field to a specific output channel.
Group End:	A single bit in the output buffer indicates the last value in a channel group.
Burst End:	A single bit in the output buffer indicates the last value in an output burst sequence.
Output Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported

RATE GENERATORS

Analog outputs and inputs can be clocked from either of two independent rate generators, or both inputs and outputs can be synchronized to a single generator. Each rate generator uses a 16-bit adjustable frequency divider, and the two generators can be operated in series to provide very low clocking rates.

PCI INTERFACE

- **Compatibility:** Conforms to PCI Specification 2.2, with D32 read/write transactions.
  Supports "plug-n-play" initialization.
  Providessingle multifunction interrupt.
  Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

- **Power Requirements**

+5VDC ±0.2 VDC at 1.0 Amps, maximum, 1.1 Amps typical
Power Dissipation: 7.0 Watts maximum; 5.5 Watts typical

- **Physical Characteristics** (Overall, excluding spacers)**:**

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in)

- **Environmental Specifications**

Ambient Temperature Range:	Operating: 0 to +70 degrees Celsius * Storage: -40 to +85 degrees Celsius
	*Temperature of inlet cooling air.
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A", as indicated below. For example, model number PC104P-16AIO-4 describes a board with 4 output channels.

Optional Parameter	Value	Specify Option As:
Number of Analog Outputs	No Output Channels	A = 0
	4 Output Channels	A = 4

SYSTEM I/O CONNECTIONS

Table 1. System I/O Connector Pin Functions

PIN	FUNCTION	PIN	FUNCTION
1	INPUT RTN	26	ANA INP 22 LO
2	INPUT RTN	27	ANA INP 24 HI
3	ANA INP 00 HI	28	ANA INP 24 LO
4	ANA INP 00 LO	29	ANA INP 26 HI
5	ANA INP 02 HI	30	ANA INP 26 LO
6	ANA INP 02 LO	31	ANA INP 28 HI
7	ANA INP 04 HI	32	ANA INP 28 LO
8	ANA INP 04 LO	33	ANA INP 30 HI
9	ANA INP 06 HI	34	ANA INP 30 LO
10	ANA INP 06 LO	35	ANA OUT 03
11	ANA INP 08 HI	36	ANA OUT 02
12	ANA INP 08 LO	37	ANA OUT 01
13	ANA INP 10 HI	38	ANA OUT 00
14	ANA INP 10 LO	39	VTEST
15	ANA INP 12 HI	40	OUTPUT RTN
16	ANA INP 12 LO	41	TRIG OUT
17	ANA INP 14 HI	42	N/C
18	ANA INP 14 LO	43	N/C
19	ANA INP 16 HI	44	N/C
20	ANA INP 16 LO	45	TRIG IN
21	ANA INP 18 HI	46	N/C
22	ANA INP 18 LO	47	N/C
23	ANA INP 20 HI	48	N/C
24	ANA INP 20 LO	49	+5VDC
25	ANA INP 22 HI	50	DIGITAL RTN

* Analog inputs are shown for the differential input mode. In single-ended mode, LO inputs become consecutive odd-numbered channels, beginning with ANA INP 01 replacing ANA INP 00 LO.

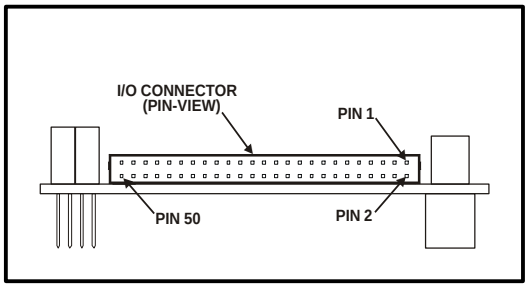

Figure 2. System Input/Output Connector

System Mating Connector:
Polarized 50-Pin socket connector:
AMP #1-746288-0,
with strain-relief #499252-4.

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