2.5” SATA-SSD Datasheet

CONTENTS

Revision History

Rev.	Date	History
0.1	2009/10/14	1. 1st draft
0.2	2009/10/21	1. Revise specification
0.3	2009/11/19	1. Revise specification
0.4	2009/12/17	1. Create 8GB LBA data
0.5	2010/4/21	1. Add 4GB SLC SSD

1. Overview

Advantech SQFlash 2.5" SATA-SSD (Solid State Drive) delivers all the advantages of Flash Disk technology with the Serial ATA II interface, fully compliant with standard 2.5-inch form factor. SATA Drives are replacing the older and slower (PATA) interface in embedded environments.

The SATA SSD is based on a standard 7-pin interface for data segment and 15-pin for power segment, designed to operate at a maximum operating frequency of 150MHz with 30MHz external crystal. Its capacity could provide a wide range from 8GB to up to 256GB. Also it can reach 220MB/s read as well as 160MB/s write high performance based on MLC flash (with 64MB DDR enabled and measured by CrystalDiskMark v2.1). The power consumption of Flash Disk is much lower than traditional Hard Drive. In addition, Advantech SQFlash 2.5" SATA-SSD provides hot-swapping abilities when removing, replacing or upgrading flash disks.

2. Features

- **Standard SATA interface**
  - Support SATA 1.5 Gbps and 3.0 Gbps interface
  - SATA Revision 2.6 compliant
  - Power management supported
- **Operating Voltage：5.0V**
- **Support 48/32/28 bit ECC correct per 2K Byte data**
- **Capacities**
  - SLC type：4GB，8GB，16GB，32GB，64GB
  - MLC type：16GB，32GB，64GB，128GB，256GB
- **Performance**
  - SLC type
    - Sustain Read Speed up to 210 MB/s
    - Sustain Write Speed up to 200 MB/s
  - MLC type
    - Sustain Read Speed up to 220 MB/s
    - Sustain Write Speed up to 160 MB/s
- **Temperature Ranges**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage
  - Industrial Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage
- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：5% ~ 95% under 55℃
- **Endurance**
  - > 2,000,000 program/erase cycles
- **MTBF**
  - 2,000,000 hours
- **Data Retention**
  - 10 years
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：100 mm x 69.85 mm x 9.5 mm**

3. General Description

Advanced NAND Flash Controller

Advantech SQFlash 2.5" SATA-SSD includes Bad Block Management Algorithm, Wear Leveling Algorithm and Error Detection / Correction Code (EDC/ECC) Algorithm.

Bad Block Management

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash 2.5" SATA-SSD implement an efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

Wear Leveling

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash 2.5" SATA-SSD provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

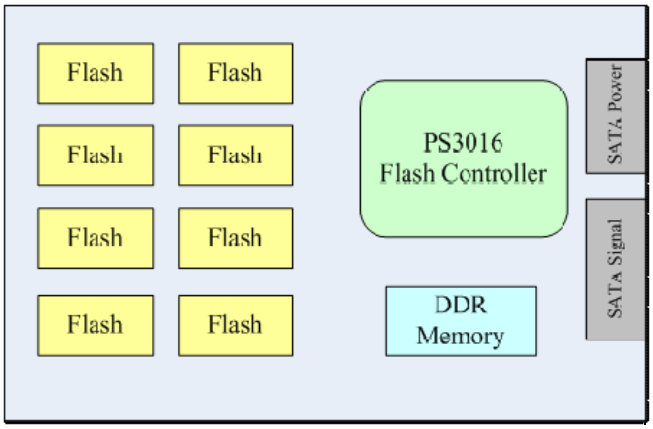
Error Detection / Correction

Advantech SQFlash 2.5" SATA-SSD utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. This algorithm can support 48/32/28 bit ECC correct per 2K Byte data.

Sophisticate Product Management Systems

Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

■ Block Diagram



■ LBA、Cylinders、Heads、Sectors value for SLC type

Density	LBA (K bytes)	Cylinders	Heads	Sectors
4 GB	7,863,912	15,603	16	63
8 GB	15,727,824	15,603	16	63
16 GB	31,587,696	16,383	16	63
32 GB	64,323,504	16,383	16	63
64 GB	129,760,848	16,383	16	63

■ LBA、Cylinders、Heads、Sectors value for MLC type

Density	LBA (K bytes)	Cylinders	Heads	Sectors
16 GB	30,080,736	16,383	16	63
32 GB	60,292,512	16,383	16	63
64 GB	124,780,320	16,383	16	63
128 GB	253,891,646	16,383	16	63
256 GB	508,952,304	16,383	16	63

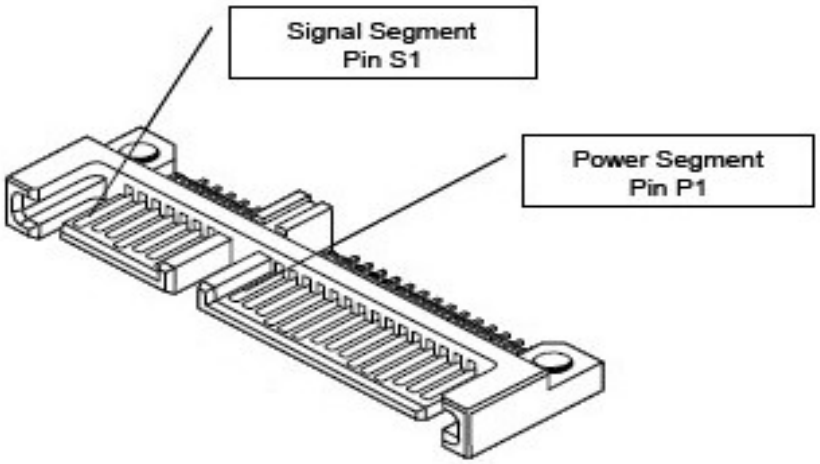
4. Pin Assignment and Description

4.1 2.5" SATA-SSD Interface Pin Assignments (Signal Segment)

Pin #	Function	Description
S1	GND	2nd mate
S2	A+	Differential signal pair A
S3	A-	
S4	GND	2nd mate
S5	B-	Differential signal pair B
S6	B+	
S7	GND	2nd mate

4.2 2.5" SATA-SSD Interface Pin Assignments (Power Segment)

Pin #	Function
P1	Not Used (3.3V)
P2	Not Used (3.3V)
P3	Not Used (3.3V Pre-Charge)
P4	GND
P5	GND
P6	GND
P7	5V Pre-Charge
P8	5V
P9	5V
P10	GND
P11	RESERVED
P12	GND
P13	Not Used (12V Pre-Charge)
P14	Not Used (12V)
P15	Not Used (12V)



5. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

Word Address	F：Fixed V：Variable X：Both	Default Value	Data Field Type Information
0	F	045Ah	General configuration bit-significant information
1	X	3FFFh	Obsolete – Number of logical cylinders (16383)
2	V	0h	Specific configuration
3	X	0010h	Obsolete – Number of logical heads (16)
4-5	X	02007E00h	Retired
6	X	003Fh	Obsolete – Number of logical sectors per logical track (63)
7 - 8	V	0h	Reserved for assignment by the Compact Flash Association
9	X	0h	Retired
10 - 19	F	Varies	Serial number (20 ASCII characters)
20 - 21	X	0h	Retired
22	X	0h	Obsolete
23 - 26	F	Varies	Firmware revision (8 ASCII characters)
27 - 46	F	Varies	Model number (xxxxxxxx)
47	F	8001h	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	0h	Reserved
49	F	0F00h	Capabilities
50	F	4000h	Capabilities
51 - 52	X	00000200h	Obsoleted
53	F	0007h	Words 88 and 70:64 valid
54	X	3FFFh	Obsolete – Number of logical cylinders (16383)
55	X	0010h	Obsolete – Number of logical heads (16)
56	X	003Fh	Obsolete – Number of logical sectors per track (63)
57 - 58	X	00FBFC10h	Obsolete
59	F	0100h	Number of sectors transferred per interrupt on MULTIPLE commands
60 - 61	F	037DFF40h (32G) xxxxxxxxh (64G)	Total number of user addressable sectors
62	X	0h	Obsolete
63	F	0007h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Manufacturer's recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69 - 70	F	0h	Reserved
71 - 74	F	0h	Reserved for the IDENTIFY PACKET DEVICE command
75	F	0h	Queue depth
76	F	0002h	Serial SATA capabilities
77	F	0h	Reserved for future Serial ATA definition
78	F	0h	Serial ATA features supported
79	V	0H	Serial ATA features enabled
80	F	00F8h	Major Version Number
81	F	0021h	Minor Version Number
82	F	7429h	Command set supported

Word Address	F：Fixed V：Variable X：Both	Default Value	Data Field Type Information
83	F	7008h	Command set supported
84	F	4000h	Command set/feature supported extension
85	V	7028h	Command set/feature enabled
86	V	3000h	Command set/feature enabled
87	V	4000h	Command set/feature default
88	V	007Fh	Ultra DMA Modes
89	F	0h	Time required for security erase unit completion
90	F	0h	Time required for Enhanced security erase completion
91	V	0h	Current advanced power management value
92	V	0h	Master Password Revision Code
93	F	0h	Hardware reset result. The contents of the bits (12:0) of this word shall change only during the executeion of s hardware reset.
94	V	0h	Vebdor's recommended and actual acoustic management value
95	F	0h	Stream Minimum Request Size
96	V	0h	Streaming Transfer Time – DMA
97	V	0h	Streaming Access Latency – DMA and PIO
98 - 99	F	0h	Streaming Performance Granularity
100 - 103	V	xxxxxxxxh (32G) xxxxxxxxh (64G) xxxxxxxxh (128G) xxxxxxxxh (256G)	Maximum user LBA for 48 bit Address feature set
104	V	0h	Streaming Transfer Time – PIO
105	F	0h	Reserved
106	F	0h	Physical sector size / Logical sector size
107	F	0h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108 - 111	F	0h	Unique ID
112 - 115	F	0h	Reserved
116	V	0h	Reserved
117 - 118	F	0h	Words per logical Sector
119	F	0h	Supported settings
120	F	0h	Command set/Feature Enabled/Supported
121 - 126	F	0h	Reserved
127	F	0h	Removable Media Status Notification feature set support
128	V	0h	Security status
129 - 159	X	0h	Vendor specific
160	F	0h	Compact Flash Association (CFA) power mode 1
161 - 175	X	0h	Reserved for assignment by the CFA
176 - 205	V	0h	Current media serial number
206 - 216	F	0h	Reserved
217	F	0h	Non-rotating media device
218 - 221	F	0h	Reserved
222	F	0h	Reserved
223 - 233	F	0h	Reserved
234		0h	Reserved
235		0h	Reserved
236 - 254	F	0h	Reserved
255	X	Varies	Integrity word (Checksum and Signature)

6. ATA Command Set

[Command Set List]

No.	Command set	Code	Protocol	Argument
1	CHECK POWER MODE	98h,E5h	ND	28-bit
2	DOWNLOAD MICROCODE	92h	PO	28-bit
3	EXECUTE DEVICE DIAGNOSTIC	90h	DD	28-bit
4	FLUSH CACHE	E7h	ND	28-bit
5	FLUSH CACHE EXT	EAh	ND	28-bit
6	IDENTIFY DEVICE	ECh	PI	28-bit
7	IDLE	97h,E3h	ND	28-bit
8	IDLE IMMEDIATE	95h,E1h	ND	28-bit
9	INITIALIZE DEVICE PARAMETERS	91h	ND	28-bit
10	NOP	00h	ND	28-bit
11	READ BUFFER	E4h	PI	28-bit
12	READ DMA	C8h,C9h	DM	28-bit
13	READ DMA EXT	25h	DM	48-bit
14	READ MULTIPLE	C4h	PI	28-bit
15	READ MULTIPLE EXT	29h	PI	48-bit
16	READ NATIVE MAX ADDRESS	F8h	ND	28-bit
17	READ NATIVE MAX ADDRESS EXT	27h	ND	48-bit
18	READ SECTOR(S)	20h,	PI	28-bit
19	READ SECTOR(S) EXT	24h	PI	48-bit
20	READ VERIFY SECTOR(S)	40h,41h	ND	28-bit
21	READ VERIFY EXT	42h	ND	48-bit
22	RECALIBRATE	1Xh	ND	28-bit
23	SECURITY DISABLE PASSWORD	F6h	PO	28-bit
24	SECURITY ERASE PREPARE	F3h	ND	28-bit
25	SECURITY ERASE UNIT	F4h	PO	28-bit
26	SECURITY FREEZE	F5h	ND	28-bit
27	SECURITY SET PASSWORD	F1h	PO	28-bit
28	SECURITY UNLOCK	F2h	PO	28-bit
29	SEEK	7Xh	ND	28-bit
30	SET MAX ADDRESS	F9h	ND	28-bit
31	SET MAX ADDRESS EXT	37h	ND	48-bit
32	SET FEATURE	EFh	ND	28-bit
33	SET MULTIPLE	C6h	ND	28-bit
34	SLEEP	99h,E6h	ND	28-bit
35	SMART READ DATA	B0h		
36	SMART ENABLE/DISABLE AUTO SAVE	B0h		
37	SMART EXECUTE OFF-LINE	B0h		
38	SMART READ LOG	B0h		
39	SMART ENABLE OPERATION	B0h		
40	SMART DISABLE OPERATION	B0h		
41	SMART RETURN STATUS	B0h		
42	STANDBY	96h,E2h	ND	28-bit
43	STANDBY IMMEDIATE	94h,E0h	ND	28-bit
44	WRITE BUFFER	E8h	PO	28-bit
45	WRITE DMA	CAh,CBh	DM	28-bit
46	WRITE DMA EXT	35h	DM	48-bit
47	WRITE MULTIPLE	C5h	PO	28-bit

No.	Command set	Code	Protocol	Argument
48	WRITE MULTIPLE EXT	39h	PO	48-bit
49	WRITE SECTOR(S)	30h	PO	28-bit
50	WRITE SECTOR(S) EXT	34h	PO	48-bit
51	WRITE SECTOR(S) W/O ERASE	38h	PO	28-bit
52	WRITE VERIFY	3Ch	PO	28-bit

Note: ND = Non-Data Command
PI = PIO Data-In Command
PO = PIO Data-Out Command
DM = DMA Command
DD = Execute Diagnostic Command

[Command Set Descriptions]

1. CHECK POWER MODE (code: 98h or E5h);
This command allow host to determine the current power mode of the device.

2. DOWNLOAD MICROCODE (code: 92h);
This command enable the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.
All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the content of the LBA Low register and the Sector Count register.
This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512bytes increments.

3. EXECUTE DEVICE DIAGNOSTIC (code: 90h);
This command performs the internal diagnostic tests implemented by the module.

4. FLUSH CACHE (code: E7h);
This command used by the host to request the device to flush the write cache.

5. FLUSH CACHE EXT (code: EAh);
This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media.

6. IDENTIFY DEVICE (code: ECh);
The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

7. IDLE (code: 97h or E3h);
This command allows the host to place the module in the IDLE mode and also set the Standby timer. INTRQ may be asserted even through the module may not have fully transitioned to IDLE mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

8. IDLE IMMEDIATE (code: 95h or E1h);
This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

9. INITIALIZE DEVICE PARAMETERS (code: 91h);
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

10. NOP (code: 00h);
If this command is issued, the module respond with command aborted.

11. READ BUFFER (code: E4h);
This command enables the host to read the current contents of the module's sector buffer.

12. READ DMA (code: C8h or C9h);
This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

13. READ DMA Ext (code: 25h);
This command allows the host to read data using the DMA data transfer protocol.

14. READ MULTIPLE (code: C4h);

This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sector per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

15. READ MULTIPLE EXT (code: 29h);

This command performs similarly to the READ SECTORS command. The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits (7:0) in word 47 in the IDENTIFY DEVICE information.

16. READ NATIVE MAX ADDRESS (code: F8h);

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition.

17. READ NATIVE MAX ADDRESS EXT (code: 27h);

This command returns the native maximum address.

18. READ SECTOR(S) (code: 20h or 21h);

This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

19. READ SECTOR(S) EXT (code: 24h);

This command reads from "1" to "65536" sectors as specified in the Sector Count register. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

20. READ VERIFY SECTOR(S) (code: 40h or 41h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

21. READ VERIFY SECTOR(S) EXT (code: 42h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

22. RECALIBRATE (code: 1xh);

This command return value is select address mode by the host request.

23. SECURITY DISABLE PASSWORD (code: F6h);

This command transfers 512 bytes of data from the host. Table defines the content of this information. If the password selected by word 0 match the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password is set.

24. SECURITY ERASE PREPARE (code: F3h);

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device eraseing and unlocking.

25. SECURITY ERASE UNIT (code: F4h);

This command transfer 512 bytes of data from the host. Table## defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command.

26. SECURITY FREEZE LOCK (code: F5h);

This command shall set the device to frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen shall be disabled by power-off or hardware reset.
If SECURITY FREEZE LOCK is issued when the drive is in frozen mode, the drive executes the command and remains in frozen mode.

27. SECURITY SET PASSWORD (code: F1h);

This command transfer 512 bytes of data from the host. Table defines the content of this information. The data transferred controls the function of this command. Table defines the interaction of the identifier and security level bits.

28. SECURITY UNLOCK (code: F2h);

This command transfer 512 bytes of data from the host. Table (as Disable Password) defines the content of this information.
If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.
If the identifier bit is set to user then the device shall compare the supplied password with the stored User password.
If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall be decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reachs zero then SECURITY UNLOCK and SECURITY ERASE UNIT command shall be aborted unitl a power-on or a hardware reset.

29. SEEK (code: 7Xh);

This command performs address range check.

30. SET FEATURE (code: EFh);

This command is used by the host to establish parameters that affect the execution of certain device features.

31. SET MAX ADDRESS (code: F9h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error.
IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

32. SET MAX ADDRESS EXT (code: 37h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error.
IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

33. SET MULTIPLE MODE (code: C6h);

This command enables the device to perform READ and Write Multiple operations and establishes the block count for these commands.

34. SLEEP (code: 99h or E6h);

This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

35. SMART READ DATA (code: B0h with Feature register value of D0h);
This command returns the Device SMART data structure to the host.

36. SMART ENABLE/DISABLE AUTO SAVE (code: B0h with Feature register value of D2h);
This command enables and disables the optional attribute autosave feature of the device.

37. SMART EXECUTE OFF_LINE (code: B0h with Feature register value of D4h);
This command cause the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

38. SMART READ LOG (code: B0h with Feature register value of D5h);
This command returns the specified log data to the host.

39. SMART ENABLE OPERATION (code: B0h with Feature register value of D8h);
This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device.

40. SMART DISABLE OPERATION (code: B0h with Feature register value of D9h);
This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations.
After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATION commands, with exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

41. SMART RETURN STATUS (code: B0h with Feature register value of DAh);
This command cause the device to communicate the reliability status of the device to the host.

42. STANDBY (code: 96h or E2h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

43. STANDBY IMMEDIATE (code: 94h or E0h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

44. WRITE BUFFER (code: E8h);
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

45. WRITR DMA (code: CAh or CBh);
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

46. WRITR DMA EXT (code: 35h);
This command writes from "1" to "65536" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

47. WRITE MULTIPLE (code: C5h);
This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

48. WRITE MULTIPLE EXT (code: 39h);

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

49. WRITE SECTOR(S) (code: 30h or 31h);

This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

50. WRITE SECTOR(S) EXT (code: 34h);

This command writes from "1" to "65536" sectors as specified in the Sector Count register. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

51. WRITE SECTOR(S) W/O ERASE (code: 38h);

This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

52. WRITE VERIFY (code: 3Ch);

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

7. System Power Consumption

7.1 Supply Voltage

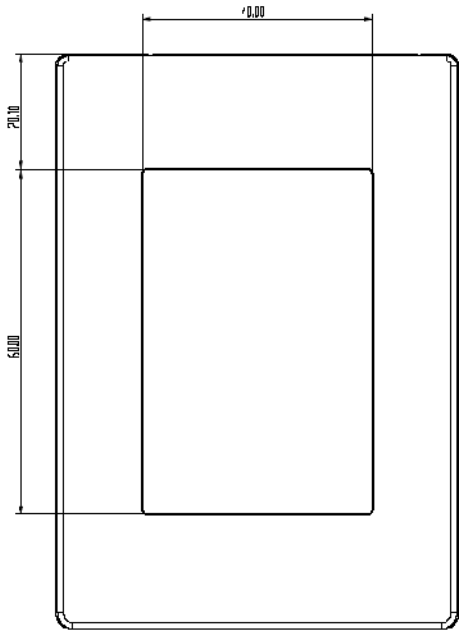
Parameter	Rating
Operating Voltage	5V +/- 5%
Max. Ripple	100mV, 0~30MHz

7.2 Power Consumption

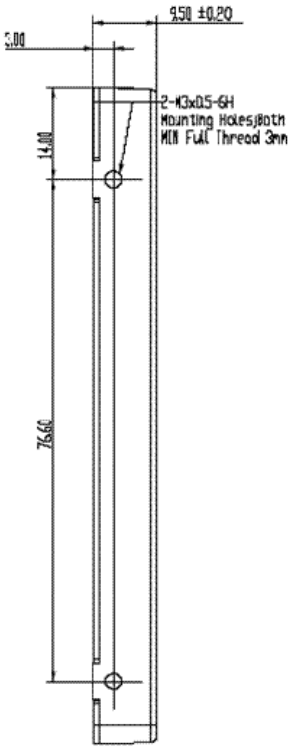
Parameter	Value
Standby	0.5W
Operating	5.3W

8. Physical Dimension

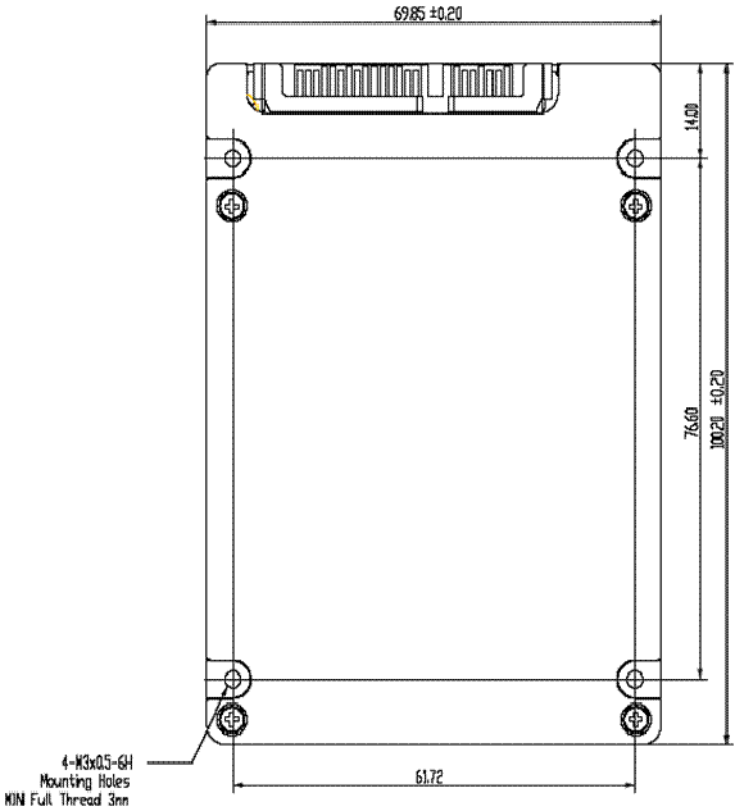
2.5" SATA SSD (Unit: mm)



(Top View)



(Side View)



(Bottom View)

Appendix: Part Number Table

Product	Advantech PN	Manufacture PN
Advantech SQFlash 2.5" SATA SSD 4G SLC, DMA (0~70°C)	SQF-S25S4-4G-CTE	SSB004GTSC0-S30
Advantech SQFlash 2.5" SATA SSD 8G SLC, DMA (0~70°C)	SQF-S25S4-8G-CTE	SSB008GTSC0-S30
Advantech SQFlash 2.5" SATA SSD 16G SLC, DMA (0~70°C)	SQF-S25S8-16G-CTE	SSB016GTSC0-S30
Advantech SQFlash 2.5" SATA SSD 32G SLC, DMA (0~70°C)	SQF-S25S8-32G-CTE	SSB032GTSC0-S30
Advantech SQFlash 2.5" SATA SSD 64G SLC, DMA (0~70°C)	SQF-S25S8-64G-CTE	SSB064GTSC0-S30
Advantech SQFlash 2.5" SATA SSD 4G SLC, DMA (-40~85°C)	SQF-S25S4-4G-ETE	SSB004GTSE0-S30
Advantech SQFlash 2.5" SATA SSD 8G SLC, DMA (-40~85°C)	SQF-S25S4-8G-ETE	SSB008GTSE0-S30
Advantech SQFlash 2.5" SATA SSD 16G SLC, DMA (-40~85°C)	SQF-S25S8-16G-ETE	SSB016GTSE0-S30
Advantech SQFlash 2.5" SATA SSD 32G SLC, DMA (-40~85°C)	SQF-S25S8-32G-ETE	SSB032GTSE0-S30
Advantech SQFlash 2.5" SATA SSD 64G SLC, DMA (-40~85°C)	SQF-S25S8-64G-ETE	SSB064GTSE0-S30
Advantech SQFlash 2.5" SATA SSD 16G MLC, DMA (0~70°C)	SQF-S25M4-16G-CTE	SSB016GTMC0-S30
Advantech SQFlash 2.5" SATA SSD 32G MLC, DMA (0~70°C)	SQF-S25M8-32G-CTE	SSB032GTMC0-S30
Advantech SQFlash 2.5" SATA SSD 64G MLC, DMA (0~70°C)	SQF-S25M8-64G-CTE	SSB064GTMC0-S30
Advantech SQFlash 2.5" SATA SSD 128G MLC, DMA (0~70°C)	SQF-S25M8-128G-CTE	SSB128GTMC0-S30
Advantech SQFlash 2.5" SATA SSD 256G MLC, DMA (0~70°C)	SQF-S25M8-256G-CTE	SSB256GTMC0-S30
Advantech SQFlash 2.5" SATA SSD 16G MLC, DMA (-40~85°C)	SQF-S25M4-16G-ETE	SSB016GTME0-S30
Advantech SQFlash 2.5" SATA SSD 32G MLC, DMA (-40~85°C)	SQF-S25M8-32G-ETE	SSB032GTME0-S30
Advantech SQFlash 2.5" SATA SSD 64G MLC, DMA (-40~85°C)	SQF-S25M8-64G-ETE	SSB064GTME0-S30
Advantech SQFlash 2.5" SATA SSD 128G MLC, DMA (-40~85°C)	SQF-S25M8-128G-ETE	SSB128GTME0-S30
Advantech SQFlash 2.5" SATA SSD 256G MLC, DMA (-40~85°C)	SQF-S25M8-256G-ETE	SSB256GTME0-S30