X5-G12

V 1.2 11/8/10

Innovative Integration
... real time solutions!

PCI Express XMC Module with Dual channel 1 GSPS,12-bit Digitizer, Virtex5 FPGA and 512MB Memory

FEATURES

- Two 1 GSPS, 12-bit A/D channels
- 2 GSPS, 12-bit single channel mode
- +/-1V, 50 ohm, AC coupled inputs with simultaneous DC-offset measurement
- Xilinx Virtex5, SX95T or LX155T FPGA
- 512MB DDR2 DRAM
- 4MB QDR-II SRAM
- Integrated FFT engine: 256K point in 3.3 ms
- 8 Rocket IO private links, 2.5 Gbps each
- >1 GB/s, 8-lane PCI Express Host Interface
- Power Management features
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

APPLICATIONS

- Wireless Receiver
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording
- IP development

SOFTWARE

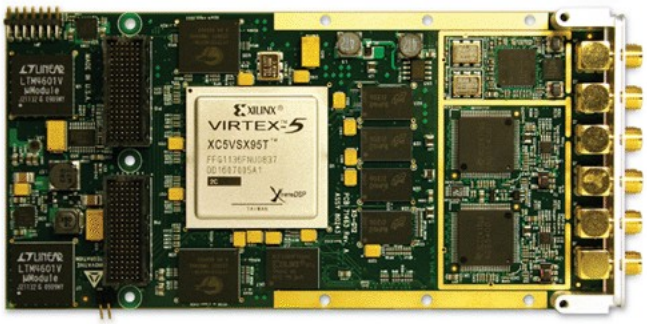
- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

IP Cores

- 16 or 32 independent DDC channels
- 128 or 256 tunable channelizer
- FFT analysis
- PSK and FSK demodulation

MATLAB®

XILINX®



DESCRIPTION

The X5-G12 is an XMC I/O module featuring dual channels of 1 GSPS 12-bit digitizing with a Virtex5 FPGA computing core, DRAM and SRAM memory, and eight lane PCI Express host interface.

A Xilinx Virtex5 SX95T or LX155T with 512 MB DDR2 DRAM and 4MB QDR-II memory provides a very high performance DSP core for demanding applications such RADAR and direct RF digitizing. The close integration of the analog IO, memory and host interface with the FPGA enables real-time signal processing at rates exceeding 300 GMAC/s. High speed spectral analysis is supported with an integrated FFT engine capable of processing 256K point complex FFTs in 3.3 ms.

The X5 XMC modules couple Innovative's powerful Velocia architecture with a high performance, 8-lane PCI Express interface that provides over 1 GB/s sustained transfer rates to the host. Private links to host cards with >1.6 GB/s capacity using P16 are provided for system integration.

The X5 family can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

IP logic cores are also available for SDR applications that provide from 16 to 4096 DDC channels. These IP cores transform the X5 modules into versatile receivers using proven logic cores from R-Interface and Innovative, ready for integration into your application.

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided, including logging A/D samples to disk.

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This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
X5-G12	80243-SX95T2-<ER>	PCI Express XMC module with two channels of 1 GSPS, 12-bit A/Ds, AC-coupled input, simultaneous DC-offset measurement, Virtex5 SX95T -2 speed FPGA, 4MB SRAM, 512MB DRAM. <ER> is the environmental rating L0 through L4. See table below.
X5-G12	80243-LX155T2-<ER>	PCI Express XMC module with two channels of 1 GSPS, 12-bit A/Ds, AC-coupled input, simultaneous DC-offset measurement, Virtex5 LX155T -2 speed FPGA, 4MB SRAM, 512MB DRAM. <ER> is the environmental rating L0 through L4. See table below.
Logic		
X5-G12 FrameWork Logic	55029	X5- GSPS FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables		
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters		
XMC-PCIe x1 Adapter	80172-0	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
XMC- PCIe x8 Adapter	80173-0	PCI Express Carrier card for XMC PCI Express modules, x8 lanes
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
Embedded PC Host		
eInstrumentPC embedded PC XMC host	90200	Embedded PC with support for two XMC modules; Celeron, Core2Duo or Penryn CPU; Windows or Linux
eInstrumentPC-Atom low-power embedded PC XMC host	90201	Embedded PC with support for two XMC modules; Intel Atom or Penryn CPU; Windows or Linux

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Operating Environment Ratings

X5 modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Contact sales support for further information on pricing and availability.

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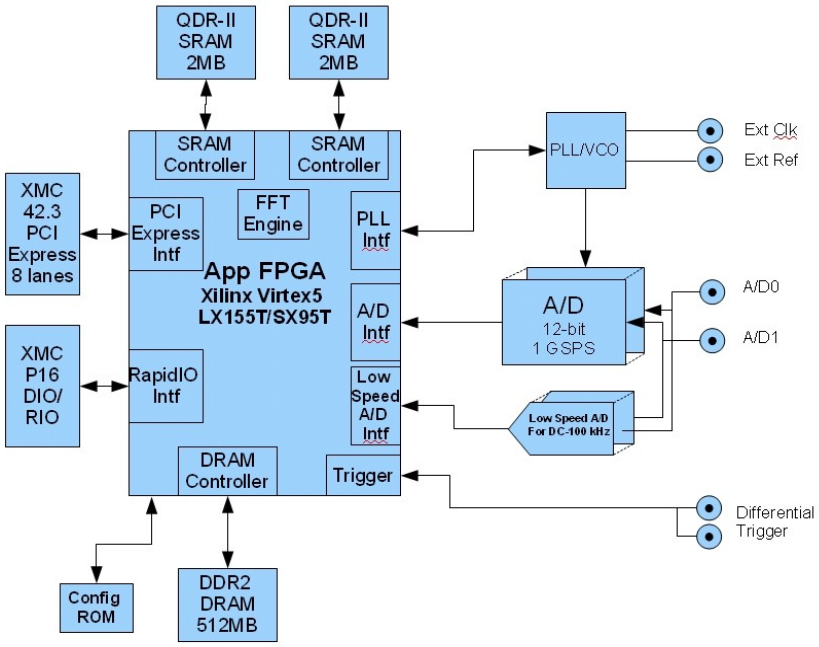
X5-G12 Block Diagram



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Standard Features

Analog	
Inputs	2 or single channel at dual rate
Input Range	+/- 1V
Input Type	Single ended, AC coupled with low frequency DC-100KHz secondary channel
Input Impedance	50 ohm
A/D Resolution	12-bit
A/D Sample Rate	100 to 1000 MHz per channel; may be joined for single channel 2 GSPS mode
Data Format	2's complement, 16-bit integer
Connectors	SMA female
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

FPGA	
Device (2 offered)	Xilinx Virtex5 XC5VSX95T-2FF1136C XC5VLX155T-2FF1136C
Speed Grade	-2 (commercial)
Size	SX95T :~9M gate equivalent LX155T :~15M gate equivalent
Flip-Flops	SX95T: 69120 LX155T : 97280
Multipliers	SX95T: 640 LX155T: 128
Slice	SX95T: 17,280 LX155T: 24,320
Block RAMs	SX95T: 296 (5328 Kbits) LX155T: 212
Rocket IO	16 lanes @ 2.5 Gbps
Configuration	SelectMAP from on-board flash EEPROM - JTAG during development FLASH holds 2 images
FPGA Usage (Framework Logic without FFT)	SX95T: LUT=21% FF=29% BR=26% DSP48E=1% LX155T: LUT=25% FF=21% BR=36% DSP48E=4%

Memories	
DRAM	512MB DDR2 DRAM 4 devices @ 64Mx16 each
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	4.2 GB/s storage/retrieval rate sustained
SRAM Size	4 MB total 2 devices @ 512Kx32 each
SRAM Controller	Two independent SRAM controllers implemented in FPGA logic
SRAM Type	QDR-II
SRAM Rate	1.2 GB/s simultaneous read and write rates, (2.4 GB/s total)

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Host Interface	
Type	PCI Express; 8 lanes
Sustained Data Rate	1 GB/s
Protocol	PCI Express with Velocia packet system
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Source	Programmable PLL: TI CDCE72010, output sample clock rates to 1 GHz
	External: Sine/square 100 MHz to 1 GHz, 0.5-3.3Vp-p (-2 to +14.3 dBm) AC-coupled, 50-ohm terminated. 500 MHz max if used as PLL reference
Jitter	PLL: <200 fs RMS @ 1 GHz External: 30 fs additive, divider = 1, 500 MHz
External Clock Connector	SMA female
Triggering	External, software, acquire N frame
Trigger Connector	SMA female
Trigger Levels	AC-coupled, 50 ohm input impedance, single-ended or differential. LVTTL compatible (0 to 3.3V), LVPECL compatible.
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Acquisition Monitoring	
Alerts	Trigger Start, Trigger Stop, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure
Alert Timestamping	4 ns resolution, 32-bit counter

P16 Digital IO	
Rocket IO Channels	8
Rocket IO data rate	2.5 Gbps/lane (2 Gbps effective rate when 8b/10b encoded)
DIO Bits, total	33
Signal Standard	LVTTL (3.3V)
Drive	+/-12 mA
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables power supplies
Power Control	Channel enables and power up enables
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	135g without heatsink
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Supply Voltage, VPWR to GND	+4.5	+12.5	V	
Analog Input Voltage, Vin+ or Vin- to GND	-5.7	+5.7	V	
Operating Temperature	See Environmental Ratings Table			
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	See Environmental Ratings Table			
Shock	See Environmental Ratings Table			

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	+3.15	+3.3	+3.45	V
Supply Voltage	+11	+12	+13	V
Operating Temperature	0		60	C

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ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Analog Input Bandwidth	1975	MHz	-3dB
SFDR	65.9	dB	100.67 MHz sine input, -3 db FS, 1 GSPS
S/N	58	dB	100.67 MHz sine input, -3 db FS, 1 GSPS
THD	-62.2	dB	100.67 MHz sine input, -3 db FS, 1 GSPS
ENOB	8.7	bits	100.67 MHz sine input, -3 db FS, 1 GSPS
Channel Crosstalk	<-85	dB	Aggressor = 100.67 MHz, 1.9Vp-p adjacent channel
Noise floor	<-90	dB	Grounded input, 64K point FFT
Power Consumption	28	W	All channels sampling at 1000 MSPS, 23C ambient; specific applications may be may vary from 20 to 35W 12V @ 0.7A, 3.3V @ 6.1A
Gain Error	<0.02	% of FS	Calibrated
Offset Error	<5	mV	Calibrated

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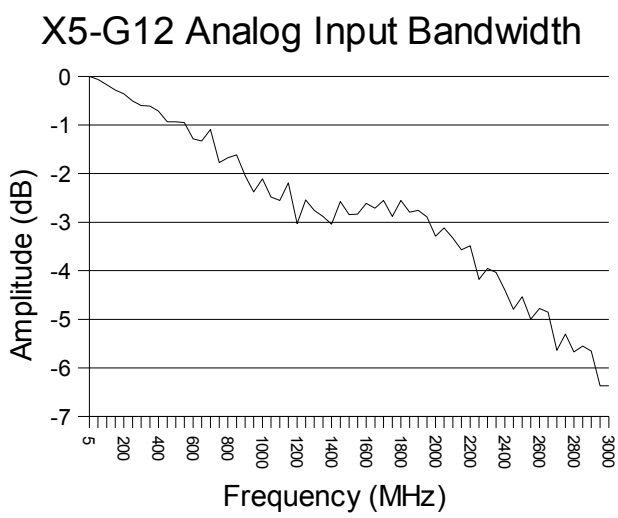
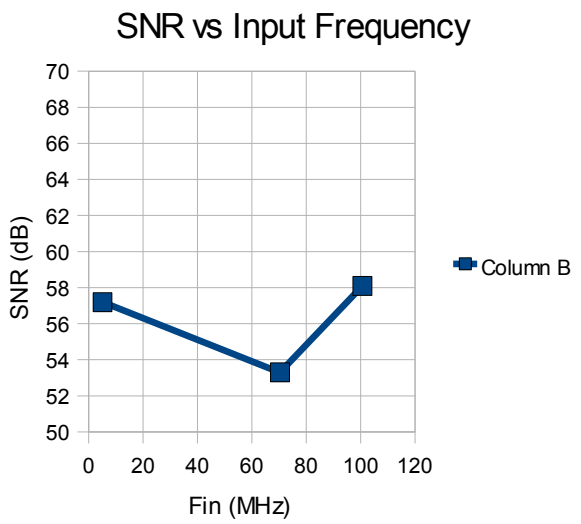


Fs = 1000 MHz, Fin = 1.95Vp-p



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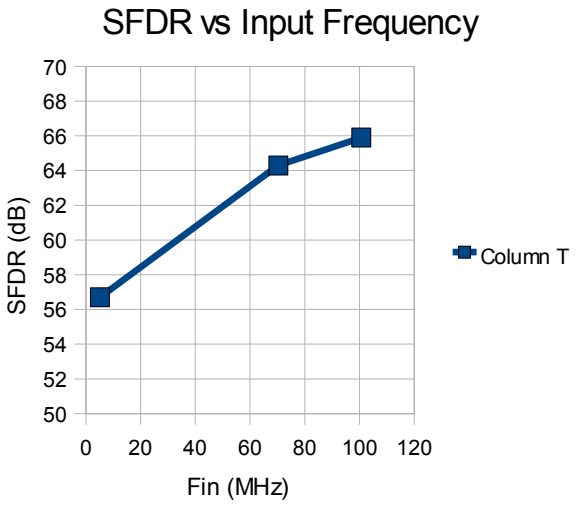

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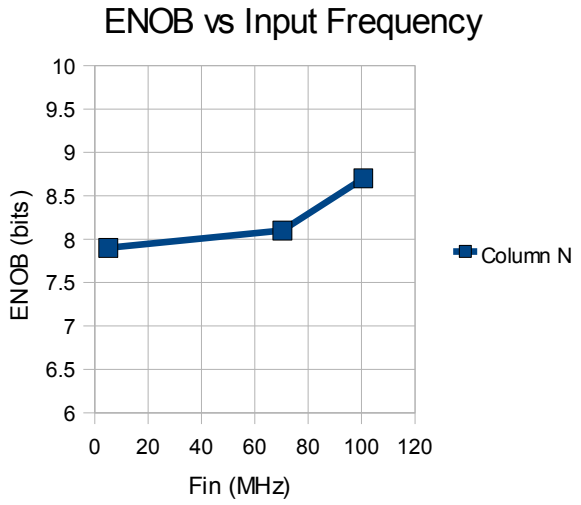

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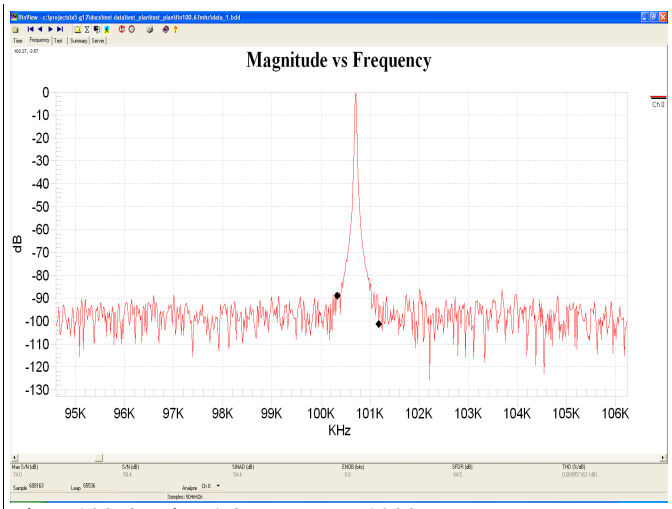
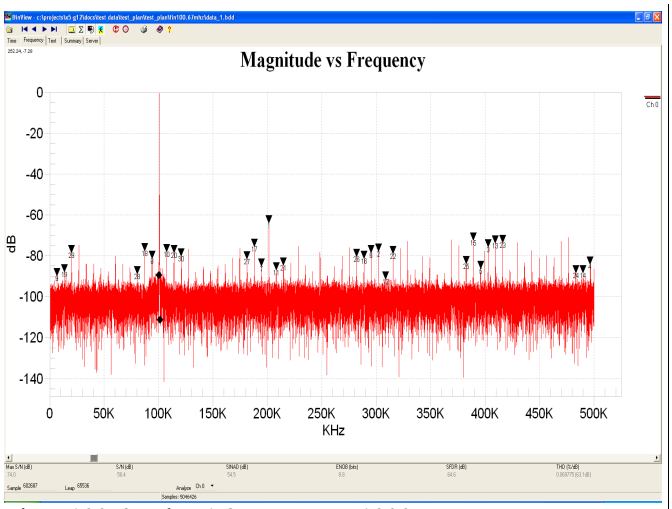


Fin = 100.67Mhz, 1.95Vp-p, Fs=1000MHz

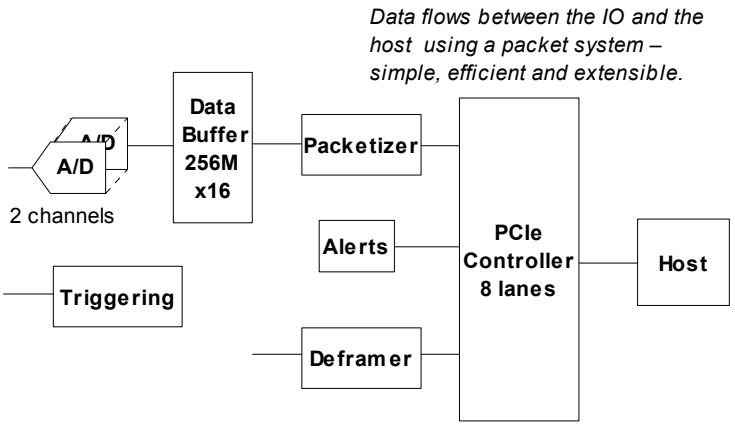


Fin = 100.67Mhz, 1.95Vp-p, Fs=1000MHz

X5-G12

Architecture and Features

The X5-G12 module architecture integrates analog IO with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates making it ideal as a front-end for demanding wireless, RADAR, signal identification and pulse digitizing applications.



X5-G12 Architecture

Analog IO

The analog front end of the X5-G12 module has two simultaneously sampling channels of 12-bit, 1 GSPS A/D input. The A/D inputs have an analog input bandwidth of 1 GHz for wideband and direct sampling applications. The A/D channels may operate in interleaved data mode to effectively increase the sample rate to 2 GSPS. The A/Ds are directly connected to the FPGA for minimum data latency.

Low frequency and DC signal information is acquired using a DC-coupled secondary A/D for each input. This A/D provides data from DC out to 125 kHz for each input for signal baseline monitoring. The low speed samples are synchronous to the high speed samples.

In the standard logic, the A/Ds have an interface component that receives the data, provides digital error correction, and a FIFO. The digital error correction is used to compensate for gain and offset errors. This method is more stable than analog adjustments and typically sacrifices less than 1% of the analog range. A non-volatile ROM on the card is used to store the calibration coefficients for the analog and is programmed during factory test.

The A/D channels operate synchronously for simultaneously sampling systems using either the on-board PLL sample clock source or an external sample clock. When the PLL is in use, either an on-board fixed-frequency crystal oscillator or and external clock may act as its reference, supporting synchronization with common external timebases such as a 10 MHz reference produced by a GPS unit.

Controls for triggering allow precise control over the collection of data and are integrated into the FPGA logic. Trigger modes include frames of programmable size, external and software. Multiple cards can sample simultaneously by using external trigger inputs. The trigger component in the logic can be customized to accommodate a variety of triggering requirements.

FPGA Core

The X5 Module family has a Virtex5 FPGA and memory at its core for DSP and control. The Virtex5 FPGA is capable of $>150x10^9$ MACs (SX95T operating at 250 MHz internally), about 20x faster than traditional DSPs. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying this processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to 512MB of DDR2 DRAM capable of >4 GB/s data transfer rate and an two independent banks of 2MB QDR SRAM capable of 4GB/s data rate each. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay or spatial filters. A multiple-queue controller component in the FPGA implements multiple data buffers in the DRAM that is used for

system data buffering and algorithm support.

The X5 module family uses the Virtex5 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the data flow, signal processing, controls and host interfaces, allowing complete customization of the X5 module functionality.

PCI Express Host Interface

The X5 architecture delivers over 1 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex5 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 20 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 200 MB/s per lane. Since PCI Express is not a shared bus but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

Private Data Links

The X5 module family has private data links on the P16 connector that can be used for system integration. The P16 connector has 8 Rocket IO links each capable of 2.5 Gbps and 16 sideband signals. The 8 RIO lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Aurora can be used.

Module Management

The data acquisition process can be monitored using the X5 alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the X5 cards easier to integrate into larger systems.

FPGA Configuration

The X5 modules have a 128Mb FLASH that holds two FPGA application images. In addition to the application image, a "golden" image is kept in FLASH for disaster recovery. The FLASH can be reprogrammed in-system using a software applet for field upgrades.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx cables such as Platform USB and Parallel IV Cable.

Software Tools

Software development tools for the X5 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools

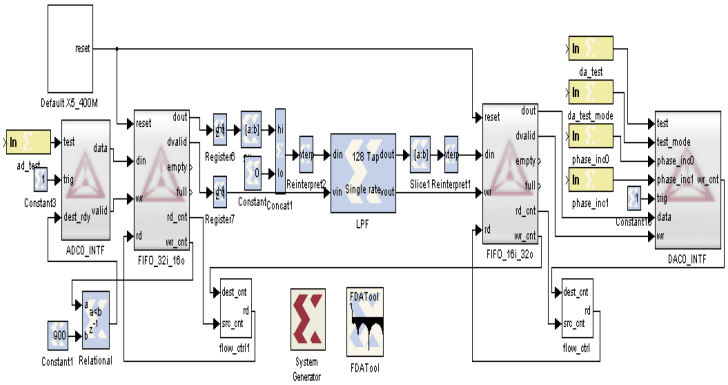
deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every X5 module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the X5 performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X5 modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for X5 Logic Design

The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

IP for DDC Channelizer Cores

Innovative provides a range of down-conversion channelizer logic cores for wideband and narrowband receiver applications for the X5 family. When fitted with these cores, the X5 modules provide powerful receiver functionality integrated for IF processing.

The DDC channelizers are offered in channel densities from 4 to 128. The four channel DDC offers complete flexibility and independence in the channels, while the 128 channel core offers higher density for uniform channel width applications. The DDC cores are highly configurable and include programmable channel filters, decimation rates, tuning and gain controls. An integrated power meter allows the DDC to measure any channel power for AGC controls.

Each IP core is provided with a MATLAB simulation model that shows bit-true, cycle-true functionality. Signal processing designers can then use this model for channel design and performance studies. Filter coefficients and other parameters from the MATLAB simulation can be directly loaded to the hardware for verification.

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Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58014	IP-MDDC4	4	Fs/2^32	16 to 32768	Fs/16	Programmable 100 tap filter
58015	IP-MDDC128	128	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter
58016	IP-MDDC-2GSPS	4	Fs/2^32	128 to 32768	Fs/128	Front-end 48 tap bandpass, Programmable 80 tap filter

Additional IP cores are offered for IF processing and baseband demodulation.

Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision.
58002	FSK Demodulation	Programmable discrimination filters, bit decision logic.
58003	TinyDDS	Tiny DDS, 1/3 to ½ size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions (Included in X5-G12 Framework)
58012	Windowing	IP core for Hann, Blackman and uniform data windowing functions.
58013	CORDIC	IP core for sine/cosine generation using CORDIC method, resulting in 1/3 logic size of standard DDS cores.

Applications Information

Cables

The X5-G12 module uses coaxial cable assemblies for the analog IO. The mating cable should have an SMA male connector and 50 ohm characteristic impedance for best signal quality.

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X5 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with 16 LVTTL signals provide support for data transfer rates up to 1.6 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80173 is suitable for high speed P16 applications.

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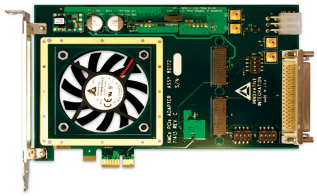
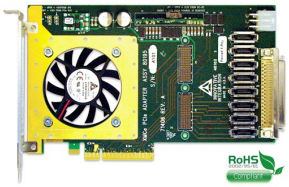
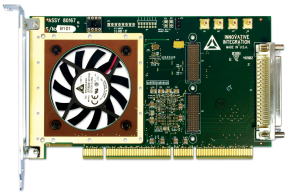
PCIe-XMC Adapter (80172) x1 PCIe to XMC Clock and trigger inputs	**PCIe-XMC Adapter x8 lane (80173)** x8 PCIe to XMC x8 RIO ports supported on P16	**PCI-XMC Adapter (80167)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC	**Compact PCI-XMC Adapter (80207)** 64-bit, 133 MHz PCI-X host x4 PCIe to XMC PXI triggers and clock support
			

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X5 modules.

eInstrument PC with Dual PCI Express XMC Modules (90199 or 90201) Windows/Linux embedded PC Low power Intel Atom available 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to XMCs 100 MB/s, 400 GB datalogger 12V operation	**eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)** PCI Express system expansion Up to 7 meter cable electrically isolated from host computer software transparent
	

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