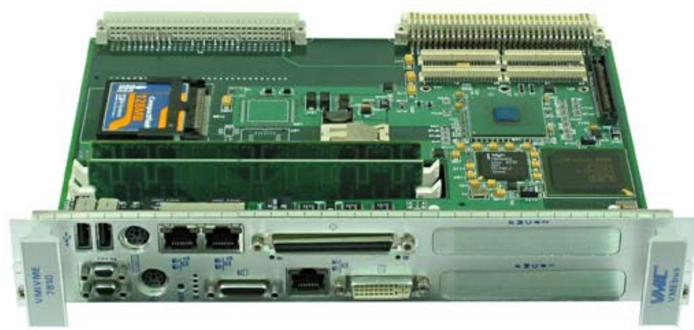
GE Fanuc Automation

VMIVME-7810 Specifications



Intel® Pentium® M Processor-Based VME Single Board Computer

Features:

- Dual slot VMEbus single board computer (SBC)
- Intel® Pentium® M processor, 478-pin µPGA
- Processor speeds up to 1.8 GHz
- 1 Mbyte L2 cache on-die
- Up to 4 Gbyte PC1600 DDR SDRAM in 2 DIMMs
- New microarchitecture supporting Micro-ops fusion, dedicated stack manager capabilities, and advanced instruction prediction capability
- Includes real time endian conversion hardware for little-endian and big-endian data interfacing (patent no. 6,032,212)
- Intel E7501 chipset
- Reliability, Availability, Serviceability, Usability and Manageability (RASUM) features:
  - Supports S4EC/D4ED ECC and x4 chipkill ECC
  - Primary hub interfaces protected by ECC
  - Secondary hub interface protected by parity
- Streaming SIMD Extensions 2
- One 10/100 Ethernet port on the front panel
  - IEEE 802.3/802.3u
  - 100BaseTX
  - IEEE 802.3x full-duplex flow control
  - 3 Kbyte TX/RX FIFO
- Two 10/100/1000 Ethernet ports on the front panel
  - IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX, and 10BaseT applications (802.3ab, 802.3u, 802.3)
  - 16 Kbyte TX FIFO, 48 Kbyte RX FIFO
  - IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX
- Dual channel SCSI support
  - One Ultra320 SCSI channel available on front panel
  - One single-ended channel available through P2 backplane connector
  - Software RAID support

(features continued on next page)

Embedded Systems

Ordering Options							
Sept. 20, 2005 800-007810-000 J		A	B	C	D	E	F
VMIVME-7810	–				0	0	

A = Processor
0 = Reserved
1 = 1.1 GHz Pentium M Processor
2 = 1.6 GHz Pentium M Processor
3 = 1.8 GHz Pentium M Processor
B = SDRAM Memory
0 = Reserved
1 = 512 Mbyte
2 = 1 Gbyte
3 = 2 Gbyte
4 = 4 Gbyte
C = CompactFlash
0 = No CompactFlash
1 = 128 Mbyte CompactFlash
2 = 256 Mbyte CompactFlash
3 = 512 Mbyte CompactFlash
4 = 1 Gbyte CompactFlash
D = 0 (Option reserved for future use)
E = 0 (Option reserved for future use)
F = Special Sales Order
0 = VME Standard
1 = 1101.10 Front Panel
2 = VME Standard with Conformal Coating
3 = 1101.10 Front Panel with Conformal Coating

Connector Adapters

Adapter	Length	Part Number
Micro-DB9 to Standard DB9	4 inches	360-010050-001
Micro-DB25 to Standard DB25	4 inches	360-010051-000

VMIACC-0045 Cable Kit contains:
Qty. 2 – Micro-DB9 to Standard DB9, 4 inches
Qty. 1 – Micro-DB25 to Standard DB25, 4 inches

VMIACC-0562 VMEbus Rear Transition Utility Board

The VMIACC-0562 installs in the rear transition area of the VMEbus backplane. The VMIACC-0562 is sold separately.

Note

All VME single board computer products come standard with a VME specification compliant front panel.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
Email: info.embeddedsystems@gefanuc.com
Web Address: www.gefanuc.com/embedded

- Two 133/100/66 MHz PCI-X expansion sites
- PMC rear I/O support (P2 connectors)
- PCI graphics (32-bit/66 MHz) using ATI Mobility Radeon M6 processor:
  - 16 Mbyte internal SGRAM
  - Video resolutions up to 1600 x 1200 x 16
  - Front panel DVI-I connector providing analog video with digital flat panel support
- Two high performance serial ports on the front panel
  - DTE RS232 support
  - 16550-compatible UART operates up to 1.5 Mbps Enhanced ESD protection
- One enhanced parallel port on the front panel
  - IEEE1284
  - EPP 1.7/1.9 support
  - ECP Level 2 support
- Two USB ports on the front panel
  - USB Revision 1.1 compliant
- Ultra DMA/100 IDE support out P2 rear panel connector
- Up to 1 Gbyte CompactFlash
- PS/2-style keyboard and mouse ports
- Real time clock and miniature speaker
- GE Fanuc Embedded Systems' suite of real time support functions:
  - Two 32-bit programmable timers
  - Two 16-bit programmable timers
  - One programmable watchdog timer
  - 32 Kbyte NVRAM
- Passive heatsink solution
- Operating system support for Windows® 2000, Windows XP, Linux® and VxWorks®

Functional Characteristics

Overview: The VMIVME-7810 brings the power of the Intel Pentium M processor coupled with dual data rate (DDR) SDRAM memory, Gigabit Ethernet and the high speed PCI-X internal bus to provide the highest level of data processing and handling capabilities in a VME form factor. The two PMC expansion sites utilize the PCI-X bus to provide higher I/O bandwidth than previously available in a VME SBC. The higher speed PCI-X bus provides up to 1 Gbyte/s bandwidth to support faster I/O devices such as Fibre Channel, Gigabit Ethernet, SCSI, Reflective Memory and InfiniBand™.

Microprocessor: The VMIVME-7810 supports the Intel Pentium M processor. The Pentium M processor provides higher levels of performance in an Intel Architecture (IA-32) processor through the use of 1 Mbyte L2 advanced transfer cache and a new, redesigned microarchitecture. This new microarchitecture features higher clock speeds, a 400 MHz system bus, micro-ops fusion, dedicated stack manager capabilities, and advanced instruction prediction capability. These features are incorporated specifically to increase performance and throughput while reducing power demands. These features are critical to providing increased processing power in power-limited environments like the VME.

The following list provides some of the key features on the Intel Pentium M processor:

- Supports Intel architecture with dynamic execution
- High performance, low power core
- On-die, primary 32 Kbyte instruction cache and 32 Kbyte write-back data cache
- On-die, 1 Mbyte level two cache with Advanced Transfer Cache architecture
- Advanced branch prediction and data prefetch logic
- Streaming SIMD Extensions 2 (SSE2)
- 400 MHz, source-synchronous processor system bus

400 MHz System Bus: The Intel Pentium M processor's 400 MHz processor system bus utilizes a split-transaction, deferred reply protocol. The 400 MHz processor system bus uses source-synchronous transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4x data transfer rate, as in AGP 4x). Along with the 4x data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2x address bus. Working together, the 4x data bus and 2x address bus provide a data bus bandwidth of up to 3.2 Gbyte/s.

Level 1 Execution Trace Cache: The Pentium M processor more than doubles the L1 cache of previous Intel processors, offering a 32 Kbyte data cache and a 32 Kbyte instruction cache. The processor also features an advanced branch prediction architecture that significantly reduces the number of mispredicted branches. The result is a means to deliver a high volume of instructions to the processor's execution units.

Level 2 Advanced Transfer Cache: The Pentium M processor offers 1 Mbyte L2 advanced transfer cache (ATC). The processor's data prefetch logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance.

Higher Core Frequencies: The new Pentium M microarchitecture allows for higher core frequencies, significantly increasing the performance and scalability of the processor.

Streaming SIMD Extensions 2 (SSE2): With the introduction of SSE2, the Intel NetBurst™ microarchitecture now extends the SIMD capabilities that MMX™ technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase. They accelerate a broad range of applications including video, speech, image, photo processing, encryption, financial, engineering and scientific applications.

The processor maintains support for MMX technology and internet streaming SIMD instructions, and full compatibility with IA-32 software. The high performance core features architectural innovations like micro-op fusion and advanced stack management that reduce the number of micro-ops handled by the processor. This results in more efficient scheduling and better performance at lower power.

The Streaming SIMD Extensions 2 enables break-through levels of performance in multimedia applications including 3D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3D geometry techniques such as ray tracing.

E7501 Chipset: The VMIVME-7810 uses the latest Intel E7501 chipset designed to deliver maximized system bus, memory and I/O bandwidth to enhance performance, scalability and end-user productivity. The Intel E7501 chipset utilizes a modular design and offers platform implementation flexibility to meet the expanding needs of high-end processors through three core components: The memory controller hub (MCH), the 64-bit PCI/PCI-X Controller Hub 2 (P64H2), and I/O controller hub 3-S (ICH3-S).

Memory Controller Hub (MCH): The MCH is the central hub for all data passing through core system elements such as the processor via the system bus interface, the memory via the memory interface, and both the 64-bit PCI/PCI-X and I/O controller hubs via Intel hub interfaces. The Intel E7501 chipset delivers compelling performance at 3.2 Gbyte/s of bandwidth across the 400 MHz system bus and up to 3.2 Gbyte/s of bandwidth across two high performance double data rate SDRAM memory channels. To balance the performance offered by the processor and memory interfaces, the MCH allows several high bandwidth I/O configuration options for a total of 3.2 Gbyte/s of I/O bandwidth.

64-bit PCI/PCI-X Controller Hub 2 (P64H2): The P64H2 connects to the MCH through a point-to-point Hub Interface 2.0 connection. In the VMIVME-7810, three P64H2 devices are attached to the MCH, each providing an I/O bandwidth greater than 1 Gbyte/s for a total of 3.2 Gbyte/s of I/O bandwidth. Each P64H2 contains two independent 64-bit PCI-X for a total of six independent 64-bit PCI-X buses. The VMIVME-7810 uses these PCI-X buses to provide the highest throughput available to the built-in dual Gigabit Ethernet ports, SCSI controller and the two PMC sites.

I/O Controller Hub 3-S (ICH3-S): The ICH3-S connects to the MCH through a point-to-point Hub Interface 1.5 connection. The ICH3-S provides legacy I/O interfaces through integrated features including a two-channel Ultra ATA/100 bus master IDE controller and three USB controllers. The ICH3-S also offers an integrated System Manageability Bus 2.0 (SMBus 2.0) controller, an integrated 10/100 ethernet controller and a PCI 2.2-compliant interface.

DDR SDRAM: The VMIVME-7810 supports PC1600 registered dual data rate (DDR) SDRAM and can accommodate two low-profile (1.2 inches or less) 184-pin DIMMS that allow up to 4 Gbyte total memory. Data transfers to and from the SDRAM on every clock edge at a 200 MHz rate for an overall transfer rate of 3.2 Gbyte/s.

10/100 Ethernet Controller: The VMIVME-7810 has a single 10/100 Ethernet controller that is integrated into the E7501 chipset's I/O controller hub (ICH) and utilizes an RJ45 connector located on the front panel. The controller supports an interface fully compliant with the IEEE 802.3/802.3u standard including the Auto-Negotiation (and 100BaseTX) standard and the IEEE 802.3x full-duplex flow control standard. The controller features enhanced scatter-gather bus mastering capabilities which allows the LAN controller to perform high speed data transfers over the PCI bus. The bus mastering capabilities enable the LAN controller to process high level commands and perform multiple operations, thereby offloading communication tasks from the system processor. Two large transmit and receive FIFOs (3 Kbyte each) are also included in the architecture to enhance performance while minimizing the use of system resources.

10/100/1000 Ethernet Controller: The VMIVME-7810 has a dual 10/100/1000 Gigabit Ethernet controller. The dual Gigabit Ethernet controller is a discrete device connected to the chipset via a private PCI-X bus segment, allowing for maximum data transfer rates of 800 Mbyte/s between the processor and Ethernet controller. The Gigabit Ethernet controller uses dual RJ45 connectors located on the front panel and provides an interface to the host processor by using on-chip command and status registers and a shared host memory area. The controller's descriptor ring management architecture is optimized to deliver both high performance and PCI-X bus efficiency. Using hardware acceleration, the Ethernet controller can offload various tasks from the host processor, such as TCP/UDP/ IP checksum calculations and TCP segmentation. The Gigabit Ethernet controller caches up to 64 packet descriptors in a single burst for efficient PCI-bandwidth usage while the large 64 Kbyte on-chip packet buffer maintains superior performance as available PCI bandwidth descriptors change. Fully integrated physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BaseT, 100BaseTX, and 10BaseT applications (802.3ab, 802.3u, 802.3).

Remote Ethernet Booting: The VMIVME-7810 utilizes the Argon Manage Boot BIOS that provides the ability to remotely boot the VMIVME-7810 using PXE, NetWare, TCP/IP or RPL network protocols.

Remote Ethernet Features:

- PXE, NetWare, TCP/IP, RPL network protocol support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Comprehensive diagnostics
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

Dual Channel Ultra320 SCSI: A PCI-X Ultra320 SCSI controller provides two independent SCSI channels. One channel is capable of data transfers at up to 320 Mbyte/s and is accessed via a front panel connector. For applications requiring connection through the backplane, the second channel is routed through user-defined pins on the VMEbus P2 connector and supports single-ended SCSI-2.

"PCI-X on PMC" Expansion Sites: The VMIVME-7810 is the industry's first VMEbus board to incorporate PMC expansion sites that support the PCI-X bus. Each PMC site is on a private PCI-X bus segment allowing maximum data transfer rates of 1 Gbyte/s between the processors and the PMC device. Each PMC site is fully backward compatible with legacy 32-bit/33 MHz and 64-bit/66 MHz PMCs with 5V/3V signaling.

Super VGA Controller: The VMIVME-7810 offers an integrated high performance 3D super VGA (SVGA) controller, the ATI mobility radeon, that supports high-resolution graphics and multimedia quality video with 16 Mbyte of SGRAM. The SVGA controller is on a private 66 MHz PCI bus allowing for maximum data transfer rates of 264 Mbyte/s. Video resolutions supported by the graphics adapter are shown in the following table.

Table 1. Video Resolutions Supported

Screen Resolution	Colors (bpp)*	Refresh Rate (Hz)
640 x 480	32 bpp	160, 120, 100, 90, 85, 75, 72, 60
800 x 600	32 bpp	160, 120, 100, 90, 85, 75, 72, 70, 60
1,024 x 768	32 bpp	120, 100, 90, 85, 75, 72, 70, 60
1,280 x 1,024	32 bpp	120, 100, 90, 85, 75, 70, 60
1,600 x 1,200	32 bpp	100, 85, 75, 60

*bpp = bits per pixel.

Digital Visual Interface (DVI): The VMIVME-7810 has a digital visual interface (DVI) located on the front panel that provides both a high speed digital video connection and legacy analog (VGA) connection. DVI supports a single transition minimized differential signal (TMDS) link allowing for flat panel resolutions up to 1,600 x 1,200. DVI also supports the VESA display data channel (DDC) and extended display identification data (EDID) specification, which provide for varying display device parameters such as timing, resolution and color depth to be accommodated. For legacy VGA support, an adapter is supplied to convert the DVI-I connector to a DB15HD female connector.

Serial Ports: The VMIVME-7810 offers two RS232 serial ports controlled by 16550-compatible UARTS. Each port has an independent 16-byte FIFO to support baud rates up to 115 Kbaud. The serial ports provide enhanced ESD protection for:

±15kV, human body model
±8kV, IEC1000-4-2, contact discharge
±15kV, IEC1000-4-2, air-gap discharge

The serial ports are accessible via two micro-DB9 male connectors located on the front panel. An adapter is available to adapt the micro-DB9 connector to a standard male DB9 connector (GE Fanuc Embedded Systems P/N 360-010050-001).

CompactFlash: The VMIVME-7810 includes a CompactFlash socket on the assembly. The CompactFlash can be configured as the boot device through the BIOS boot device set up. The CompactFlash, as an ordering option, is available up to 1 Gbyte of storage space.

Parallel Port: The VMIVME-7810 offers a single enhanced parallel port. The parallel port is IEEE1284 compliant and supports EPP 1.7/1.9 and ECP Level 2 standards. The parallel port is accessible via a micro-DB25 connector located on the front panel. An adapter is available to adapt the micro-DB25 connector to a standard DB25 female connector (GE Fanuc Embedded Systems P/N 360-010051-000).

USB Port: The VMIVME-7810 offers two USB ports compliant with the USB 1.1 specification. The USB ports are accessible via USB connectors located on the front panel.

Keyboard/Mouse Ports: The VMIVME-7810 supports a standard PS/2 keyboard and mouse. The keyboard and mouse ports are accessible via two 6-pin mini DIN connectors located on the front panel.

Programmable Timer: The VMIVME-7810 provides the user with two 16-bit timers and two 32-bit timers. These timers are mapped in PCI memory space, are completely software programmable, and can generate PCI interrupts.

Watchdog Timer: The VMIVME-7810 provides a software-programmable watchdog timer. The watchdog timer is enabled under software control. Once the timer is enabled, software must access the timer within the specified time period, or the output of the watchdog timer will reset the VMIVME-7810.

Nonvolatile SRAM: The VMIVME-7810 provides 32 Kbyte of nonvolatile SRAM. The contents of the SRAM are preserved when power is interrupted or removed from the unit.

Reset Switch and Annunciators: A push-button switch located on the front panel is used to reset the VMIVME-7810. Indicators on the front panel include: Attention (Red), Power/Reset (Green), IDE Activity (Yellow), VMEbus SYSFAIL (Red), LAN activity and LAN link speed.

VMEbus Interface: The VMIVME-7810 VMEbus interface is based on the Universe IID high performance PCI-to-VMEbus interface from Tundra. The following VME64 modes are supported: A32/A24/D32/D16/D08(EO)/MBLT64/BLT32.

System Controller: The VMEbus system controller capabilities allow the board to operate as a slot 1 controller, or it may be disabled when another board is acting as the system controller. The system controller may be programmed to provide the following modes of arbitration:

Round Robin (RRS)
Single Level (SGL)
Priority (PRI)

The system controller provides a SYSCLK driver, IACK* daisy-chain driver, and a VMEbus access timeout timer. The system controller also provides an arbitration timeout if BBSY* is not seen within a specified period after a BGOUT* signal is issued. This period is programmable for 16 or 256 μs.

VMEbus Requester: The microprocessor can request and gain control of the bus using any of the VMEbus request lines (BR3* to BR0*) under software control. The requester can be programmed to operate in any of the following modes:

Release-On-Request (ROR)
Release-When-Done (RWD)
VMEbus Capture and Hold (VCAP)

Mailboxes: The VMEbus interface provides four 32-bit mailboxes, which are accessible from both the microprocessor and the VMEbus, providing interprocessor communication. The mailboxes have the ability to interrupt the microprocessor when accessed by VMEbus.

Interrupt Handler: The interrupt handler monitors, and can be programmed to respond to any or all VMEbus IRQ* lines. All normal-process VMEbus-related interrupts can be mapped to PCI INTA# or SERR# interrupts. These include:

Mailbox interrupts
VMEbus interrupts
VMEbus interrupter IACK cycle (acknowledgment of VMIVME-7810 VMEbus-issued interrupts)

All error processing VMEbus-related interrupts can be mapped to PCI INTA# or SERR#. Note: PCI SERR# initiates an SBC NMI. These include:

ACFAIL* interrupt
BERR* interrupt
SYSFAIL* interrupt

The interrupt handler has a corresponding STATUS/ID register for each IRQ* interrupt. Once the handler receives an IRQ*, it requests the VMEbus and, once granted, it performs an IACK cycle for that level. Once the IACK cycle is complete and the STATUS/ID is stored in the corresponding ID register, an appropriate interrupt status bit is set in an internal status register and a PCI interrupt is generated. The PCI interrupt can be mapped to PCI INTA# or SERR#.

Interrupter: Interrupts can be issued under software control on any or all of the seven VMEbus interrupt lines (IRQ7* to IRQ1*). A common ID register is associated with all interrupt lines. During the interrupt acknowledge cycle, the interrupter issues the ID to the interrupt handler.

The interrupter can be programmed to generate a PCI INTA# or SERR# interrupt when a VMEbus interrupt handler acknowledges a software-generated VMEbus interrupt.

Byte Swapping: The Intel 80x86 family of processors uses little-endian format. To accommodate other VMEbus modules that transfer data in big-endian format (such as the 680x0 processor family), the VMIVME-7810 incorporates byte-swapping hardware. This provides independent byte swapping for both the master and slave interfaces. Both master and slave interface byte swapping are under software control.

The VMIVME-7810 supports high throughput DMA transfers of bytes, words and longwords in both master and slave configurations.

If endian conversion is not needed, we offer a special "bypass" mode that can be used to further enhance throughput. (Not available for byte transfers.)

Master Interface: MA32:MBLT32:MBLT64 (A32:A24:A16:D32:D16:D8 (EO):BLT32)

The VMEbus master interface provides nine separate memory windows into VMEbus resources. Each window has separate configuration registers for mapping PCI transfers to the VMEbus (that is, PCI base address, window size, VMEbus base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the nine windows are as follows:

Window	Minimum Size	Maximum Size
0, 4	4 Kbyte	4 Gbyte
1 to 3, 5 to 7	64 Kbyte	4 Gbyte
Special Cycle	64 Mbyte	64 Mbyte

Slave Interface: Memory Access : SAD032:SD32:SBLT32:SBLT64 (A32:A24:A16:D32:D16:D8 (EO): BLT32)

The VMEbus slave interface provides eight separate memory windows into PCI resources. Each window has separate configuration registers for mapping VMEbus transfers to the PCI bus (that is, VMEbus base address, window size, PCI base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the eight windows are as follows:

Window	Minimum Size	Maximum Size
0, 4	4 Kbyte	4 Gbyte
1 to 3, 5 to 7	64 Kbyte	4 Gbyte

In addition, each window can be programmed to operate in coupled or decoupled mode. In decoupled mode, the window utilizes a write-posting FIFO and/or a read prefetching FIFO for increased system performance. In coupled mode, the FIFOs are bypassed and VMEbus transactions are directly coupled to the PCI bus (that is, transfers on VMEbus are not completed until they are completed on the PCI bus).

Enhanced Bus Error Handling: Enhancements over the Universe chip's bus error handling features are provided. A latch and register are provided to allow the SBC to read the VMEbus address that caused the bus error in all modes. The Universe chip's support is limited to decoupled mode. Support for bus cycle timeout and assertion of bus error is provided. The board may be configured to assert bus error upon timeout regardless of its status as system controller. The Universe chip asserts bus error only if it is system controller. In addition, this board may be configured to assert an interrupt upon bus cycle timeout.

Operating System and Software Support

The VMIVME-7810 supports a variety of operating systems including Microsoft® Windows 2000, Windows XP, Linux and VxWorks Tornado/AE BSPs. The BSP provides support for the VMEbus interface, Ethernet and timers.

Physical/Environmental Specifications

Dimensions: 6U (8HP) dual slot Eurocard form factor

Height	9.2 in. (233.4mm)
Depth	6.3 in. (160mm)
Thickness	0.8 in. (20.3mm)

Power Requirements:
+5VDC (±5 percent), 12A (typical), 14A maximum
+12VDC (±5 percent), 10mA (typical), 25mA maximum
-12VDC (±5 percent), 0mA (typical), 8mA maximum

Note: Installing PMCs may increase one, or all, of the current requirements. No PMC boards were installed during power measurements. Power measurements were made running PassMark Software's BurnIn Test ver. 4.0 which exercises the processor, chipset, memory bus, video chip, SCSI, USB, serial/parallel ports, and disk drives. For this product, the +12V and -12V supplies are not used to power any on-board devices and only go to the two PMC sites and the GE Fanuc Embedded Systems PCI expansion connector.

The currents at +12 and -12VDC are specified with the serial connectors open.

PMC Expansion Site Connector: 3.3V signaling, auto-VIO
64-bit PCI-X bus, 133 MHz maximum
(Backward compatible to 3V 33 MHz PCI)

PMC Rear I/O Support: via the P2 connectors

Airflow: Heatsink with forced air cooling required: 400 LFM minimum

Temperature:
Operating: 0 to +50° C
Storage: -40 to +80° C

Altitude:
Operating: 0 – 10,000 ft (3,000m)
Storage: 0 – 40,000 ft (12,000m)

Humidity:
Operating: relative humidity 10% to 90%, noncondensing
Storage: relative humidity 10% to 90%, noncondensing

MTBF: 165,000 hours

Trademarks

MMX and NetBurst are trademarks and Intel and Pentium are registered trademarks of Intel Corporation. Microsoft and Windows are registered trademarks of Microsoft Corporation. Other registered trademarks are the property of their respective owners.

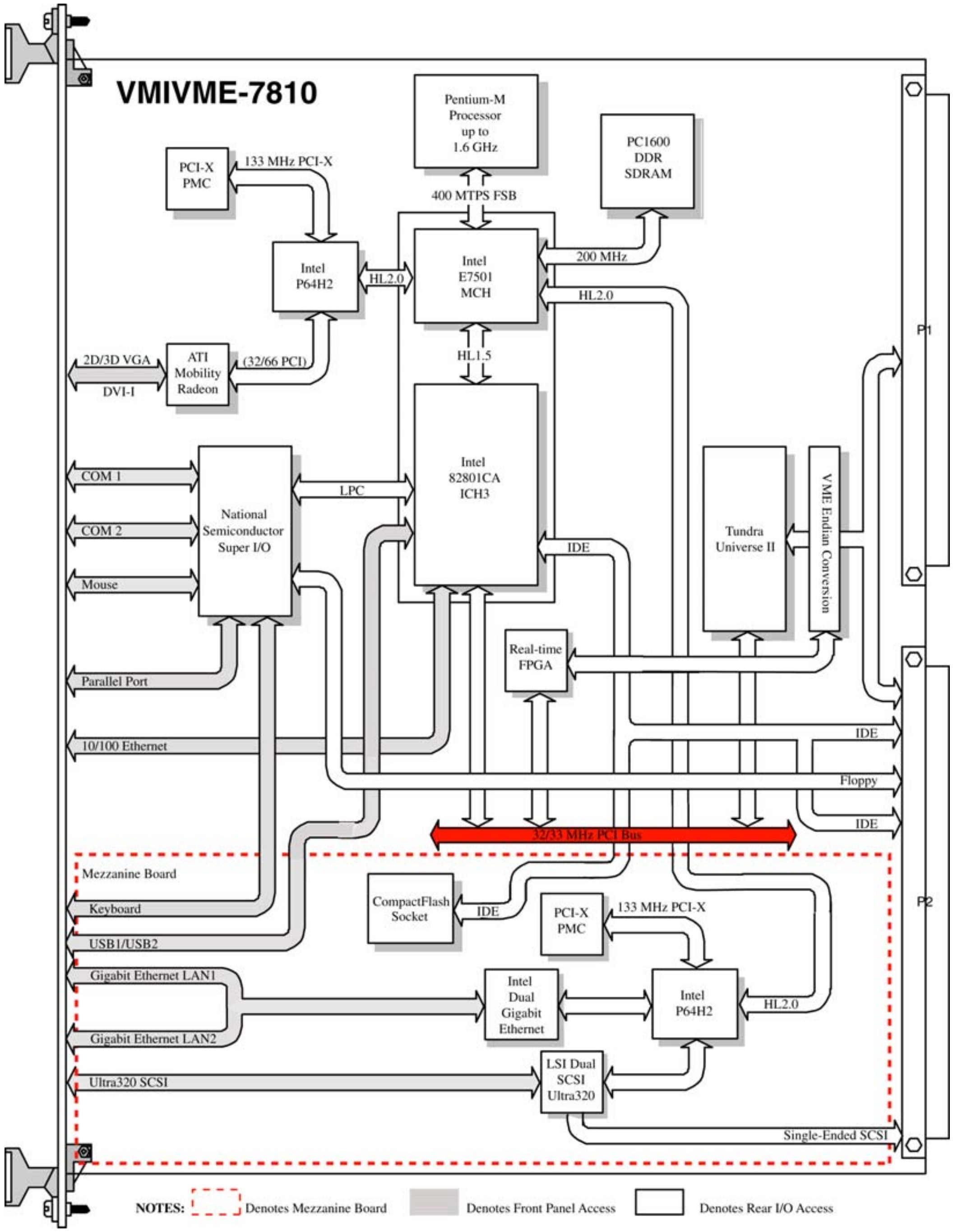


Figure 1. VMIVME-7810 Block Diagram

GE FANUC

Embedded Systems

GE Fanuc Embedded Systems Information Centers

Americas:

Huntsville, AL	1 800 322-3616
	1 (256) 880-0444
Camarillo, CA	1 (805) 987-9300
Greenville, SC	1 (864) 627-8800
Richardson, TX	1 (972) 671-1972

Europe, Middle East and Africa:

Edinburgh, UK	44 (131) 561-3520
Paris, France	33 (1) 4324 6007

Additional Resources

For more information, please visit the GE Fanuc Embedded Systems web site at:
www.gefanuc.com/embedded