Vox Global Sourcing

ICF Series

Industrial CompactFlash® Card

Data Sheet

Rev. 1.0

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REVISION HISTORY

Revision	Description	Date
1.0	Release	September 2005

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1. Introduction

The IGS Industrial CompactFlash® Memory Card (ICF) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association (PCMCIA) ATA (PC Card ATA) standard. (In Japan, the applicable standards group is JEIDA.) The CompactFlash® and PCMCIA cards support True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot. Designed to replace traditional rotating disk drives, IGS Industrial CompactFlash® Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial work place. These Industrial CompactFlash® feature an extremely lightweight, reliable, low-profile form factor.

2. Features

The Industrial ATA products provide the following system features:

- Capacities: 32, 64, 128, 256, 512 and 1024MB
- PCMCIA v2.1 and PC Card v2.01 ATA compatible
- Three access mode
  - Memory Card Mode
  - I/O Mode
  - True IDE Mode
- High reliability based on the internal ECC (Error Correction Code) function
- +3.3V/+5V single power supply operation
- Non-volatile storage (no battery required)
- Support Auto Stand-by and Sleep Mode.
- Support Master/Slave mode
- Industrial class, very rigid & rugged design
- MTBF >3,000,000 hours
- Minimum 10,000 insertions
- Shock: 30G, Vibration: 1500G
- High performance:
  - Read: 10MBytes/s
  - Write: 9MBytes/s
- Temperature range:
  - Industrial: -10°C ~ +70°C
  - Wide: -40°C ~ +85°C
- ABS Mechanical Cover

3. Pin Assignment

See Table 1 for ICF pin assignments.

Table 1: ICF Pin Assignments

Pin No.	Name	I/O	Pull Up/Down	Schmitt Trigger	Driving Capability[1]
1	GND	Power			GND
2	HD[3]	I/O		V	4 or 8 mA
3	HD[4]	I/O		V	4 or 8 mA
4	HD[5]	I/O		V	4 or 8 mA
5	HD[6]	I/O		V	4 or 8 mA
6	HD[7]	I/O		V	4 or 8 mA
7	CE1B	I	Up	V	
8	HA[10]	I		V	
9	OEB	I	Up	V	
10	HA[9]	I		V	
11	HA[8]	I		V	
12	HA[7]	I		V	
13	HOST VCC	Power			HOST VCC
14	HA[6]	I		V	
15	HA[5]	I		V	
16	HA[4]	I		V	
17	HA[3]	I		V	
18	HA[2]	I		V	
19	HA[1]	I		V	
20	HA[0]	I		V	
21	HD[0]	I/O		V	4 or 8 mA
22	HD[1]	I/O		V	4 or 8 mA
23	HD[2]	I/O		V	4 or 8 mA
24	IOIS16B	O			4 or 8 mA
25	GND	Power			GND
26	GND	Power			GND
27	HD[11]	I/O		V	4 or 8 mA
28	HD[12]	I/O		V	4 or 8 mA
29	HD[13]	I/O		V	4 or 8 mA
30	HD[14]	I/O		V	4 or 8 mA
31	HD[15]	I/O		V	4 or 8 mA
32	CE2B	I	Up	V	
33	VS1	Power			GND
34	IORB	I	Up	V	
35	IOWB	I	Up	V	
36	WEB	I	Up	V	
37	IREQ	O			4 or 8 mA
38	HOST VCC	Power			HOST VCC

Pin No.	Name	I/O	Pull Up/Down	Schmitt Trigger	Driving Capability[1]
39	CSELB	I	Up		
40	VS2	Power			GND
41	RESET	I	Up	V	
42	WAITB	O			4 mA
43	INPACKB	O			4 or 8 mA
44	REGB	I	Up	V	
45	DASPB	I/O	Up	V	4 or 8 mA
46	PDIAGB	I/O	Up	V	4 or 8 mA
47	HD[8]	I/O		V	4 or 8 mA
48	HD[9]	I/O		V	4 or 8 mA
49	HD[10]	I/O		V	4 or 8 mA
50	GND	Power			GND

1. The Driving Capability “4 or 8 mA” means ---

   When in 5V environment, the output driving capability is 4mA,

   When in 3.3V environment, the output driving capability is 8mA, but these PAD is 5V design, so the really output capability is UNDER 8mA.

4. Pin Description

Table 2 describes the pin descriptions for ICF

Table 2: ICF Pin Description

Pin No.	Pin Name	I/O	Description
41	RESET (PC Card Memory Mode)	I	If this signal is asserted high, the card internal initialization begins to operate. During the card internal initialization RDY/BSY# is low. After the card internal initialization RDY/BSY# is high.
	RESET (PC Card I/O Mode)	I	If this signal is asserted high, the card internal initialization begins to operate. In this mode, RDY/BST# signal can not be used, so using Status Register the Ready/Busy status can be confirmed.
	RESET# (True IDE Mode)	I	If this signal is asserted low, all the registers in this card are reset. In this mode, RDY/BSY# signal can not be used, so using Status Register the Ready/Busy status can be confirmed.
39	CSELB (PC Card Memory Mode) (PC Card I/O Mode)	I	This signal is not used.
	CSELB (True IDE Mode)	I	When MSB signal is High, this signal is used to configure this device as a Master or Slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a Master. When the pin is High, this device is configured as a Slave.
7, 32	CE[2:1]B (PC Card Memory Mode) (PC Card I/O Mode)	I	CE1B and CE2B are low active card select signals. Byte/Word/Odd byte mode is defined by combination of CE1B, CE2B and HA0.
	CE[2:1]B (True IDE Mode)	I	CE2B is used for select the Alternate Status Register and the Device Control Register while CE1B is the chip select for the other task file registers.
44	REGB (PC Card Memory Mode)	I	REGB is used during memory cycles to distinguish between task file and attribute memory access. High for task file, Low for attribute memory is accessed.
	REGB (PC Card I/O Mode)	I	REGB is constantly low when task file or attribute memory is accessed.
	REGB (True IDE Mode)	I	This input signal is not used and should be connected to VCC.
9	OEB (PC Card Memory Mode)	I	OEB is used for the control of reading register's data in attribute area or task file area.
	OEB (PC Card I/O Mode)	I	OEB is used for the control of reading register's data in attribute area.
	ATASEL# (True IDE Mode)	I	To enable True IDE mode, this input should be grounded by the host.
36	WEB (PC Card Memory Mode)	I	WEB is used for the control of writing register's data in attribute area or task file area.
	WEB (PC Card I/O Mode)	I	WEB is used for the control of writing register's data in attribute area.
	WEB (True IDE Mode)	I	To enable True IDE mode, this input should be connected to VCC by the host.

Pin No.	Pin Name	I/O	Description
34	IORB (PC Card Memory Mode)	I	This signal is not used.
	IORB (PC Card I/O Mode)	I	IORB is used for control of read data in I/O task file area. This card does not respond to IORB until I/O card interface setting up.
	IORB (True IDE Mode)	I	IORB is used for control of read data in I/O task file area. This card does not respond to IORB until I/O card interface setting up.
35	IOWB (PC Card Memory Mode)	I	This signal is not used.
	IOWB (PC Card I/O Mode)	I	IOWB is used for control of write data in I/O task file area. This card does not respond to IOWB until I/O card interface setting up.
	IOWB (True IDE Mode)	I	IOWB is used for control of write data in I/O task file area. This card does not respond to IOWB until I/O card interface setting up.
8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	HA[10:0] (PC Card Memory Mode) (PC Card I/O Mode)	I	Address bus
	HA[10:0] (True IDE Mode)	I	Address bus. Only HA[2:0] are used.
42	WAITB (PC Card Memory Mode) (PC Card I/O Mode)	O	The WAITB signal is always driven high to signal the host to zero-delay completion of a memory or I/O cycle that is in progress.
	IORDY (True IDE Mode)	O	In True IDE Mode this output signal may be used as IORDY, and always driven pull-high.
37	RDY/BSY# (PC Card Memory Mode)	O	The signal turns low level during the card internal initialization operation at VCC applied or reset applied, so next access to the card should be after the signal turned high level.
	IREQ (PC Card I/O Mode)	O	The signal of low level indicates that the card is requesting software service to host, and high indicates that the card is not requesting.
	INTRQ (True IDE Mode)	O	This signal is the active high Interrupt Request to the host.
43	INPACKB (PC Card Memory Mode)	O	This signal is not used and should not be connected at the host.
	INPACKB (PC Card I/O Mode)	O	This signal is asserted low by this card when the card is selected and responding to an I/O read cycle at the address that is on the address bud during CE# and IORD# are low. This signal is used for the input data buffer control.
	INPACKB (True IDE Mode)	O	This signal is not used and should not be connected at the host.
24	WP (PC Card Memory Mode)	O	WP is held low because this card does not have write-protect switch.
	IOIS16B (PC Card I/O Mode)	O	IOIS16B is asserted (Low) when task file registers are accessed in 16-bit or add byte only mode.
	IOIS16B (True IDE Mode)	O	This output signal is asserted low when this device is expecting a word data transfer cycle. Default mode is 16-bit. The card operates in byte mode, if the user issued a Set Feature Command to put the device in Byte access mode.
31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	HD[15:0] (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	I/O	Host data bus. HD0 is the LSB of the even byte of the word. HD8 is the LSB of the odd byte of the word.

Pin No.	Pin Name	I/O	Description
45	BVD2 (PC Card Memory Mode)	I/O	BVD2 output the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
	SPKR# (PC Card I/O Mode)	I/O	SPKR# output speaker signal. This output line is constantly driven to a high state since this product does not support the audio function.
	DASPB (True IDE Mode)	I/O	DASPB is the Slave Present signal in the Master/Slave handshake protocol. And is Disk Active signal after power on diagnostic command.
46	BVD1 (PC Card Memory Mode)	I/O	BVD2 output the battery voltage status in the card. This output line is constantly driven to a high state since a battery is not required for this product.
	STSCHG# (PC Card I/O Mode)		STSCHG# is used for changing the status of Configuration and Status Register in attribute area.
	PDIAGB (True IDE Mode)		PDIAGB is the Pass Diagnostic signal in Master/Slave handshake protocol.

5. Specifications

5.1 CE and FCC Compatibility

ICF conforms to CE requirements and FCC standards.

5.2 Environmental Specifications

5.2.1 Temperature Ranges

Temperature Range: -10°C to +70°C

Storage Temperature: -40°C to +85°C

5.2.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.2.3 Shock and Vibration

Table 3: Shock/Vibration Testing for ICF

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 5 g, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 10ms, 50 g, 3 axes	IEC 68-2-27
Drop Unit	From a height of 1.5 m	IEC 68-2-32

5.2.4 Mean Time between Failures (MTBF)

Table 5 summarizes the MTBF prediction results for various ICF configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

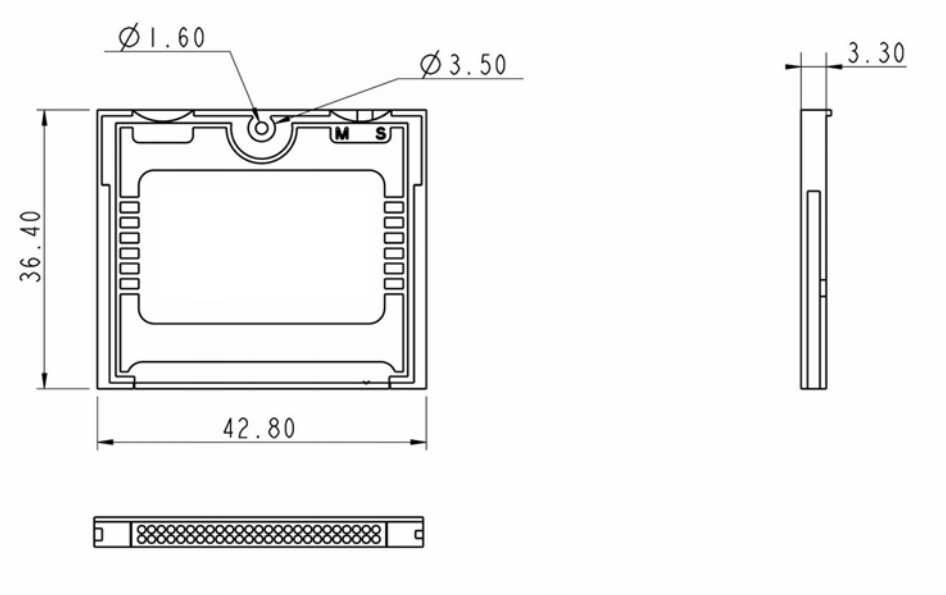
Table 4: ICF MTBF

Product	Condition	MTBF (Hours)	Failure Rate per Million Hours
ICF	Telcordia SR-332 GB, 25 °C	6,188,875	0.1616

5.3 Mechanical Dimensions

Mechanical Dimension: 42.80/36.40/3.30mm (W/T/H)

Figure 1: Mechanical Dimension of ICF



5.4 Electrical Specifications

5.4.1 Electric Characteristic

Table 5: ICF Electric Characteristic

V_{DD}=4.5V~5.5V

Item	Symbol	Value			Unit	Measuring conditions
		Min	Standard	Max		
Input voltage (TTL Level)	V_{IH}	2.0	-	-	V	
	V_{IL}	-	-	0.8	V	
Input voltage (CMOS Level)	V_{IH}	3.5	-	-	V	
	V_{IL}	-	-	1.5	V	
Schmitt trigger input (TTL Level)	V_{+}	-	1.51	2.15	V	
	V_{-}	0.6	1.01	-	V	
	V_{h}	0.25	-	-	V	
Output voltage	V_{OH}	3.7	-	-	V	I_{OH}=2mA~-24mA
	V_{OL}	-	-	0.4	V	I_{OL}=2mA~-24mA
Input leakage current	I_{IH}	-10	-	10	µA	$V_{IN}=V_{DD}$
	I_{IL}	-10	-	10	µA	V_{IN}=GND
Output leakage current	I_{OZ}	-10	-	10	µA	Hi-Z state
Pull-up resistor	R_{PU}	50	-	500	KOhm	V_{IN}=GND
Pull-down resistor	R_{PD}	15.7	-	128	KOhm	$V_{IN}=V_{DD}$

V_{DD}=3.0V~3.6V

Item	Symbol	Value			Unit	Measuring conditions
		Min	Standard	Max		
Input voltage (TTL Level)	V_{IH}	1.75	-	-	V	
	V_{IL}	-	-	0.65	V	
Input voltage (CMOS Level)	V_{IH}	2.15	-	-	V	
	V_{IL}	-	-	0.95	V	
Schmitt trigger input (TTL Level)	V_{+}	-	1.32	1.75	V	
	V_{-}	0.45	0.86	-	V	
	V_h	0.25	-	-	V	
Output voltage	V_{OH}	2.4	-	-	V	I_{OH}=1mA~-12mA
	V_{OL}	-	-	0.4	V	I_{OL}=1mA~-12mA
Input leakage current	I_{IH}	-10	-	10	µA	$V_{IN}=V_{DD}$
	I_{IL}	-10	-	10	µA	V_{IN}=GND
Output leakage current	I_{OZ}	-10	-	10	µA	Hi-Z state
Pull-up resistor	R_{PU}	76.6	-	750	KOhm	V_{IN}=GND
Pull-down resistor	R_{PD}	24	-	200	KOhm	$V_{IN}=V_{DD}$

5.4.2 Maximum Absolute Ratings

Table 6: ICF Maximum Absolute Ratings

(Referenced to GND)

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD} (HVCC)	-0.6 ~ +6.0	V
	V_{DD} (CVCC/FVCC)	-0.3 ~ +4.0	V
Input voltage	V_{IN} (HVCC)	-0.6 ~ V_{DD}+0.6	V
	V_{IN} (CVCC/FVCC)	-0.3 ~ V_{DD}+0.3	V
	V_{IN} (5V)	-0.3 ~ +7.3	V
Output current	I_{OUT}	±15 (8mA buffer)	mA
Storage temperature	T_{STG}	-55 ~ +125	°C

5.4.3 Recommended Operation Conditions

Table 7: ICF Recommended Operation Conditions

item	Symbol	Rating	Unit
Power supply voltage	V_{DD} (HVCC)	3.0~3.6	V
		4.5~5.5	V
	V_{DD} (CVCC/FVCC)	3.0~3.6	V
Ambient operating temperature	T_A (Pin Capacitance : 40pF)	-40~+85	°C
	T_A (Pin Capacitance : 80pF)	0~+70	°C

5.4.4 Timing Specifications

Figure 2: Reading Timing Diagram, PIO Mode 4

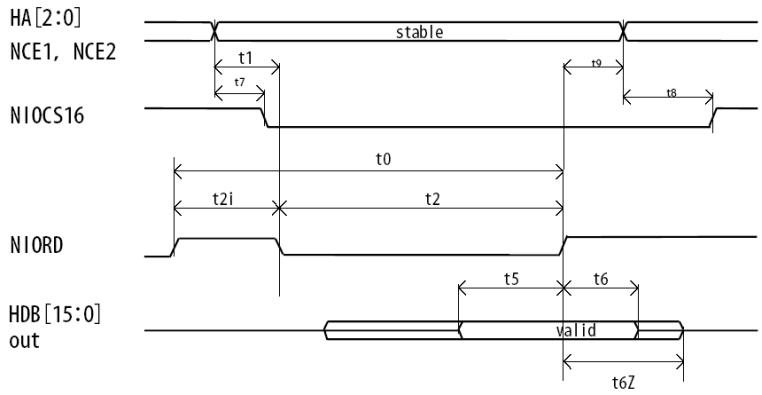


Table 8: Reading Timing Specifications, PIO Mode 4

Item	Symbol	Min〔ns〕	Max〔ns〕
Cycle Time	t0	120	—
IORD Data Setup	t5	20	—
IORD Data Hold Time	t6	5	—
IORD Data Tri-state Time	t6Z	—	30
IORD Width Time	t2	70	—
IORD Recovery Time	t2i	25	—
Address Setup Time	t1	25	—
Address Hold Time	t9	10	—
IOIS16 Delay Falling from Address	t7	—	40
IOIS16 Delay Rising from Address	t8	—	30

Figure 3: Writing Timing Diagram, PIO Mode 4

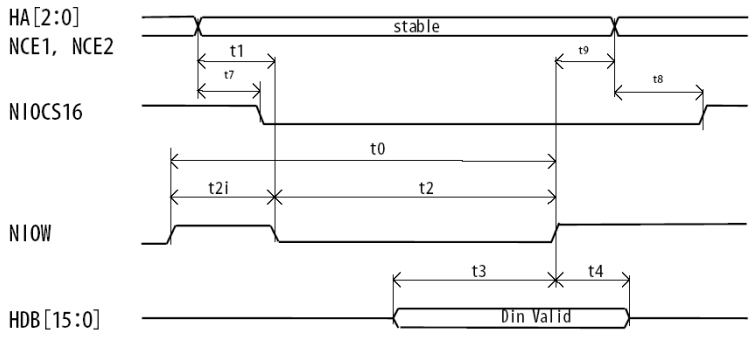


Table 9: Writing Timing Specifications, PIO Mode 4

Item	Symbol	Min〔ns〕	Max〔ns〕
Cycle Time	t0	120	—

Item	Symbol	Min〔ns〕	Max〔ns〕
IOWR Data Setup Time	t3	20	—
IOWR Data Hold Time	t4	10	—
IOWR Width Time	t2	70	—
Address Setup Time	t1	25	—
Address Hold Time	t9	10	—
IOIS16 Delay Falling from Address	t7	—	40
IOIS16 Delay Rising From Address	t8	—	30

Figure 4: Reset Timing Diagram

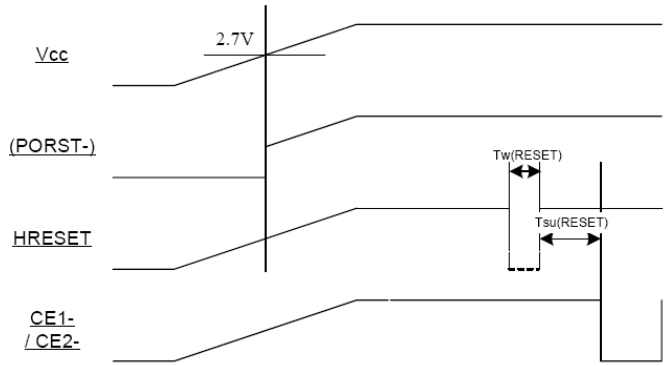


Table 10: Reset Timing Specifications

Item	Symbol	Min	Max	Unit
RESET Setup	T_{SU} (RESET)	2		ms
RESET Width	T_W (RESET)	25		µs

5.5 Supported IDE Commands

ICF supports the commands listed in Table 11.

Table 11: IDE Commands

Command Name	Command Code
CHECK POWER MODE	98H or E5H
EXECUTE DEVICE DIAGNOSTIC	90H
FORMAT TRACK	50H
IDENTIFY DEVICE	ECH
IDLE	97H or E3H
IDLE IMMEDIATE	95H or E1H
INITIALIZE DEVICE PARAMETERS	91H
NOP	00H
READ BUFFER	E4H

Command Name	Command Code
READ LONG SECTOR	22H or 23H
READ MULTIPLE	C4H
READ SECTOR(S)	20H or 21H
READ VERIFY SECTOR	40H or 41H
RECALIBRATE	1XH
SEEK	7XH
SET FEATURES	EFH
SET MULTIPLE MODE	C6H
SET SLEEP MODE	99H or E6H
STANDBY	96H or E2H
STANDBY IMMEDIATE	94H or E0H
WRITE BUFFER	E8H
WRITE LONG SECTOR	E8H
WRITE MULTIPLE	C5H
WRITE SECTOR(S)	30H or 31H
WRITE VERIFY	3CH

6. Physical Outline

Figure 5: ICF Physical Outline