X5-COM

Innovative Integration
... real time solutions!

PCI Express XMC Module with Four Ethernet/SRIO/Gigabit Serial Ports, Virtex5 SXT or FXT FPGA and 512MB Memory
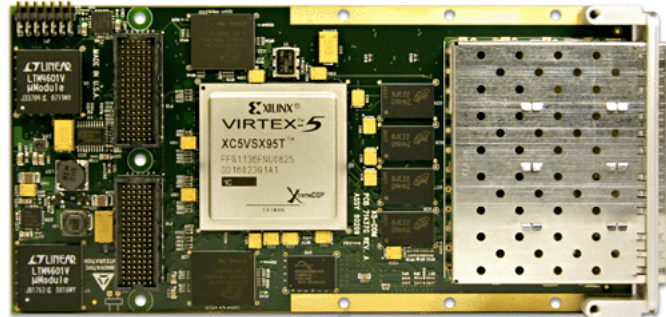
FEATURES

- Four communications ports Gigabit Ethernet, Aurora, Infiniband, Serial Rapid IO (requires supporting IP in FPGA)
- Xilinx Virtex5 SX95T or FX100T FPGA
- SX95T: 640 DSP MACs
- FX100T: 2 PowerPC+ 256 DSP MACs
- Industry-standard SFP modules support up to 4.125 Gbps over Copper or Fiber Optic cables (rates depend on FPGA speed and cable)
- 512MB DDR2 DRAM supporting 4 GB/s transfer rates
- 4MB QDR-II SRAM for computations
- 4 Rocket IO links for data plane using P16
- >1 GB/s, 8-lane PCI Express Host Interface
- Conduction cooling and thermal monitoring
- XMC Module (75x150 mm)
- PCI Express (VITA 42.3)

APPLICATIONS

- Ethernet packet processing
- Communications test equipment
- FPGA computing node
- Digital Wireless IF Receiver and Transmitter
- Real-time data encryption for Ethernet
- Remote IO interfacing
- High Speed Data Recording and Playback
- IP development

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ Host Tools

MATLAB

XILINX

RoHS 2002/95/EC Compliant

DESCRIPTION

The X5-COM is an XMC IO module featuring four 4.125 Gbps serial ports directly connected to a Virtex5 FPGA computing core with DRAM and SRAM memory, and PCI Express host interface. With supporting IP, the X5-COM is ideal for computational intensive applications for Ethernet packet processing, encryption and test.

A Xilinx Virtex5 FPGA with 512MB DDR2 DRAM and 4MB QDR-II SRAM memory provides a very high performance computing core. Either the SXT95 or FXT100 Virtex5 FPGA is available. The FPGA has four Ethernet MACs and 2 PowerPCs (FX100T) in the FPGA logic array.

The X5 XMC modules couple Innovative's powerful Velocia architecture with a high performance, 8-lane PCI Express interface that provides over 1 GB/s sustained transfer rates to the host. Private links to host cards with > 800 MB/s capacity using P16 are provided for system integration.

The X5 family can be fully customized using VHDL and MATLAB using the FrameWork Logic toolset. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator.

Software tools for host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features and use are provided.

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ORDERING INFORMATION

Product	Part Number	Description
X5-COM	80209-0	PCI Express XMC module with four SFP ports, Virtex5 SX95T FPGA, 4MB SRAM, 512MB DRAM. SFP modules sold separately.
	80209-1	PCI Express XMC module with four SFP ports, Virtex5 FX100T FPGA, 4MB SRAM, 512MB DRAM. SFP modules sold separately.
X5-Breakout	34012	Remote digital interface module which converts clocked, parallel digital data into serial format, which connects to the X5-COM module via up-to-four SFP cables.
Logic		
X5-COM FrameWork Logic	55018	X5-COM FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Cables	**Cables**	**Cables**
SMA to BNC cable	67048	IO cable with SMA (male) to BNC (female), 1 meter
Adapters	**Adapters**	**Adapters**
XMC-PCIe x1 Adapter	80172-0	PCI Express Carrier card for XMC PCI Express modules, x1 lanes
XMC- PCIe x8 Adapter	80173-0	PCI Express Carrier card for XMC PCI Express modules, x8 lanes
XMC-PCI Adapter	80167	PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-cPCI Adapter	80207	3U Compact PCI Carrier card for XMC PCI Express modules, 64-bit PCI-X
XMC-Cabled PCIe Adapter	90181	Cabled PCI Express Carrier card for XMC PCI Express modules, single-lane.
Embedded PC Host	**Embedded PC Host**	**Embedded PC Host**
eInstrument PC	90199	Embedded PC XMC host with support for two XMC modules for standalone applications.

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X5-COM Block Diagram
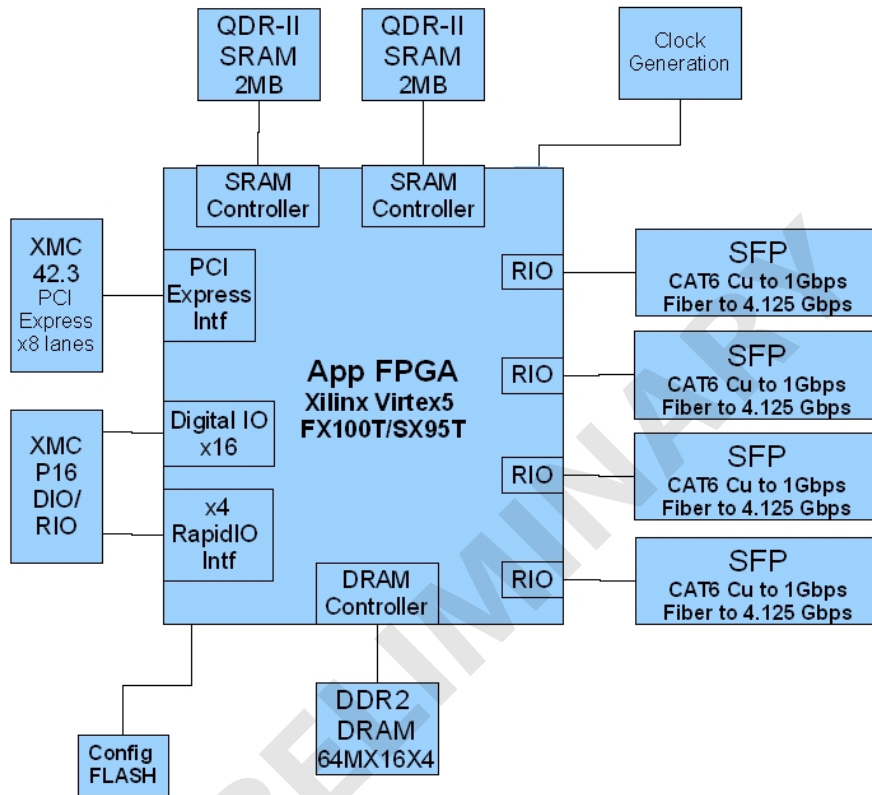
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Standard Features

Front Panel Communications Ports	
Ports	4 gigabit serial ports in FPGA (a.k.a. Rocket IO or GTP/GTX ports)
Data Rates (Max)	4.125 Gbps (FX100T) 3.2 Gbps (SX100T) simultaneously in each direction, per port
Interface	SFP module (Small Form-factor Pluggable)
Cables	CAT6 Ethernet cable to ~1Gbps Fiber to 4.125 Gbps
Transmission Distance	CAT6 to ~10 meters Fiber to 10 km (module and cable dependent)
IO Type	CML

Memories	
DRAM Size	512MB total 4 devices @ 64Mx16 each
DRAM Type	DDR2 DRAM
DRAM Controller	Controller for DRAM implemented in logic. DRAM is controlled as a single bank.
DRAM Rate	4.2 GB/s storage/retrieval rate sustained
SRAM Size	4 MB total 2 devices @ 512Kx32 each
SRAM Controller	Two independent SRAM controllers implemented in FPGA logic
SRAM Type	QDR-II
SRAM Rate	3.2 GB/s storage/retrieval max rate sustained

FPGA	
Devices	Xilinx Virtex5 Option -0: XC5VSX95T-1FF1136C Option -1: XC5VFX100T-1FF1136C
Speed Grade	-1 (commercial)
Pins	1136
Size	~10M gate equivalent (standard device)
Flip-Flops	SX95T: 58880 FX100T: 64000
DSP48E cores	SX95T: 640 FX100T: 256
CLB	SX95T: 14720 FX100T: 16000
Block RAMs	SX95T: 488 (8748 Kbits) FX100T: 456 (8208 Kbits)
Rocket IO	SX95T: 16 lanes @ 3.2 Gbps FX100T: 16 lanes @ 4.125 Gbps
Ethernet MAC	4 per device 802.3-2002 compliant UNH verified Supports jumbo frames DCR bus to microprocessors
Configuration	SelectMAP from on-board flash EEPROM - JTAG during development

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Host Interface	
Type	PCI Express; 8 lanes
Sustained Data Rate	1 GB/s each direction simultaneous
Protocol	PCI Express with Velocia packet system
Connector	XMC P15
Interface Standard	PCIe 1.0a; VITA 42.3
Logic Update	In-system reconfiguration

Clocks and Triggering	
Clock Sources	125 MHz clock (other frequencies may be special ordered)
Jitter	<200 fs RMS

P16 Interfaces	
Rocket IO Channels	4
Rocket IO data rate	SX95T: 3.125 Gbps/lane FX100T : 4.125 Gbps/lane Effective rate is 80% of max when 8b/10b data encoded
DIO Bits, total	16
Signal Standard	LVTTL (0 to 3.3V max)
Drive	+/-12 mA (adjustable in FPGA)
Connector	XMC P16

Power Management	
Temperature Monitor	May be read by the host software
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables power supplies above 85C FPGA die temperature
Power Control	Port enables and power up enables from FPGA
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	130g (excludes SFPs)
Hazardous Materials	Lead-free and RoHS compliant

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ABSOLUTE MAXIMUM RATINGS				
Exposure to conditions exceeding these ratings may cause damage!				
Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	+3.0	+3.6	V	
Supply Voltage, VPWR to GND	+4.5	+16	V	
Analog Input Voltage, Vin+ or Vin- to GND	-6	+6	V	
Operating Temperature	0	70	C	Cooling is required for operation. Convection cooling must be non-condensing.
Storage Temperature	-65	+150	C	
ESD Rating	-	1k	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

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RECOMMENDED OPERATING CONDITIONS					
Parameter	Min	Typ	Max	Units	Conditions
Supply Voltage	+3.15	+3.3	+3.45	V	
Operating Temperature	0		60	C	Cooling is required.
Forced Air Cooling	2**	10	-	CFM	** All systems should be characterized to determine the cooling requirements.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
Power Consumption	15	W	FPGA system clock @ 250 MHz, all RIO ports operating, 300 mW SFP per port, 22C ambient; specific applications may be may vary from 12 to 25W
Mean Time Between Failures (MTBF)	TBD	hours	

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Architecture and Features

The X5-COM module architecture integrates high speed gigabit serial communications ports (GBT) with an FPGA computing core, memories and PCI Express host interface. This architecture tightly couples the FPGA to the communications, enabling the module to perform real-time signal processing with low latency and extremely high rates. Integration within the FPGA logic array of the GBT ports, Ethernet MACs, and PowerPC processors (FX100T) make it the X5-COM ideal for demanding applications in Ethernet packet processing, wireless IF processing, and electronic warfare applications.

Communications Ports

The X5-COM module has four independent communications ports using Virtex5 integrated serial data GTP/GTX ports. With supporting logic, the ports can implement a variety of high speed communications protocols including Ethernet, Aurora, Serial Rapid IO, Fiber Channel and many others. Logic cores for most standard protocols can be purchased.

The communications ports can be programmed for a variety of data rates, protocols and flow control features for custom applications. Network test equipment can synchronize multiple ports for data transmission and receive testing with absolute data alignment since all ports are in the FPGA.

The communications ports are clocked using a low-jitter PLL on the X5-COM. The PLL provides software programmable clocks to the GTPs and supports most standard bit rates. Multiple modules can be synchronized for simultaneous operation.

SFP Interface Modules

Each GTP port uses an SFP module for its cable interface on the front panel. SFP modules are industry-standard IO modules that provide the physical interface for the GTP port connection to copper or fiber optic cable. Standard cables such as CAT6 Ethernet or fiber optic cables can be used with the SFP modules.

SFP and cables are selected for the required data rate, transmission distance, and operating environment. In general CAT6 is limited to about 10 meters at 1 Gbps while fiber optic cables can provide rates up to 4.125 Gbps and distances up to 10 km.

An SPF module

The SFP modules can be monitored for signal loss and presence by the FPGA.

SFP modules are NOT provided with the module.

FPGA Core

The X5 Module family has a Virtex5 FPGA and memory at its core for embedded processing, DSP and control. The X5-COM is available with either the Virtex5 SX95T for DSP applications, or the FX100T for embedded computing. The Virtex5 SX95T FPGA is capable of $>300 \times 10^9$ MACs (operating at 500 MHz internally), about 20x faster than competing DSPs. The FX100T has two Power PC processors in the FPGA in addition to DSP and memory elements.

The FPGA fabric integrates logic, memory and connectivity features that make the FPGA a powerful computing engine for f virtually any algorithm and and providing sustained performance in real-time. The FPGA has direct access to 512 MB of DDR2 DRAM capable of >4 GB/s data transfer rate and 4 MB or QDR II SRAM capable of 4GB/s data rate. The QDR memory is composed of two independent banks of 2 MB (512Kx32). These memories can be used for either PowerPC memory or to allow the FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for system data buffering and algorithms like Doppler delay. A multiple-queue controller component in the FPGA
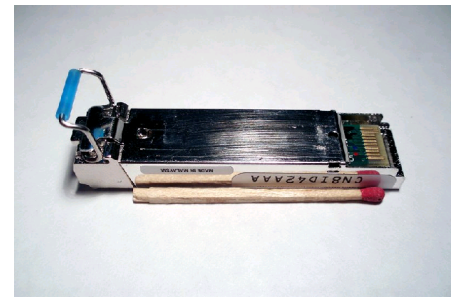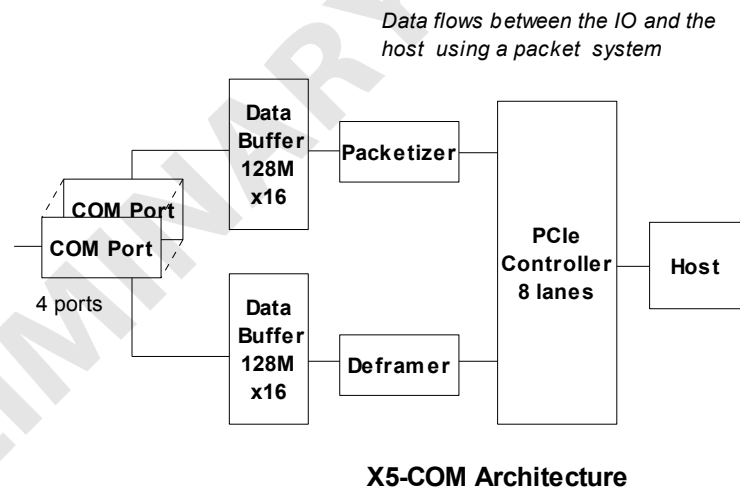
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implements multiple data buffers in the DRAM that is used for system data buffering and algorithm support.

The FX100T FPGA has dual PowerPC processors in the FPGA for embedded processing applications such as Ethernet packet processing and communications control. These PowerPC processors can be tightly integrated with the communications and memories that are connected to the FPGA. External QDR memory provides excellent computing and data storage for the processors so that two independent PowerPC computing cores can be supported. Demanding applications such as data encryption/decryption can be performed real-time using the PowerPC and FPGA processing capabilities.

The X5 module family uses the Virtex5 FPGA as a system-on-chip to integrate all the features for highest performance. As such, all IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Firmware for the FPGA completely defines the dataflow, signal processing, controls and host interfaces, allowing complete customization of the X5 module functionality.

PCI Express Host Interface

The X5 architecture delivers over 1 GB/s sustained data rates over PCI Express using the Velocia packet system. The Velocia packet system is an application interface layer on top of the fundamental PCI Express interface that provides an efficient and flexible host interface supporting high data rates with minimal host support. Using the Velocia packet system, data is transferred to the host as variable sized packets using the PCIe controller interface. The packet data system controls the flow of packets to the host, or other recipient, using a credit system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the GTP ports, or as occasional packets for status, controls and analysis results. For all types of applications, the data buffering and flow control system delivers high throughput with low latency

Data flows between the IO and the host using a packet system

X5-COM Architecture

and complete flexibility for data types and packet sizes to match the application requirements. Firmware components for assembling and dissembling packets are provided in the FrameWork Logic that allow applications to rapidly integrate data streams and controls into the packet system with minimum effort.

The PCI Express interface is implemented in the Virtex5 FPGA using 8 Rocket IO ports, for a maximum bit rate of over 20 Gbps, full duplex. Data encoding and protocol limit practical in-system data rates to about 200 MB/s per lane. Since PCI Express is not a share bus, but rather a point-to-point channel, system architectures can achieve high sustained data rates between devices – resulting in higher system-level performance and lower overall cost.

Private Data Links

The X5 module family has private data links on the P16 connector that can be used for system integration. The X5-COM P16 connector has 4 Rocket IO links, each capable of 3.125 Gbps, and 16 sideband signals. The 4 RIO lanes can be used to provide low-latency, high rate data to the system in addition to the PCI Express interface. Maximum data rates, with deterministic performance can be implemented in performance-driven systems using little or no protocol. For more complex systems, protocols such as Rapid IO or Aurora can be used.

FPGA Configuration

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Logic loads from on-board FLASH memory on power-up. The X5 modules have a 128Mb FLASH that holds the FPGA application image. The FLASH can be reprogrammed in-system using a software applet for field upgrades.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB or Parallel IV cable.

Thermal Monitoring and Cooling

The X5-COM logic provides FPGA temperature monitoring that is used to prevent overheating. If the temperature exceeds the maximum safe operating temperature (85C for commercial temperature range devices), then the module power supplies are turned off to prevent damage. The temperature can also be read by software for system health monitoring.

Conductive cooling for the module is provided through two cooling bar attachment areas along the edges. These cooling bar areas are connected to a thermal plane in the PCB that spreads heat and conducts from the devices to the bars. For convection cooling, the thermal plane provides a larger surface area and also spreads heat to the bracket for better cooling.

Software Tools

Software development for the Xilinx Virtex5 PowerPC processors is supported by the Xilinx Platform Studio (XPS) and Embedded Development Kit (EDK). XPS features a graphical IDE with GNU C/C++ compiler and debugger and is specifically designed to support high performance embedded applications. The XPS software suite includes libraries for device driver generation and board support. Download and software debug use the Xilinx JTAG port and JTAG cable. More advance supported for embedded OS such as Linux are supported through third parties such as Wind River and Green Hills.
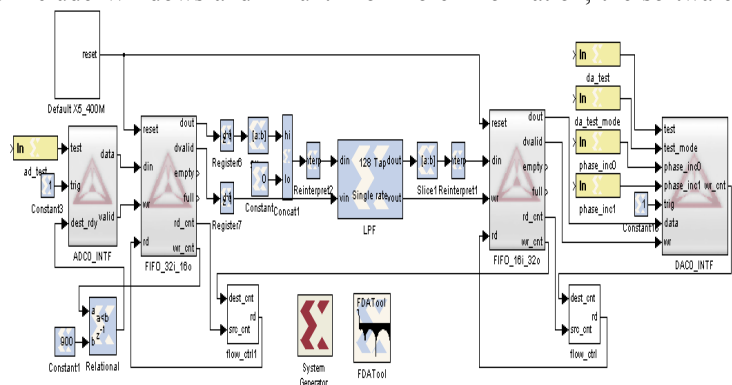
Host software development tools for the X5 modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every X5 module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for MS Visual C++ is provided. Supported OS include Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the X5 modules by modifying the logic. The FrameWork Logic tools provide support for RTL and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designers can build upon the Innovative

Using MATLAB Simulink for X5 Logic Design

components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. Each design is provided as a Xilinx ISE project, with a ModelSim testbench illustrating logic functions and providing a starting point for your application.

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The MATLAB Board Support Package (BSP) allows logic development using Simulink and Xilinx System Generator. These tools provide a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

The FrameWork Logic User sales brochure and User Guide more fully detail the development tools.

Applications Information

Ethernet Support

The X5-COM makes a unique, high performance platform for Ethernet test, packet processing, data security and monitoring applications because of Virtex5 FPGA. The Virtex5 FX100T has four Ethernet MACs in the FPGA logic that can be used with the 4 front panel communication ports for either copper or fiber optic links. The MACs provide support for 10/100/1000 Ethernet interfaces and provide low-level access to the data stream. With the PowerPC cores and logic, there is ample processing power for high performance data processing for each port.

Remote IO Interface

Applications for remote IO with parallel digital interfaces, such as I/Q data from receivers or network test equipment, can be connected to the X5-COM using the a parallel to serial conversion application card. An example design is provided showing interface to the X5-COM via high speed serial links for parallel digital IO. The application card has 4 serial channels and SFP ports that can act as simple data "pipes" to the X5-COM communication ports. Data is written with a clock and enable into the DIO ports and is piped to the X5-COM over the serial links. The X5-COM can then be used to generate or receive data from the application card.

IP Support

Logic cores for the X5-COM are available for many functions such as communications protocols, data encryption/decryption, error correction and data analysis.

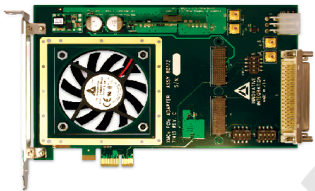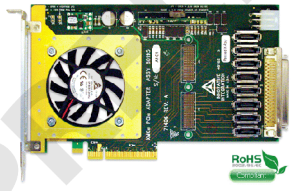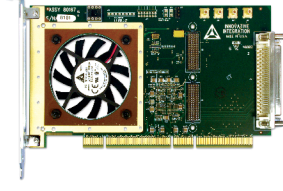| Function	IP Cores	Features	Supplier
Communications	Ethernet 10/100/1000 Core	Supports Xilinx Virtex5 integrated GTP and MAC features	Xilinx
	Aurora	Supports data rates up to ~1500GB/s with low overhead	Xilinx
	Serial RapidIO	Industry-standard data plan connectivity that supports data rates up to ~1500 GB/s	Xilinx
Channelizers	Up to 32 wideband, independent channels	1MHz channel width, 250 MSPS input rate, >90 dB dynamic range, resampler, 0.1Hz tuning, programmable filter	Innovative
	64/128/256 channels	Up to Fs/80 channel width, 250 MSPS max input rate, >85 dB dynamic range, resampler, 32-bit tuning resolution, programmable filter	Innovative
	8-4096	Up to Fs/10 channel width, 250 MSPS max input rate, >90 dB dynamic range, resampler, 32-bit tuning resolution, programmable filter	Innovative

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Forward Error Correction	Reed-Solomon, LDPC, Viterbi, Turbo	Supports standards GMR-1, GMR-2, GSM. WCDMA, 802.11, 80.16, DVB-T, DVB-S, INMARSAT	Innovative
Modem	FSK, BPSK, O-QPSK, 8PSK, 16-QAM	Satellite communications	Innovative

XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXI using a XMC adapter card. An auxiliary power connector to the PCI Express adapters provides additional power capability for XMC modules when the slot is unable to provide sufficient power. The adapter cards allow the XMC modules to be used in any PCIe or PCI system.

The X5 module family uses the auxiliary P16 connector as a private host interface. Eight Rocket IO lanes with 16 LVTTL signals provide support for data transfer rates up to 1.6 GB/s sustained, as well as sideband signals for control and status. Protocols such as Serial Rapid IO and Aurora may be implemented for host communications or custom protocols.

Note that the high speed Rocket IO lanes require a host card electrically capable of supporting the high speed signal pairs. Only the eight lane adapter, P/N 80195 is suitable for high speed P16 applications.

PCIe-XMC Adapter (80172)	**PCIe-XMC Adapter x8 lane (80173)**	**PCI-XMC Adapter (80167)**	**Compact PCI-XMC Adapter (80207)**
x1 PCIe to XMC	x8 PCIe to XMC	64-bit, 133 MHz PCI-X host	64-bit, 133 MHz PCI-X host
Clock and trigger inputs	x8 RIO ports supported on P16	x4 PCIe to XMC	x4 PCIe to XMC
			PXI triggers and clock support

Applications that need remote or portable IO can use either the eInstrument PC or eInstrument Node with X3 modules.

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eInstrument PC with Dual PCI Express XMC Modules (90199)

Windows/Linux embedded PC

8x USB, GbE, cable PCIe, VGA

High speed x8 interconnect between modules

GPS disciplined, programmable sample clocks and triggers to XMCs

100 MB/s, 400 GB datalogger

12V operation

eInstrument DAQ Node – Remote IO using cabled PCI Express (90181)

PCI Express system expansion

Up to 7 meter cable

electrically isolated from host computer

software transparent

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