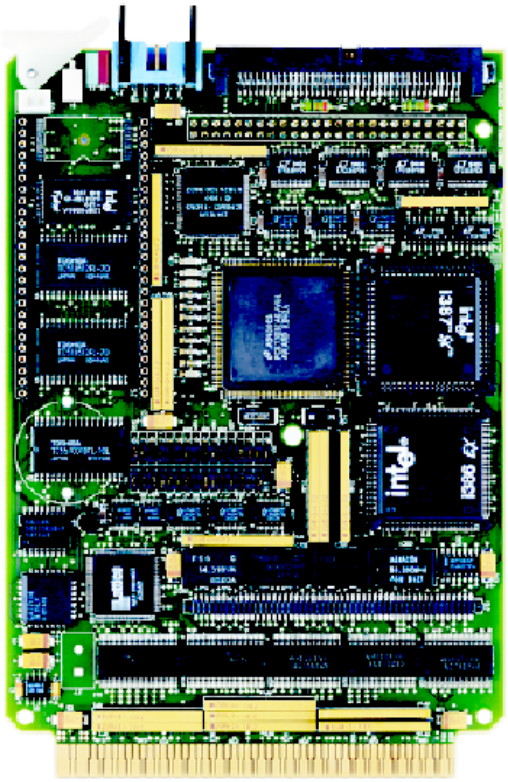
ZT 8903
ZT 8904
ZT 89CT04



Single Board 386 EX Computer

Hardware User Manual

ZIATECH CORPORATION

CONTENTS

MANUAL ORGANIZATION

The ZT 8904 family of products includes the ZT 8904, ZT 89CT04, and ZT 8903 products. The ZT 8904 is a highly integrated 386 EX single board computer which can be operated as a stand alone, as a single master in an STD 32 architecture, or as a permanent or temporary master in an STD 32 architecture.

All features of the ZT 8903 and ZT 8904 are the same, except that the ZT 8903 includes fewer features. The ZT 8903 is a more economical version of the ZT 8904 because of fewer features are included.

All features of the ZT 8904 and ZT 89CT04 are the same except for the temperature variations. The ZT 8904 has an operating temperature range from 0º to 65º C, but the ZT 89CT04 extends the operating temperature range from -40º to +85º C.

Chapter 1, "**Introduction**", provides a brief introduction to the ZT 8904. It includes a product definition, a list of product features, a functional block diagram, a description of each block, and a diagram locating the major components of the board.

Chapter 2, "**Getting Started**", summarizes the information needed to make the ZT 8904 operational. Read this chapter before attempting to use the board.

Chapter 3, "**STD Bus Interface**", discusses the STD 32 architecture and its effect on the operation of the ZT 8904.

Chapter 4, "**Interrupt Controller**", includes information on two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU.

Chapter 5, "**Counter/Timers**", includes information on one Intel-compatible 8254 device with a total of three programmable counter/timers.

Chapter 6, "**DMA Controller**", includes information regarding the DMA controller which is contained within the 386 EX microprocessor.

Chapter 7, "**Real-Time Clock**", includes information on the Motorola®-compatible 146818 real-time clock including the major features.

Chapter 8, "**Serial Controller**", discusses operation of the four ZT 8904 serial ports and provides descriptions of the two software-configurable serial port registers included on the ZT 8904.

Chapter 9, "**Centronics Printer Interface**", includes information on the bidirectional printer interface which fully supports a Centronics-compatible printer.

Chapter 10, "**Parallel I/O**", discusses the six 8-bit parallel ports for a total of 48 I/O signals. The general operation of the six parallel ports is explained in this chapter.

Chapter 11, "**System Registers**", discusses the three system registers used to control and monitor a variety of functions on the ZT 8904.

Chapter 12, "**Watchdog Timer**", lists the major features of the watchdog timer which monitors the ZT 8904 operation and takes corrective action if the system fails to function as programmed.

Chapter 13, "**Local BUS Video**", includes information on the local bus interface which permits high speed peripherals direct access to the CPU bus.

Chapter 14, "**Numeric Data Processor**", discusses how the numeric data processor extends the CPU instruction set to include trigonometric, logarithmic, and exponential functions.

Chapter 15, "**Programmable LED**", discusses the ZT 8904's two Light-Emitting Diodes (LEDs).

Chapter 16, "**AC Power Fail**", includes information on the AC power-fail detection as a means for giving the application advanced warning of an impending power failure.

Appendix A, "**Jumper Configurations**", demonstrations how the ZT 8904 offers several options tailoring the operation of the board to requirements of specific applications. The "Jumper Cross Reference" table is included.

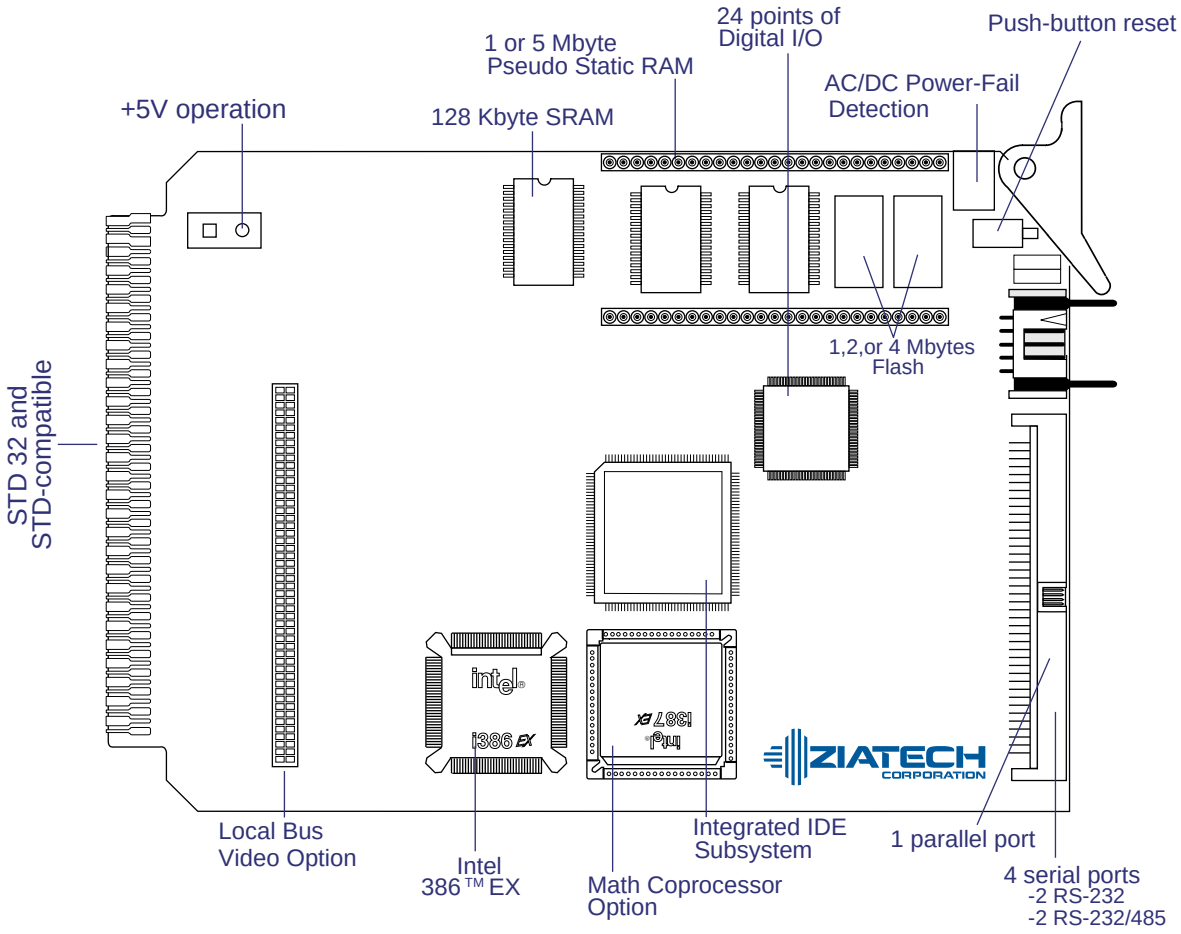
Appendix B, "**Specifications**", describes the electrical, environmental, and mechanical specifications of the ZT 8904. It includes illustrations of the board dimensions, the P/E connector pinouts, and cables commonly used with the ZT 8904. Also shown are tables listing the pin assignments for the ZT 8904's 10 connectors.

Appendix C, "**PIA System Setup Considerations**", discusses the 16C50A Parallel Interface Adapter (PIA) device used on the ZT 8904. It is designed by Ziatech to offer bidirectional I/O signals with or without event sense capability.

Appendix D, "**Customer Support**", offers technical assistance information for this product, and also the necessary information should you need to return a Ziatech product.

1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8904. It includes a product definition, a list of product features, a functional block diagram, a description of each block, and a diagram locating the major components of the board. Unpacking information and installation instructions are included in Chapter 2, "Getting Started."



Major Components

PRODUCT DEFINITION

The ZT 8904 family of products includes the ZT 8904, ZT 89CT04, and ZT 8903 products. The following topics describe these products. Using the ZT 8904 without the STD bus, as a single bus master, and as an STD 32® multiple master are also discussed.

ZT 8904

The ZT 8904 is a highly integrated 386 EX single board computer. The board meets the needs of a wide range of industrial control and processing applications by operating stand alone, as a single master in an STD 32 architecture, or as a permanent or temporary master in an STD 32 architecture.

ZT 89CT04

The ZT 89CT04 extends the ZT 8904 operating temperature range from 0 to 65º C to -40º to +85º C. Except for the temperature variations, all other features of the ZT 8904 and ZT 89CT04 are the same. Unless explicitly stated otherwise, all references in this manual to the ZT 8904 include the ZT 89CT04.

ZT 8903

The ZT 8903 is a more economical board that includes all the features of the ZT 8904 except those listed below. Unless explicitly stated otherwise, all references in this manual to the ZT 8904 include the ZT 8903 as well.

- ZT 8904 supports an IDE drive option not available on the ZT 8903
- ZT 8904 supports a multiprocessing option not available on the ZT 8903
- ZT 8904 includes RS-485 support not available on the ZT 8903
- ZT 8904 includes four serial ports and the ZT 8903 includes two
- ZT 8904 includes 128 Kbytes of battery-backed RAM not available on the ZT 8903

Stand Alone

The ZT 8904 does not require an STD bus backplane to operate. The ZT 8904 is able to operate stand-alone in many applications because of the large selection of the most commonly needed peripheral devices. A power connector location and four mounting holes are available for stand-alone operation.

STD 32 Single Master

The ZT 8904 supports additional memory and I/O through the STD bus. In an STD 32 architecture, data transfers are dynamically adjusted to support 8-bit and 16-bit boards.

STD 32 Multiple Master

The ZT 8904 can be configured to operate as a permanent master or as a temporary master in a multiple master architecture. With this architecture, up to seven ZT 8904 boards share STD bus memory and I/O resources. The ZT 8903 does not support multiple master operation.

FEATURES

- STD 32 compatible
- STD 32 multiprocessing option (not supported by ZT 8903)
- 25 MHz Intel® 386 EX CPU
- Numeric data processor socket
- Optional local bus video support
- 128 Kbyte battery-backed Static RAM (not supported by ZT 8903)
- 1, 2, or 4 Mbytes of Flash memory
- 1 or 5 Mbytes of RAM memory
- Standard AT® peripherals include:
  - Interrupt controllers (8259)
  - Counter/timers (8254)
  - Real-time clock/CMOS RAM (146818)
  - DMA controller (8237)
- Additional AT® peripherals include:
  - Two RS-232 serial channels
  - Two RS-232/485 DMA capable serial channels (not supported by ZT 8903)
  - IEEE 1284 parallel port (Centronics, ECP, EPP)
  - Optional IDE disk drive (not supported by ZT 8903)
- 24-point digital I/O with interrupt driven event sense and programmable debounce
- Two stage watchdog timer
- Pushbutton reset
- Software programmable LED
- AC/DC power monitor
- +5 V-only operation (Local charge pump for RS-232 and Flash programming)
- Compatible with the following software: MS-DOS®, OS/2®, UNIX®, QNX®, VRTX32®, and Windows® 3.1
- STD bus standard 4.5" x 6.5" board format
- DOS or STAR BIOS options
- Burned in at 55º Celsius and tested to guarantee reliability
- Five year warranty

DEVELOPMENT CONSIDERATIONS

Ziatech offers a variety of software options for ZT 8904 applications. These options include STD ROM, STAR BIOS, and Ziatech's Industrial BIOS. Contact the Ziatech for additional options.

STD ROM allows programmers to develop ROM-based applications without the use of an operating system. STD ROM connects the ZT 8904 to an IBM-compatible personal computer through a high speed serial link. The computer is used as a development station to create, download, and debug applications written in assembly, C, and other popular programming languages. The Paradigm Systems DEBUG/RT used during the debug phase includes source level debugging, single step execution, breakpoints and watchpoints.

The Ziatech Industrial BIOS provides the standard MS-DOS environment and services in Flash memory on the ZT 8904. Ziatech Industrial BIOS provides standard support for common peripherals and is supported by many third party development tools such as program editors, compilers, assemblers, and debuggers. Refer to the Ziatech system manual for configuration and operating instructions.

STAR BIOS is the DOS platform operating on more than one master in a single STD bus system. Each master supports the Ziatech Industrial BIOS operating environment and is capable of sharing STD bus memory and I/O, such as fixed disks, floppy disks, and video. Refer to the STD 32 STAR SYSTEM™ operating manual for configuration and operating instructions. The STAR BIOS is not available for the ZT 8903.

FUNCTIONAL BLOCKS

The "Functional Block Diagram" on the next page illustrates the board's major functional blocks. A description of the board's features and functional blocks is listed found in the following topics.

STD Bus Interface

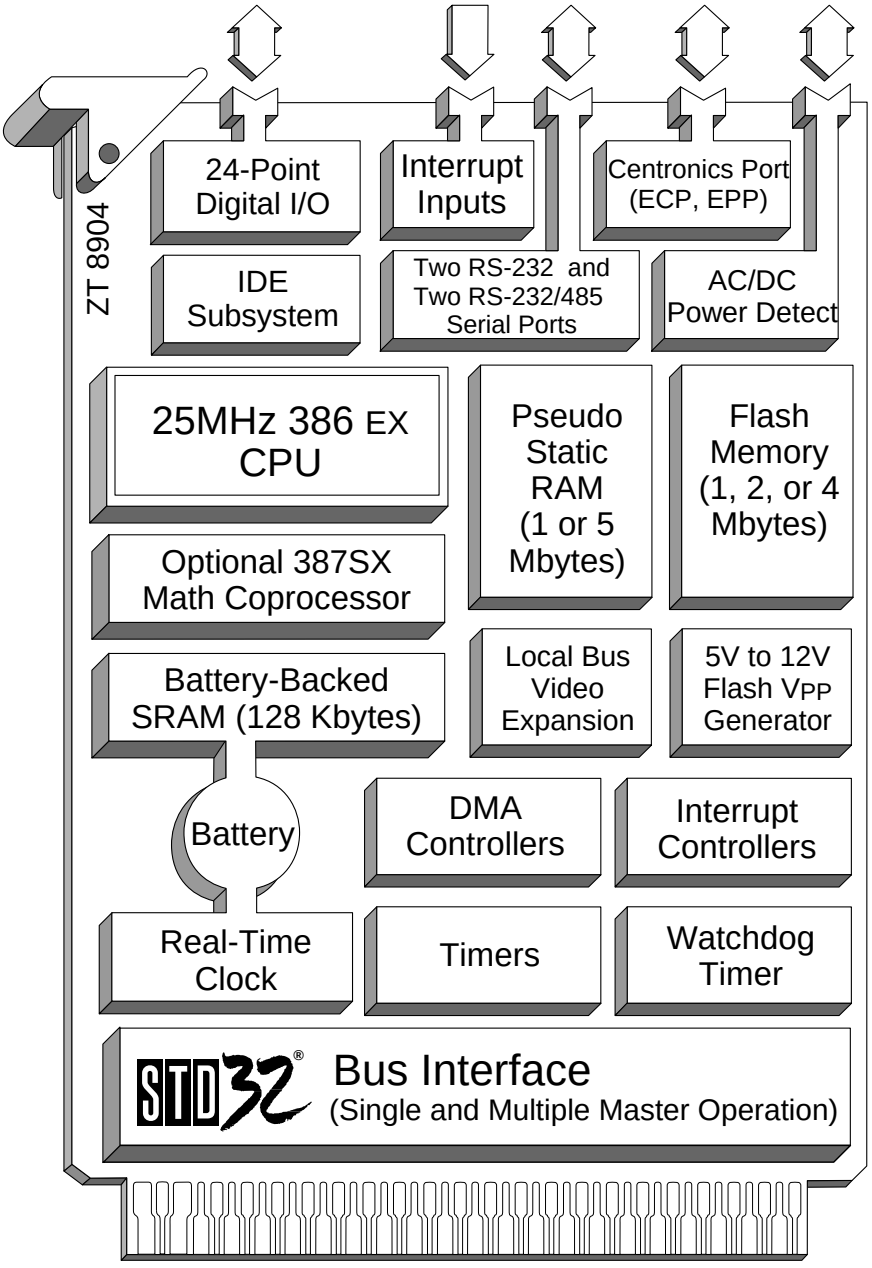
The ZT 8904 operates in STD 32 systems. In an STD 32 system, data transfers are dynamically sized for either 8 bits or 16 bits. STD 32 compatible memory and I/O boards are dynamically sensed to determine the width of the data transfer.

In addition to 16-bit data transfers, the STD 32 system provides the platform needed for multiple master operation. In a multiple master system, up to seven ZT 8901, ZT 8902, or ZT 8904 boards share STD bus resources with a fixed or rotating priority granted by an external bus arbiter, such as the ZT 89CT39. The ZT 8903 does not support multiple master operation.

See Chapter 3, "STD Bus Interface" for more information.

386 EX CPU

The ZT 8904 supports the Intel 386 EX CPU operating at 25 MHz. The 386 EX is a fully static 32-bit CPU core integrated with standard PC peripherals. Integrated peripherals include serial controller, interrupt controller, DMA controller, counter/timers, and watchdog timer. The 386 EX supports a 64 Mbyte memory address space and a 64 Kbyte I/O address space.



Functional Block Diagram

Memory and I/O Addressing

The ZT 8904 includes 1 Mbyte of system RAM, 1, 2, or 4 Mbytes of Flash, and 128 Kbytes of battery-backed RAM. The battery-backed RAM is not available on the ZT 8903. System RAM can be expanded from 1 Mbyte to 5 Mbytes with the addition of an optional memory module. Memory operations up to 16 Mbytes that are not decoded by local memory devices are directed to the STD bus.

Data transfers are dynamically adjusted to support standard architecture STD bus memory boards with an 8-bit or 16-bit data path. The memory architecture selected for the Ziatech Industrial BIOS architecture is shown in the "Memory Address Map" in Chapter 2.

The ZT 8904 also includes many I/O peripherals required for industrial control applications. I/O operations up to 64 Kbytes not decoded by local I/O devices are directed to the STD bus. The STD bus I/O expansion signal, IOEXP, is supported to limit the addressing redundancy of I/O boards decoding fewer than 16 bits of address. Data transfers are dynamically adjusted to support standard architecture STD bus I/O boards with an 8-bit or 16-bit data path. A20 is located at port 92h. Set bit 1 to 1 for disable, 0 for enable. The I/O map architecture selected for the Ziatech Industrial BIOS architecture is shown in the "I/O Address Map".

Local Bus Video

The ZT 8904 supports both STD bus and local bus video adapters. For STD bus video, Ziatech offers video boards that support VGA and flat panel displays. For local bus video, Ziatech offers zVID adapters that plug directly onto the ZT 8904 J6 local bus connector. Local bus video is up to 300% faster than STD bus video because the data transfers occur at the CPU operating speed of 25 MHz. For space-constrained applications, the zVID offerings have the added advantage of not requiring the additional card cage slot needed by the STD bus offerings.

Serial I/O

The ZT 8903 includes two RS-232 serial ports. The ZT 8904 and ZT 89CT04 include four RS-232 serial ports, two of which can be software configured for RS-485 operation. COM1 and COM2 are 16C450 compatible UARTs. COM3 and COM4 are 16C550 compatible UARTS. All of the serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115 Kbaud, and are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply.

The 386 EX multiplexes COM2 data and handshake signals with DMA signals. This results in the loss of COM2 handshake if STD bus DMA is used and the complete loss of COM2 if local printer or serial DMA is used. This selection is controlled with jumpers W24 through W27 and BIOS configuration.

The serial ports are configured as DTE and are available through the J1 80-pin frontplane connector. Optional cables convert the serial port interface to standard 9-pin D-shell connectors. The ZT 90200 cable provides the serial interface for the ZT 8904 and ZT 89CT04. The ZT 90203 cable provides the serial interface for the ZT 8903. A null-modem option is required to convert the DTE configuration to DCE.

See Chapter 8, "Serial Controller" for more information.

IEEE 1284 Parallel Port

The ZT 8904 includes an IEEE 1284 parallel port for supporting Centronics, EPP, and ECP devices. The parallel port interface is available through the J1 80-pin frontplane connector. An optional cable converts the parallel port interface to a standard 25-pin D-shell connector. The ZT 90200 cable provides the parallel interface for the ZT 8904 and ZT 89CT04. The ZT 90203 cable provides the parallel interface for the ZT 8903.

See Chapter 9, "Centronics Printer Interface" for more information.

Parallel I/O

The ZT 8904 includes three 8-bit parallel I/O ports for a total of 24 parallel I/O lines. Each line is programmable as an input or an output with readback. The outputs sink 12 mA and do not glitch during power cycles. The 24 lines, available through the J4 50-pin frontplane connector, also support software programmable signal debounce and event sense interrupt generation.

An optional cable (ZT 90072 Digital I/O Cable) connects the parallel I/O interface to an 8, 16, or 24 position I/O module mounting rack, such as Ziatech's ZT 2226 24-Channel I/O Mounting Rack or those offered by Opto 22®.

See Chapter 10, "Parallel I/O" for more information.

Interrupts

Two interrupt controllers provide a total of 15 interrupt inputs. Interrupt controller features include support for level-triggered and edge-triggered inputs, fixed and rotating priorities, and individual input masking. Interrupt sources include counter/timers, serial I/O, parallel I/O, real-time clock, keyboard, printer, optional IDE drive, and multiple master communications. There are also three frontplane and four STD bus interrupt sources. Frontplane interrupts are available via connector J2.

See Chapter 4, "Interrupt Controller" for more information.

Timers

Three timers are included on the ZT 8904. Operating modes supported by the timers include interrupt on count, frequency divider, square wave generator, software triggered, hardware triggered, and one shot. The number of counter/timers available to the application programmer depends on the operating system.

For example, the Ziatech MS DOS operating system uses timer 0 to generate system tick and timer 2 to control the speaker. Timer 1 is available to the application.

See Chapter 5, "Counter/Timers" for more information.

DMA

One DMA controller provides two DMA channels for data transfers between local or system I/O and local memory. DMA channel 0 supports both 8-bit and 16-bit STD bus DMA slaves. The primary use for STD bus DMA is floppy disk expansion. Optionally, DMA channel 0 supports the local 1284 parallel port or combines with DMA channel 1 to support one of the local serial ports.

See Chapter 6, "DMA Controller" for more information.

Watchdog Timer

The two-stage watchdog timer optionally monitors system operation. Failure to strobe the first stage within a programmable time period results in a non-maskable interrupt. Failure of the non-maskable interrupt service routine to restart the watchdog results in a stage two reset.

See Chapter 12, "Watchdog Timer" for more information.

Real-Time Clock

The real-time clock performs timekeeping functions and includes more than 200 bytes of general-purpose battery-backed CMOS RAM.

Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar.

CMOS RAM available to the application programmer depends on the operating system. For example, the Ziatech MS DOS operating system uses the CMOS RAM to store configuration parameters.

See Chapter 7, "Real-Time Clock" for more information.

Keyboard Controller

The ZT 8904 includes a PC/AT® keyboard controller that operates when the zVID local bus video adapter is installed. The keyboard connector is located on the zVID adapter.

AC Power-Fail Protection

With the addition of an AC transformer (connected to connector J3), the ZT 8904 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the CPU of an impending power failure. When the application software receives this notification, it saves critical data before the CPU is reset.

See Chapter 16, "AC Power Fail," for more information.

2. GETTING STARTED

This chapter summarizes the information needed to make the ZT 8904 operational. Read this chapter before attempting to use the board.

UNPACKING

Please check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 8904.

Do not return any product to Ziatech without a Return Material Authorization (RMA) number. Refer to Appendix D, "Customer Support," which explains the procedure for obtaining an RMA number from Ziatech.

Warning: Like all equipment utilizing MOS devices, the boards must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with your order to handle the boards.

SYSTEM REQUIREMENTS

The ZT 8904 is designed for use with or without an STD bus backplane. The ZT 8904 is electrically, mechanically, and functionally compatible with the *STD 32 Bus Specification* (ZT MSTD32) for STD bus applications. An STD 32 system is required for 16-bit data transfers to other STD bus boards and for multiple master operation. The ZT 8903 does not support multiple master operation.

Ziatech recommends vertical mounting and the use of a fan to provide the required airflow. Refer to Appendix B, "Specifications," for additional specifications.

MEMORY CONFIGURATION

The ZT 8904 addresses 64 Mbytes of memory using a 26-bit memory address. The memory map is programmable through the CPU chip select registers. The memory architecture selected for the Ziatech Industrial BIOS architecture is shown in the "Memory Address Map" figure. The ZT 8904 memory map includes several types of memory.

System RAM - 16-bit pseudo static RAM

- Video RAM - located on the STD bus or zVID memory board
- Video BIOS - 16-bit pseudo static RAM shadowed from video board

- Local RAM Drive - 8-bit battery-backed RAM (not available on the ZT 8903) paged for 128 Kbytes
- System BIOS - 16-bit pseudo static RAM shadowed from Flash #0
- Extended RAM - Optional 16-bit pseudo static RAM module
- Flash #0 - 8-bit Flash
- Flash #1 - Optional 8-bit Flash
- STD bus Expansion - 8-bit or 16-bit expansion memory
- Reserved - Not available

STD bus expansion memory is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 1.5 Mbytes/second for 16-bit data. The ZT 8904 supports the STD bus wait request signal, WAITRQ*, to interface to memory boards with longer access time requirements than those defined by zero wait state STD 32 specifications. During local memory operations, the STD bus is held static to decrease system electrical noise and power consumption.

The ZT 8904 supports 128 Kbyte battery backed RAM (BRAM) devices. BRAM is paged into the system memory map in 64 Kbyte increments at 0xD0000h through 0xDFFFFh. Paging is performed by writing specific values to bits D4, D3 and D2 of System Register 0 (0X7Bh). BRAM pages are selected as follows:

- Write XXXX111Xh to select BRAM page 0
- Write XXXX110Xh to select BRAM page 1

If larger BRAM devices are installed, use sequential codes to select subsequent pages in the memory map. Note that specific BRAM pages are used by both the Ziatech Single Master BIOS and by the STAR System BIOS. The Ziatech Technical Support Group can provide example code for using ZT 8904 BRAM.

180000h-3FFFFFh	RESERVED
140000h-17FFFFh	FLASH #0
100000h-13FFFFh	FLASH #1
080000h-0FFFFFh	STD BUS EXPANSION
050000h-07FFFFh	RESERVED
010000h-04FFFFh	EXTENDED RAM EXPANSION MODULE
00E000h-00FFFFh	SYSTEM BIOS
00D000h-00DFFFh	LOCAL RAM DRIVE STD BUS EXPANSION
00C800h-00CFFFh	STD BUS EXPANSION
00C000h-00C7FFh	VIDEO BIOS
00A000h-00BFFFh	VIDEO RAM
000000h-009FFFh	SYSTEM RAM

Memory Address Map

I/O CONFIGURATION

The ZT 8904 addresses up to 64 Kbytes of I/O using a 16-bit I/O address. The I/O map is programmable through the CPU configuration registers. The I/O map architecture selected for the Ziatech Industrial BIOS architecture is shown in the "I/O Address Map" figure following.

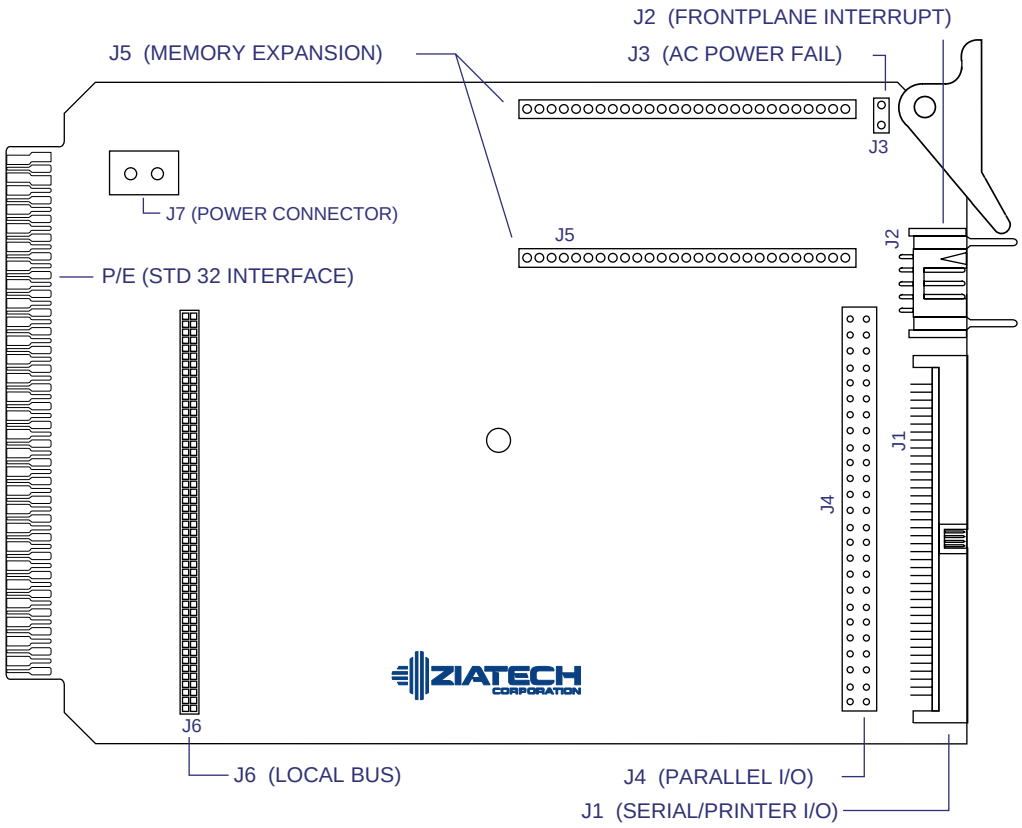
STD bus expansion I/O is transferred at a rate of up to 1 Mbyte/second for 8-bit data and 1.5 Mbytes/second for 16-bit data. The ZT 8904 supports the STD bus wait request signal, WAITRQ*, to interface to I/O boards with longer access time requirements than those defined by zero wait state STD 32 specifications. The STD bus I/O expansion signal, IOEXP, is also supported. The IOEXP signal is automatically driven low over the I/O address range FC00h to FFFFh. Application software should use this address range to access STD bus I/O boards decoding IOEXP and fewer than 16 bits of address to prevent the board from being redundantly mapped throughout the 64 Kbyte I/O address space. During local I/O operations, the STD bus is held static to decrease system electrical noise and power consumption.

F900h-FFFFh	AVAILABLE
F800h-F8FFh	CPU CONFIGURATION
F500h-F7FFh	AVAILABLE
F4D0h-F4FFh	CPU CONFIGURATION
F4C0h-F4CFh	WATCHDOG
F400h-F4BFh	CPU CONFIGURATION
F100h-F3FFh	AVAILABLE
F000h-F0FFh	CPU CONFIGURATION
0700-EFFFh	AVAILABLE
0600h-06FFh	RESERVED
0400-05FFh	AVAILABLE
03F8h-03FFh	COM1
03F6h-03F7h	IDE
03F0h-03F5h	RESERVED
0300h-03EFh	AVAILABLE
02F8h-02FFh	COM2
02F0h-02F7h	RESERVED
02E8h-02EFh	COM4
02E0h-02E7h	COM3
0280h-02DFh	RESERVED
0278h-027Fh	PRINTER (IEEE 1284)
0270h-0277h	RESERVED
026Eh-026Fh	CPU CONFIGURATION
0200h-026Dh	RESERVED
01F8h-01FFh	AVAILABLE
01F0h-01F7h	IDE
0100h-01EFh	AVAILABLE
00F0h-00FFh	COPROCESSOR
00A2h-00EFh	AVAILABLE
00A0h-00A1h	INTERRUPT #2
0094h-009Fh	AVAILABLE
0092h-0093h	CPU CONFIGURATION
0090h-0091h	AVAILABLE
0080h-008Fh	DMA PAGE REGS
0078h-007Fh	PARALLEL I/O
0070h-0077h	REAL TIME CLOCK
0068h-006Fh	RESERVED
0060h-0067h	KEYBOARD
0044h-005Fh	AVAILABLE
0040h-0043h	COUNTER / TIMERS
0024h-003Fh	AVAILABLE
0022h-0023h	CPU CONFIGURATION
0020h-0021h	INTERRUPT #1
0010h-001Fh	AVAILABLE
0000h-000Fh	DMA

I/O Address Map

CONNECTOR CONFIGURATION

The following figure shows the locations and assignments of connectors J1 - J8. See "Connectors" in Appendix B for information on connector pin assignments and cabling.



Connector Locations

JUMPER DESCRIPTIONS

The ZT 8904 includes several jumper options that tailor the operation of the board to specific application requirements. These options are summarized in Appendix A, "Jumper Configurations."

SETUP

The following topics present a brief introduction to the setup and configuration of the ZT 8904. For documentation specific to the BIOS and other utilities, see the *Ziatech Industrial BIOS manual* (shipped with Ziatech Development Systems).

System Configuration Overview

The Ziatech Industrial BIOS and MS-DOS operating system software is preprogrammed in the ZT 8904's on-board flash memory. The BIOS includes embedded support to allow the ZT 8904 flash memory to be used as a solid-state drive (SSD) in the MS-DOS environment. Ziatech also supplies SSD support for QNX (contact Ziatech for SSD drivers for other operating systems).

The ZT 8904 is configured during the boot sequence by the BIOS. The BIOS uses system configuration information stored as SETUP parameters.

To access the SETUP utility, either boot the system and press the **"S"** key during the system RAM check, or run the SETUP.COM utility from the MS-DOS prompt.

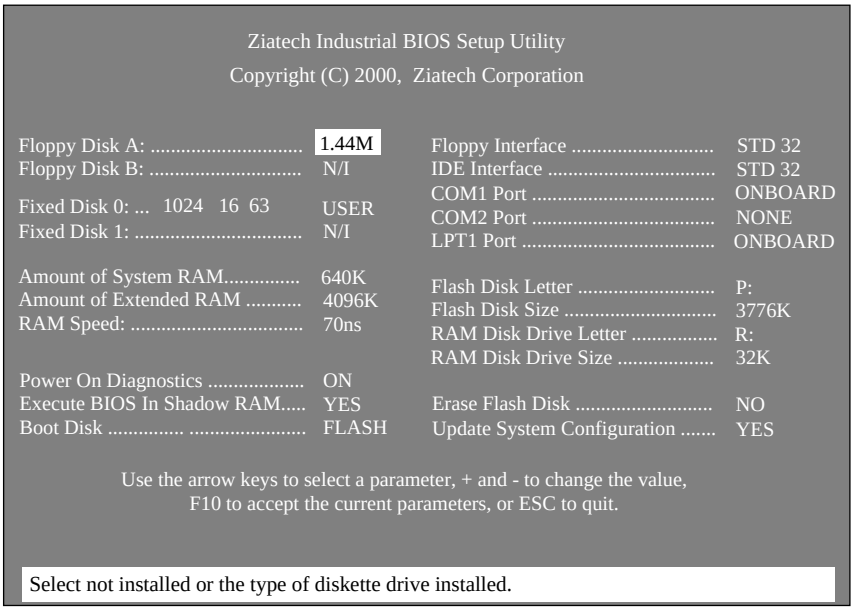
The SETUP parameters are saved in the battery-backed RAM portion of the ZT 8904's real-time clock device. The SETUP parameters can also be saved in a file format, or as the programmed BIOS defaults.

When SETUP is run, an interactive configuration screen is displayed, as shown in the "BIOS SETUP Utility Screen Example" illustration following.

Note: the SETUP program is a generic utility used for all Ziatech processor boards. Some parameters not applicable to the ZT 8904 may be labeled "N/A".

The BIOS SETUP screen is organized as a single screen. The SETUP screen allows the user to select options for such items as base memory and extended memory size selection, boot source, hard disk type, and floppy disk type.

The parameters in the SETUP screen are easily changed. Use the arrow keys to select a parameter, then press + or - to step through the valid choices for that parameter. A dynamic help line at the bottom of the screen helps you determine how to set each parameter. SETUP accepts only valid parameter sets: if changing one parameter invalidates another parameter, SETUP automatically updates the invalid parameter. After setting the parameters, press the F10 key to accept them.



ZT8904

BIOS SETUP Utility Screen Example

3. STD BUS INTERFACE

The ZT 8904 includes several I/O devices common to industrial control applications. The ZT 8904 also operates with the STD 32 bus architectures to support additional I/O and memory mapped devices as required by the application. This section discusses the STD 32 architecture and its effect on the operation of the ZT 8904.

STD 32 OPERATION

The *STD-80 Series Bus Specification*, developed in the early 1980s by Ziatech Corporation, defines the electrical, mechanical, and functional characteristics of an STD bus system based on the 8088 series of microprocessors. Features of an STD-80 system include an 8-bit data bus, 24-bit address bus, and single bus master operation.

In the late 1980s, Ziatech developed the *STD 32 Bus Specification* as an extension to the *STD-80 Bus Specification*. Features of an STD 32 system include compatibility with STD-80 memory and I/O boards, expansion capabilities of up to a 32-bit data bus and a 32-bit address bus, and support for multiple bus master operation.

STD 32 Operation

Data transfers between the ZT 8904 and any STD bus memory or I/O board occur eight bits at a time for boards supporting an 8-bit data bus and 16 bits at a time for boards supporting a 16-bit data bus in an STD 32 system. The ZT 8904 automatically determines the type of transfer at the start of each STD bus operation.

If the application software includes a 16-bit operation with an 8-bit STD bus board, the ZT 8904 automatically reduces the transfer into two STD bus cycles. If the application software includes a 16-bit operation with a 16-bit STD bus board, the ZT 8904 performs the transfer in a single STD bus cycle.

In addition to 16-bit data transfer support, the STD 32 system has another advantage: it supports up to seven ZT 8904 boards in a single system. With the addition of an STD bus arbiter, such as the ZT 89CT39, multiple ZT 8904 boards have fixed or rotating priority access to STD bus memory and I/O resources. This architecture is useful for applications that can be divided into modular control blocks, with each module running on a unique ZT 8904. The ZT 8903 does not support multiple master operation.

STD 32 BUS COMPATIBILITY

The ZT 8904 is compatible with Revision 1.2 of the *STD 32 Bus Specification* (Ziatech part number ZT MSTD32). Optional STD 32 features are discussed in terms of compliance levels.

- Permanent Master: SA16, SA8 - I, SDMABP, {MD}
- Temporary Master: SA16, SA8 - I, SDMABP, {MD}

Compliance Levels

The following is a brief description of the STD 32 compliance levels supported by the ZT 8904.

SA16, SA8 Supports 8-bit and 16-bit data transfers with STD-80 signal format and timings. The ZT 8904 automatically determines the width of the data transfer at the start of each STD bus operation. STD-80 compatible memory and I/O boards are supported.

I Supports four additional STD bus interrupts: INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. These interrupts are input from the STD bus and connected to the interrupt controller through a jumper configuration block for increased flexibility.

SDMABP Supports Standard Architecture DMA using BUSRQ*/BUSAK* for request and acknowledge and the backplane DMA control signals DMAIOR*, DMAIOW*, and T-C. It is not permissible to program the DMA controller for cascaded operation.

{MD} Supports the multiple master (DREQx*, DAKx*) protocol. These two signals are used by the ZT 8904 in a multiple master architecture to gain control of STD bus resources. The use of these signals requires a bus arbiter, such as the ZT 89CT39, to be plugged into Sot X.

STD BUS INTERRUPTS

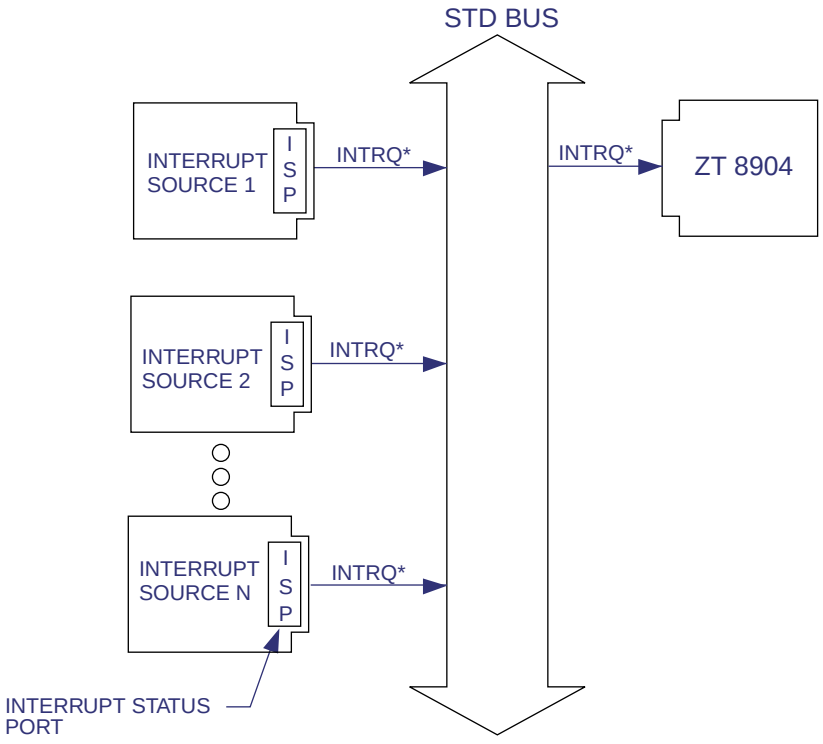
The ZT 8904 supports both maskable and non-maskable interrupts from the STD bus. This section discusses system level issues related to these interrupts. Refer to Chapter 4, "Interrupt Controller," for more information on the maskable interrupt controllers.

Maskable Interrupts

The STD bus maskable interrupts monitored by the ZT 8904 are INTRQ* (P44), INTRQ1* (P37), INTRQ2* (P50), INTRQ3* (E67), and INTRQ4* (P5). These maskable interrupts are routed to a jumper configuration block (W17-22) for added flexibility. Note that an STD 32 backplane is needed to use INTRQ3*.

The ZT 8904 is also capable of generating STD bus interrupts. This feature is useful in multiple master systems to coordinate communications between processors.

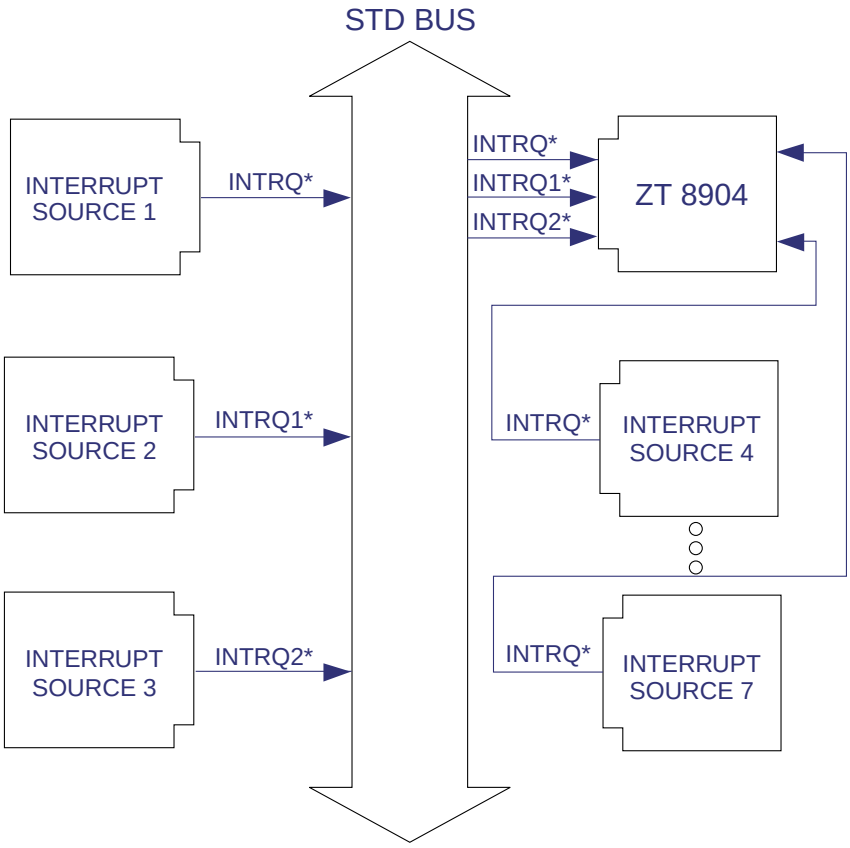
Some applications may find it necessary to share multiple interrupt sources on a single STD bus interrupt request, as shown in the "STD Bus Polled Interrupt Structure" figure following. Since the interrupt controller provides a single vector for each input, it is up to the application software to poll each possible source on the shared interrupt request signal to determine which is requesting service. This procedure is fine for most applications, provided that each source can be polled and that the interrupt controller is programmed for level-triggered operation.



STD Bus Polled Interrupt Structure

Some applications include edge-triggered interrupt sources. For example, the Ziatech Industrial BIOS uses edge-triggered interrupts to support the timer used to generate the periodic system tick. Since the interrupt controller inputs are not independently programmable for edge-triggered or level-triggered interrupts, all inputs for these applications must be treated as edge-triggered.

In an edge-triggered architecture, multiple interrupt sources should not share the same interrupt request signal because it is possible to miss an interrupt request from one source while an interrupt request from another source is being serviced. For this architecture, each interrupt source requires a unique connection to the interrupt controller, as shown in the "STD Bus Vectored Interrupt Structure" figure following.



STD Bus Vectored Interrupt Structure

Non-Maskable Interrupts

The ZT 8904 supports three sources of non-maskable interrupt requests. Each interrupt source must be jumper enabled as described in the W9-11 jumper description in Appendix A, "Jumper Configurations."

- STD bus NMIRQ* (P46)
- AC power-fail detection
- Watchdog timer stage one

RESET

The ZT 8904 is automatically reset with a precision voltage monitoring circuit that detects when Vcc is below the acceptable operating limit of 4.75 V. Other sources of reset include watchdog timer stage 2, local pushbutton switch, and the STD bus pushbutton reset signal, PBRESET* (P48).

The ZT 8904 responds to any of these reset sources by initializing local peripherals and driving the STD bus system reset, SYSRESET* (P47). The ZT 8904 reset is typically active for 350 milliseconds.

MULTIPLE MASTER AND INTELLIGENT I/O

Ziatech offers the following two architectures for increasing the number of microprocessors in a single system:

- Multiple master
- Intelligent I/O

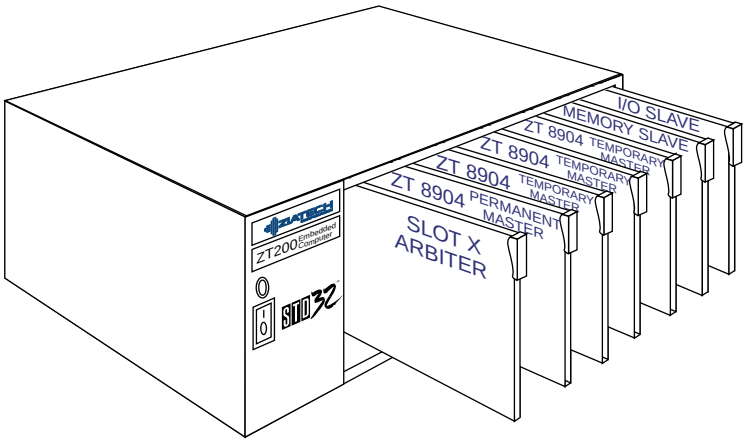
Applications can use multiple master, intelligent I/O, or a combination of the two.

Multiple Master

A multiple master architecture requires one permanent master and one or more temporary masters, as illustrated in the "Multiple Master Architecture" figure following. The ZT 8904 is configured for permanent or temporary master operation through the installation and removal of resistor packs RP16 and RP17. With both resistor packs installed, the ZT 8904 functions as a permanent master. With both resistor packs removed, the ZT 8904 functions as a temporary master. The ZT 8903 does not support multiple master operation.

In a multiple master architecture, each master has complete access to STD bus resources and operates at full speed when the local CPU is communicating with local memory and I/O. It is not until the application software attempts an STD bus access that arbitration occurs.

The ZT 8904 responds to an STD bus access from the application software by generating an STD bus request, DREQx* (E16), to an external bus arbiter such as the ZT 89CT39. The ZT 8904 then suspends all local operation until the bus arbiter returns an STD bus acknowledge, DAKx* (E15). All arbitration is done in hardware on the external bus arbiter board and is transparent to the application software. The amount of time required for this arbitration depends on the amount of time higher priority masters are in control of STD bus resources. A shared resource locking mechanism is supported to guarantee exclusive access to STD bus memory or I/O.



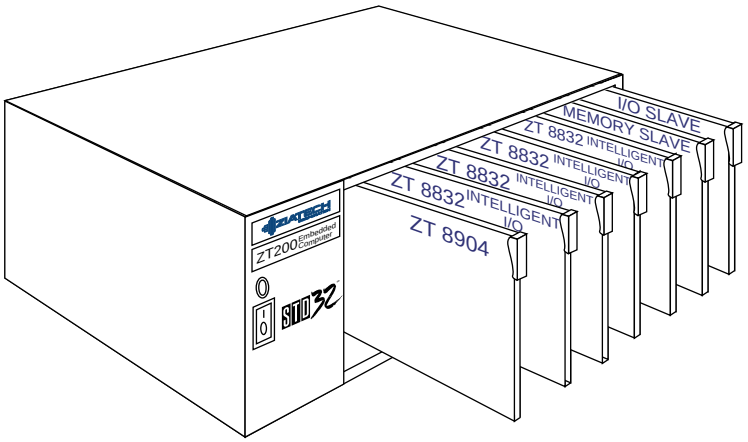
Multiple Master Architecture

Intelligent I/O

An intelligent I/O system includes a single ZT 8904 and one or more intelligent I/O boards, such as the ZT 8832. This architecture is illustrated in the following figure "Intelligent I/O Architecture." The intelligent I/O board incorporates several I/O devices, a dual-port RAM for processor communications, and a CPU dedicated to controlling these devices.

Each intelligent I/O board operates at full speed when communicating with local memory, local I/O, and dual-port RAM. The ZT 8904 also operates at full STD bus speeds when accessing the dual-port RAM. It is not until the ZT 8904 and the intelligent I/O board access the dual-port RAM at the same time that arbitration occurs.

All arbitration is done in hardware local to each intelligent I/O board, eliminating the need for an external bus arbiter. The arbitration is transparent to the application software. The amount of time required for arbitration depends on the amount of time the device in control of the dual-port RAM requires to complete operation. A shared resource locking mechanism is supported to guarantee exclusive access to dual-port RAM by either the ZT 8904 or the intelligent I/O board.



Intelligent I/O Architecture

Multiple Master Vs. Intelligent I/O

Both multiple master and intelligent I/O architectures are excellent methods of increasing system performance. The application designer has the freedom to select either architecture or combine both to meet the needs of the specific application. The following is a brief comparison of the multiple master and intelligent I/O architectures.

- An advantage of the multiple master system is that each ZT 8904 has complete access to all STD bus memory and I/O resources. However, in an intelligent I/O system, only one ZT 8904 has access to STD bus memory and I/O, including the dual-port RAM interface to each intelligent I/O board.
- An advantage of the intelligent I/O system is lower system cost. The intelligent I/O architecture operates in STD 32 bus structures. Dual port RAM arbitration is local to each intelligent I/O board, eliminating the need for a system arbiter. Also, most multiple master implementations require an STD bus memory slave for communications between the masters. With an intelligent I/O architecture, all communications between the single master and the intelligent I/O boards are through the dual-port RAM local to each intelligent I/O board.

System Requirements

The following is a list of considerations for the ZT 8904 operating in a multiple master architecture.

- One ZT 8904 must be configured as a permanent master, or there must be another board in the system responsible for managing the STD bus clock, CLOCK* (P49), and the system reset, SYSRESET (P47). The remaining ZT 8904 boards must be configured for temporary master operation: the two socketed resistor packs, RP16 and RP17, must be installed on the permanent master and removed from all temporary masters. These resistor packs are located next to the STD 32 connector.

- An STD 32 backplane is required. The STD-80 backplane does not support the bus exchange protocol (DREQx* and DAKx*).
- A ZT 89CT39, or equivalent bus arbiter, is needed to manage ZT 8904 access to the STD bus resources. The arbitration may also be built directly on to the permanent master if a ZT 8904 is not used for this function.

Multiple Master Reset

The ZT 8904, configured for single master operation, is automatically reset with a precision voltage monitoring circuit, watchdog timer, local pushbutton reset, and the STD bus pushbutton reset signal, PBRESET* (P48). In response to any of these signals, the ZT 8904 initializes local peripherals and activates the STD bus system reset, SYSRESET* (P47).

In a multiple master system, a ZT 8904 configured as a permanent master operates the same as a ZT 8904 operating in a single master architecture. A ZT 8904 configured as a temporary master manages reset differently. A temporary master does not monitor PBRESET* and does not generate SYSRESET*. Instead, a temporary master ignores PBRESET* and monitors SYSRESET*. This enables the temporary masters to be reset when the permanent master generates SYSRESET*. This also enables the pushbutton reset on the temporary master to reset only the temporary master while the pushbutton on the permanent master resets the entire system.

4. INTERRUPT CONTROLLER

The ZT 8904 includes two Intel-compatible 8259 cascaded interrupt controllers that provide a programmable interface between interrupt-generating peripherals and the CPU. The interrupt controllers monitor 15 interrupts with programmable priority. When peripherals request service, the interrupt controller interrupts the CPU with a pointer to a service routine for the highest priority device. The major features of the interrupt architecture are listed below. The ZT 8904 does not support cascaded interrupt controllers on the STD bus.

- 15 individually maskable interrupts
- Level-triggered or edge-triggered recognition
- Fixed or rotating priorities

The interrupt architecture is illustrated in the "Interrupt Architecture" figure following. Interrupt configuration jumpers (W17-22) are used to customize the interrupt architecture to the needs of the application. These jumpers connect one of two interrupt sources to an interrupt input. Wire-wrap techniques provide additional flexibility.

The interrupt sources are summarized below.

Backplane: Five STD bus interrupts are routed to the interrupt configuration jumpers. These interrupts are INTRQ*, INTRQ1*, INTRQ2*, INTRQ3*, and INTRQ4*. All five interrupts are supported in an STD 32 backplane. These interrupts are active-low on the STD bus and inverted before they reach the interrupt configuration jumpers.

Frontplane: Three frontplane interrupts are routed to the configuration jumpers. These interrupts are available through connector J2 as active-low inputs that are inverted before reaching the interrupt configuration jumpers. The pin assignments for connector J2 are given in Appendix B, "Specifications." Many STD bus boards include a J2-compatible connector for routing interrupts to the ZT 8904 through a ribbon cable. This architecture is useful if the application requires more interrupts than are available on the STD bus.

Local: Local interrupt sources include the keyboard controller, serial ports (COM1, COM2, COM3, and COM4), multiprocessor communications, 1284 parallel port, event sense parallel I/O, real-time clock, timer/counters, DMA controller, Math coprocessor, watchdog timer, and optional IDE controller.

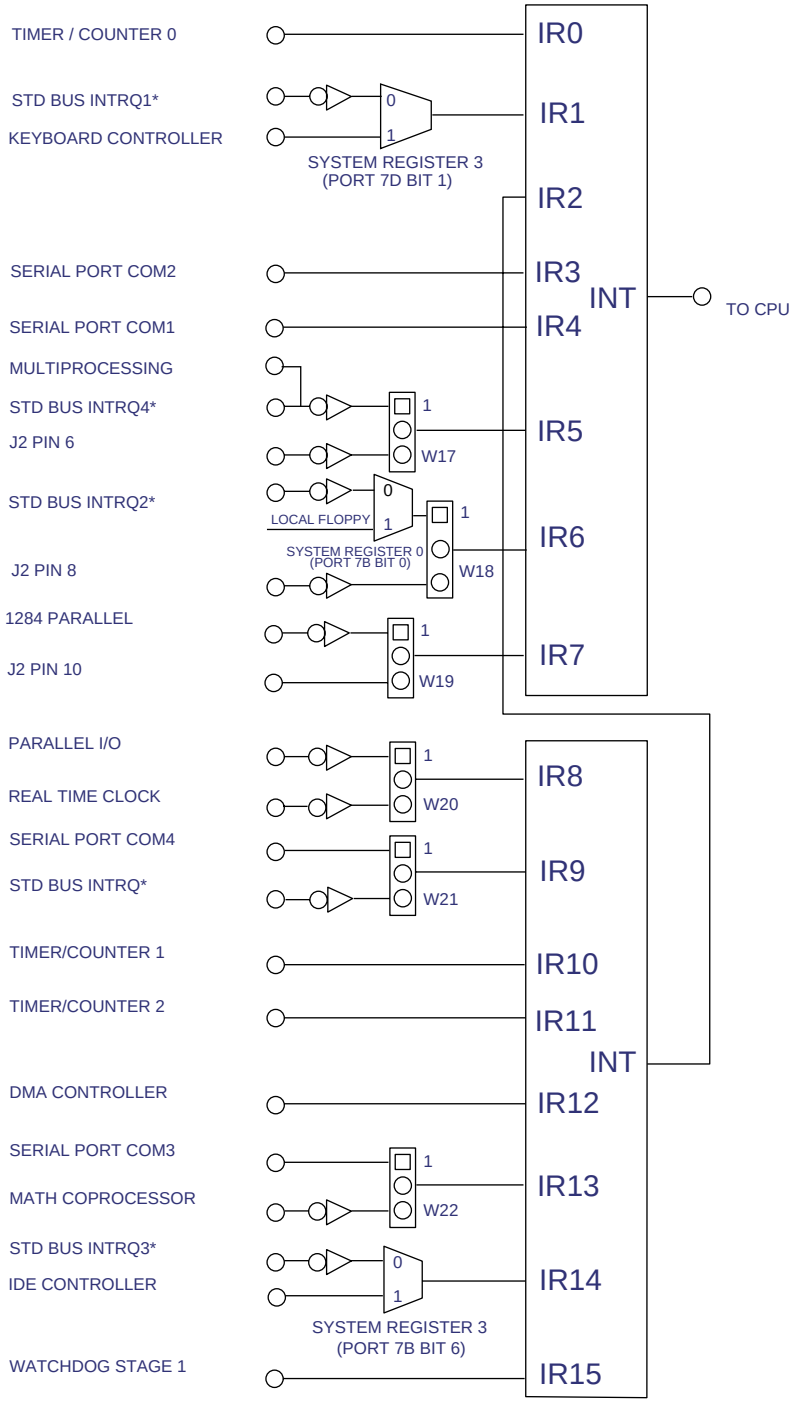
PROGRAMMABLE REGISTERS

Each interrupt controller includes four initialization registers, three control registers, and three status registers. The I/O port addressing for the interrupt controllers is given in the

following table. The base address of the master interrupt controller is 20h and the base address of the slave interrupt controller is A0h.

Interrupt Controller Register Addressing

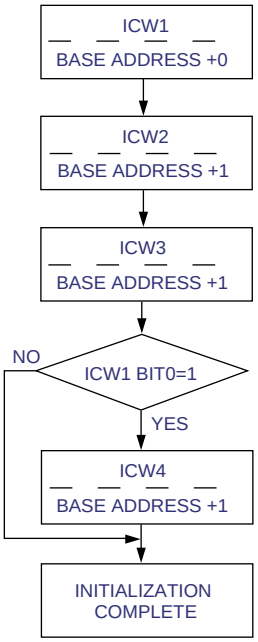
Address	Register	Operation
Base+0h	IRR, ISR, IPR	Read
Base+0h	ICW1	Write
Base+0h	OCW2, OCW3	Write
Base+1h	OCW1	Read/Write
Base+1h	ICW2, ICW3, ICW4	Write



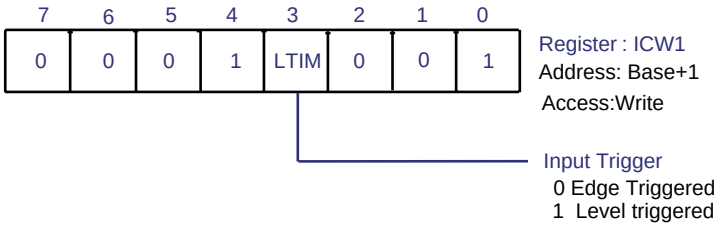
Interrupt Architecture

Interrupt Architecture Initialization Registers (ICW1-ICW4)

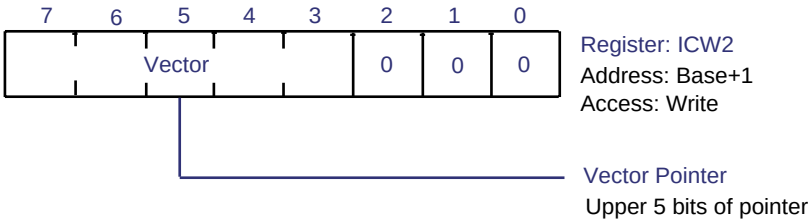
Each interrupt controller must be initialized before it is used. Initialization consists of writing two, three, or four initialization commands. The programming sequence for these registers is given in the "Interrupt Initialization Programming" figure below. ICW1, ICW2, and ICW3 must be programmed during each initialization sequence. ICW4 may or may not be programmed, as required by the application.



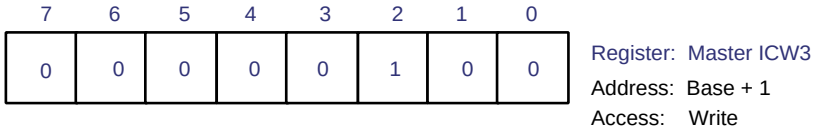
Interrupt Initialization Programming



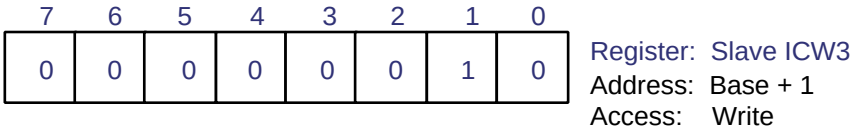
Initialization Register ICW1



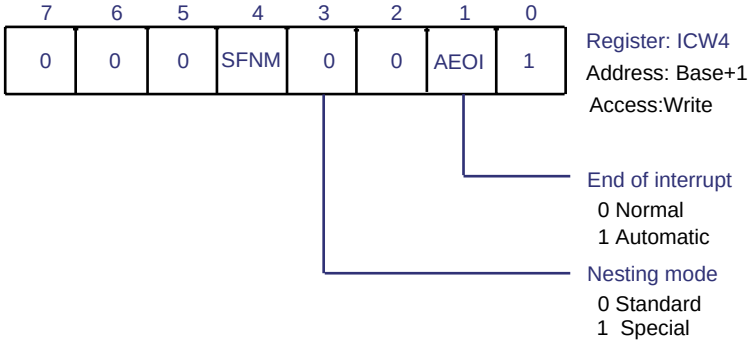
Initialization Register ICW2



Master Initialization Register ICW3



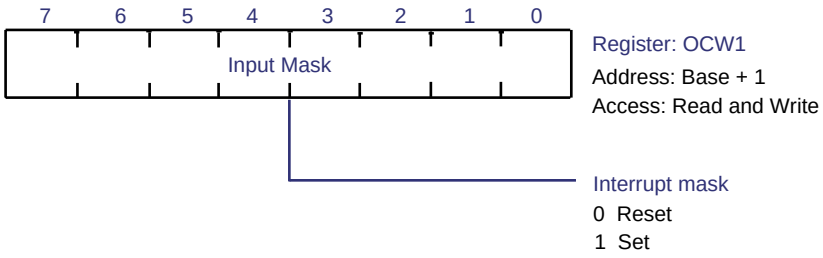
Slave Initialization Register ICW3



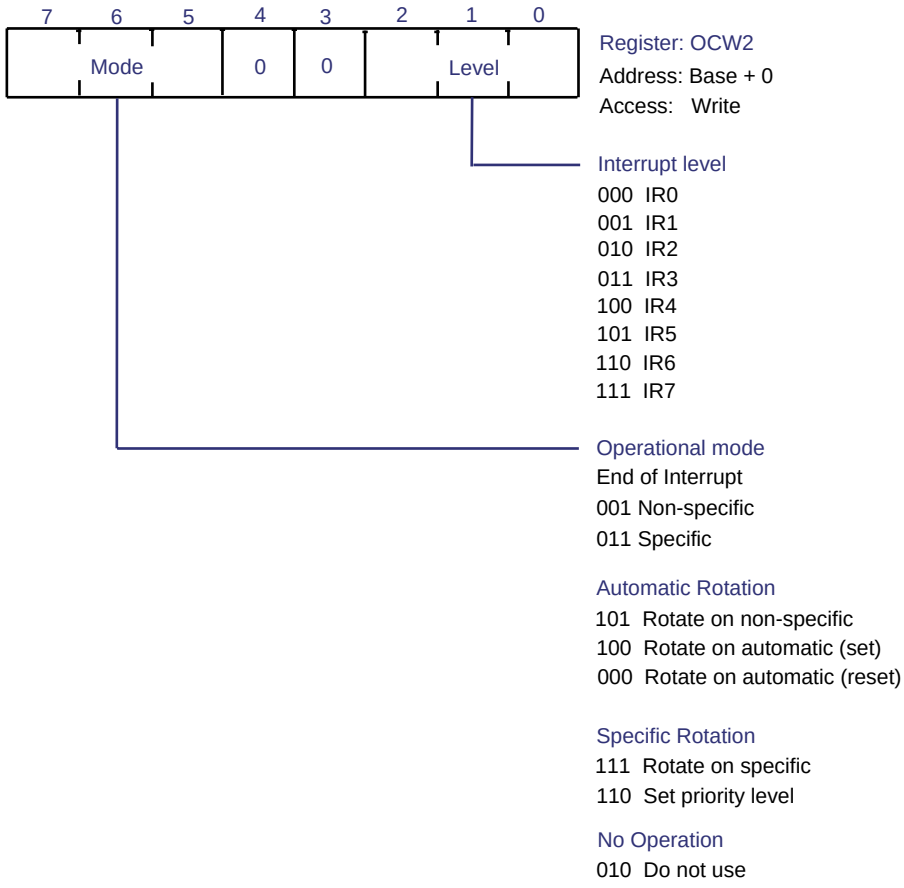
Initialization Register ICW4

Operational Registers (OCW1-OCW3)

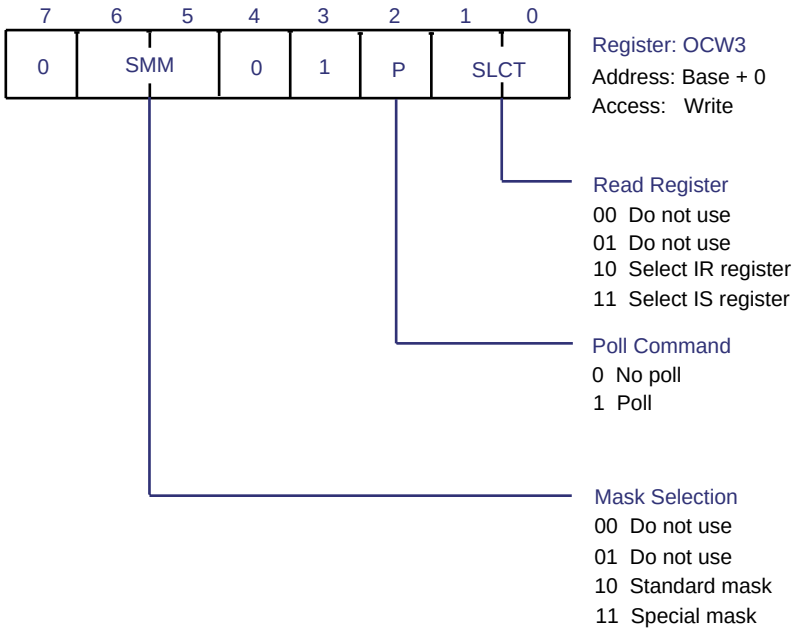
The operation of each interrupt controller is managed by three 8-bit operational registers. These registers are programmed in any sequence for things such as enabling and disabling interrupt requests and changing interrupt priorities.



Operational Register OCW1



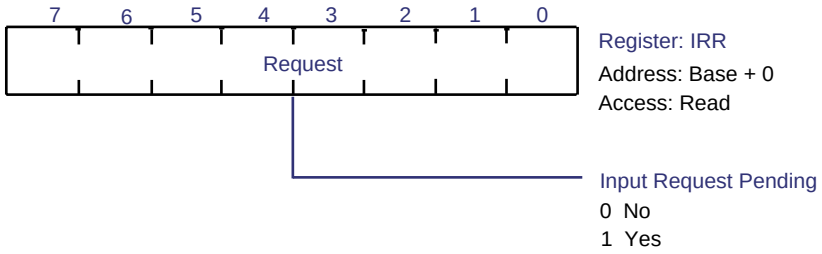
Operational Register OCW2



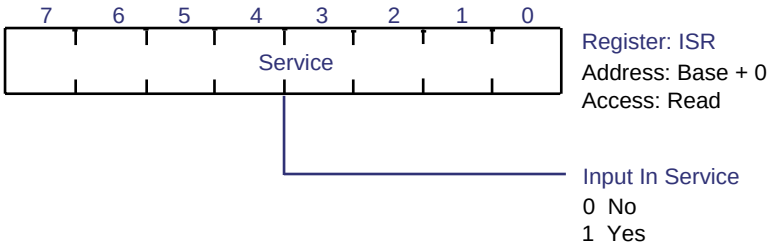
Operational Register OCW3

Status Registers (IRR, ISR, IPR)

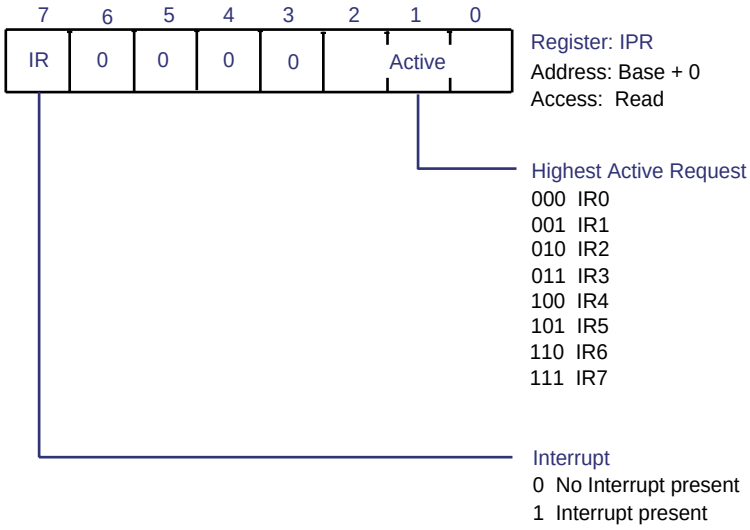
Each interrupt controller includes three status registers. A status register is selected by programming the first three bits of OCW3.



Status Register IRR



Status Register ISR



Status Register IPR

ADDITIONAL INFORMATION

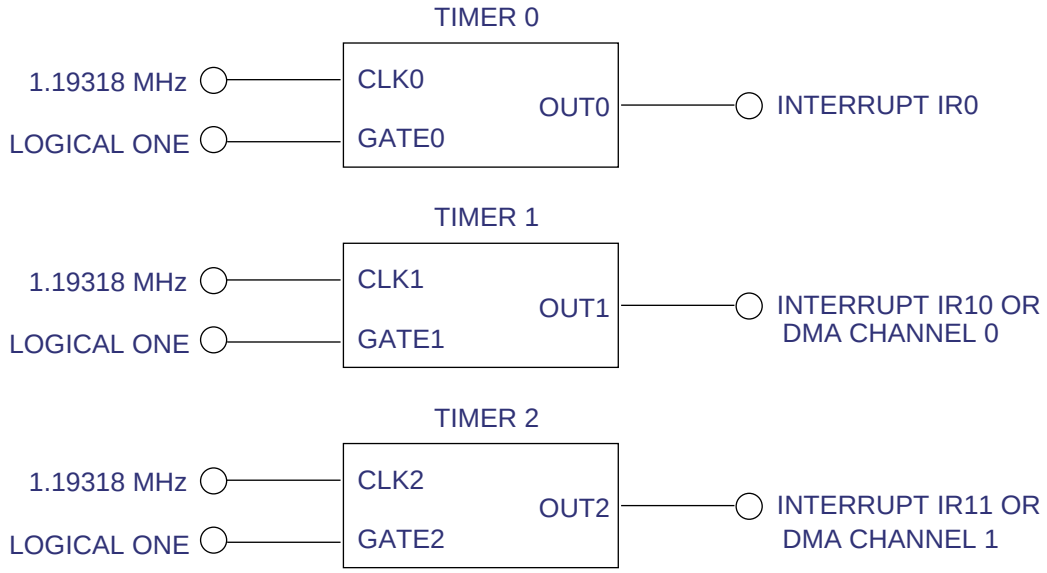
Refer to the *Ziatech Industrial Computer System Manual* for more information on the operating system's use of the interrupt inputs. Refer to the Intel 386 EX data book for more information on the interrupt controller operating modes.

5. COUNTER/TIMERS

The ZT 8904 includes one Intel-compatible 8254 device with a total of three programmable counter/timers. The counter/timers are useful for software timing loops, timed interrupts, and periodic interrupts. The major features of the counter/timers are listed below.

- Three 16-bit counter/timers
- Six programmable operating modes
- Binary and BCD counting
- Interrupt and polled operation

The counter/timer architecture is illustrated in the "Counter/Timer Architecture" figure below. In some cases, not all counter/timers are available for application development. In an MS DOS system, for example, counter/timer 0 generates a periodic system interrupt and should not be programmed by the application. Please refer to the selected operating system manual for more information.



Counter/Timer Architecture

The six programmable operating modes are summarized in the "Counter/Timer Operating Modes" table following.

Counter/Timer Operating Modes

Mode	Counter/Timer Output Operation
0	Transitions after programmed count expires
	Gate tied high to enable counting
1	Transitions after programmed count expires
	Gate tied high to enable counting
2	Periodic single pulse after programmed count expires
	Gate tied high to enable counting
3	Square wave with frequency equal to programmed count
	Gate tied high to enable counting
4	Single pulse after programmed count expires
	Gate tied high to enable counting
5	Single pulse after programmed count expires
	Gate tied high to enable counting

PROGRAMMABLE REGISTERS

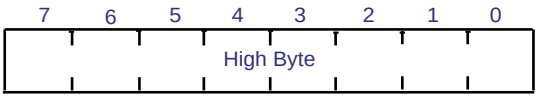
The counter/timers are accessed through four I/O addresses as shown in the following table. Each counter/timer occupies an I/O port address through which the preset count values are written and both the count and status information is read. The Control register occupies the remaining I/O port address, which services all three counter/timers.

Counter/Timer Register Addressing

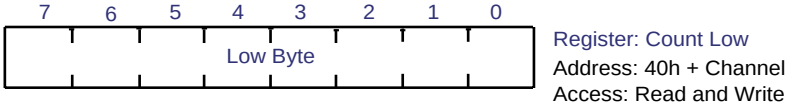
Address	Register	Operation
0040h	Channel 0 Count	Read/Write
0040h	Channel 0 Status	Read
0041h	Channel 1 Count	Read/Write
0041h	Channel 1 Status	Read
0042h	Channel 2 Count	Read/Write
0042h	Channel 2 Status	Read
0043h	Control	Write

Count Registers and Count Latch

Each counter/timer has a 16-bit Count register and count latch. Data is transferred to the counter/timers through the Count register and from the counter/timers through the count latch. The Control register defines the method for accessing the 16-bit Count register through an 8-bit I/O port.



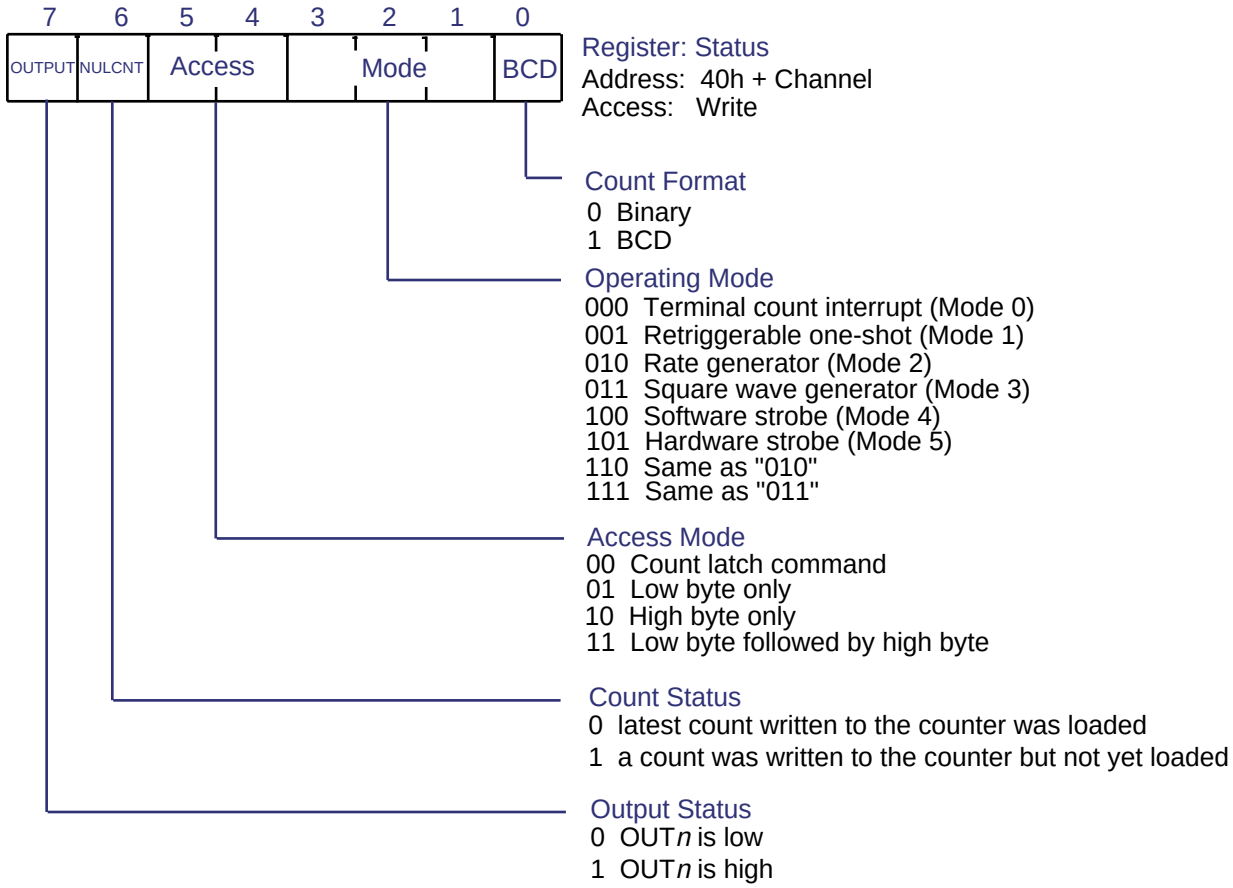
Count Register High Byte



Count Register Low Byte

Status Register

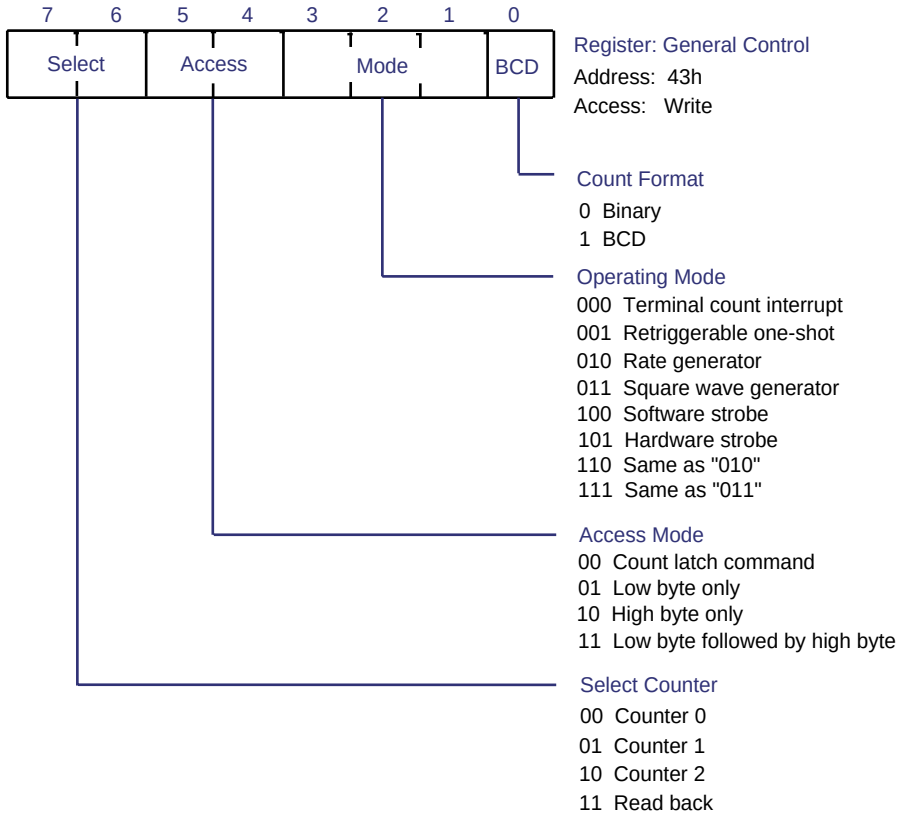
Each counter/timer has a Status register. The Status register must be read using the multiple latch command specified in the Control register.



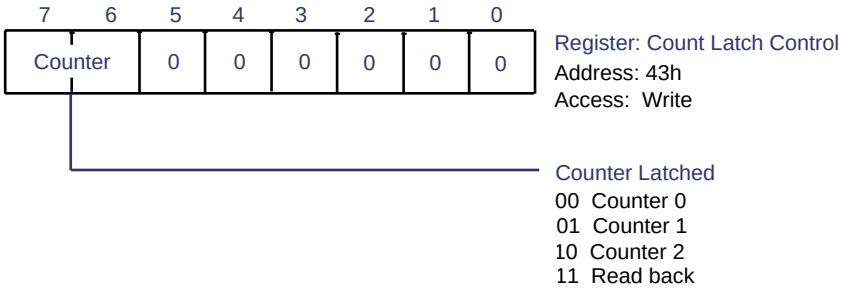
Status Register

Control Register

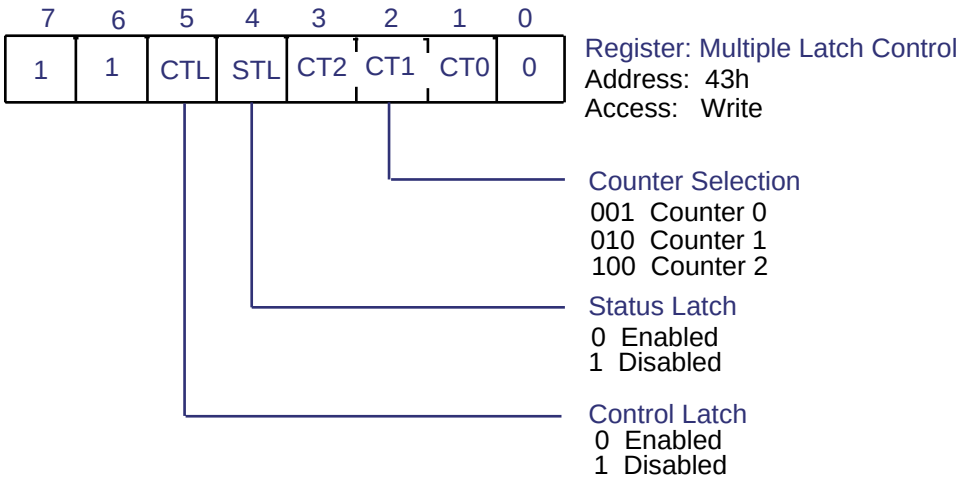
The Control register is used to initialize the counter/timers and to select the method of reading the count and status information. The Control register is best described by dividing it into three formats as illustrated below.



General Control Register



Count Latch Control Register



Multiple Latch Control Register

ADDITIONAL INFORMATION

Refer to the *Ziatech Industrial Computer System Manual* for more information on the operating system's use of the counter/timers. Refer to the Intel 386 EX data book for more information on the counter/timer operating modes.

6. DMA CONTROLLER

The DMA controller used on the ZT 8904 is contained within the 386 EX microprocessor. It improves system operation by allowing external or internal peripherals to directly transfer data to or from ZT 8904 memory. The DMA controller can transfer data between memory and I/O with 8-bit or 16-bit data path widths. It has features that are not available on an 8237A, and it can be configured to operate in an 8237A-compatible mode.

The DMA controller contains two identical, independently configurable channels. One of the following peripherals can request DMA service:

- A 386 EX external peripheral (connected to the DRQ0 or DRQ1 pins)
- A 386 EX internal peripheral (asynchronous serial I/O, synchronous serial I/O, or counter/timer unit)

The DMA configuration register (DMACFG) is used to select one of the possible sources. In addition to these hardware request sources, each channel contains a software request register that can be used to initiate transfers. Both channels share a common end-of-process signal. The major features of the DMA architecture are listed below.

- One STD bus/local DMA channel (Channel 0)
- One local DMA channel (Channel 1)
- STD bus DMA slave support
- Buffer transfer processes:
  - Single buffers
  - Autoinitialized buffers
  - Chained buffers
- Buffer transfer modes supported:
  - Single mode
  - Block mode
  - Demand mode
- DMA transfers over the full local memory range

INTEL 386 EX INTERNAL ARCHITECTURE

The 386 EX DMA controller internal architecture is illustrated in the "386 EX Internal DMA Controller Connections" figure following. This figure details all of the DRQ source

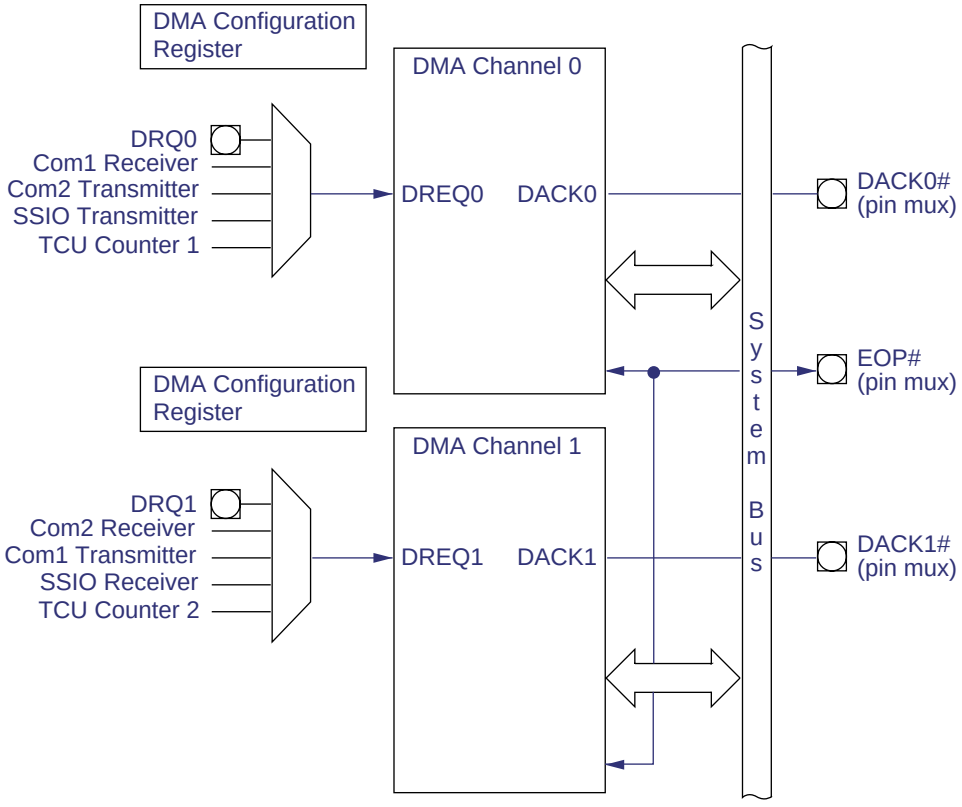
connections internal to the 386 EX. Note that the synchronous serial channel is not implemented on the ZT 8904 in favor of providing an additional asynchronous serial channel.

Channel 0 supports the following devices as DRQ sources (DMACFG.6-4).

- External DMA slave request
- COM1 receive buffer full
- COM2 transmit buffer empty
- Timer/Counter unit 1 OUT1

Channel 1 supports the following devices as DRQ sources (DMACFG.2-0).

- Local floppy disk (PC87303 internal floppy controller)
- Local IEEE-1284 (PC87303 internal parallel port)
- COM2 receive buffer full
- COM1 transmit buffer empty
- Counter/Timer unit 2 OUT2



386 EX Internal DMA Controller Connections

DMA IMPLEMENTATION

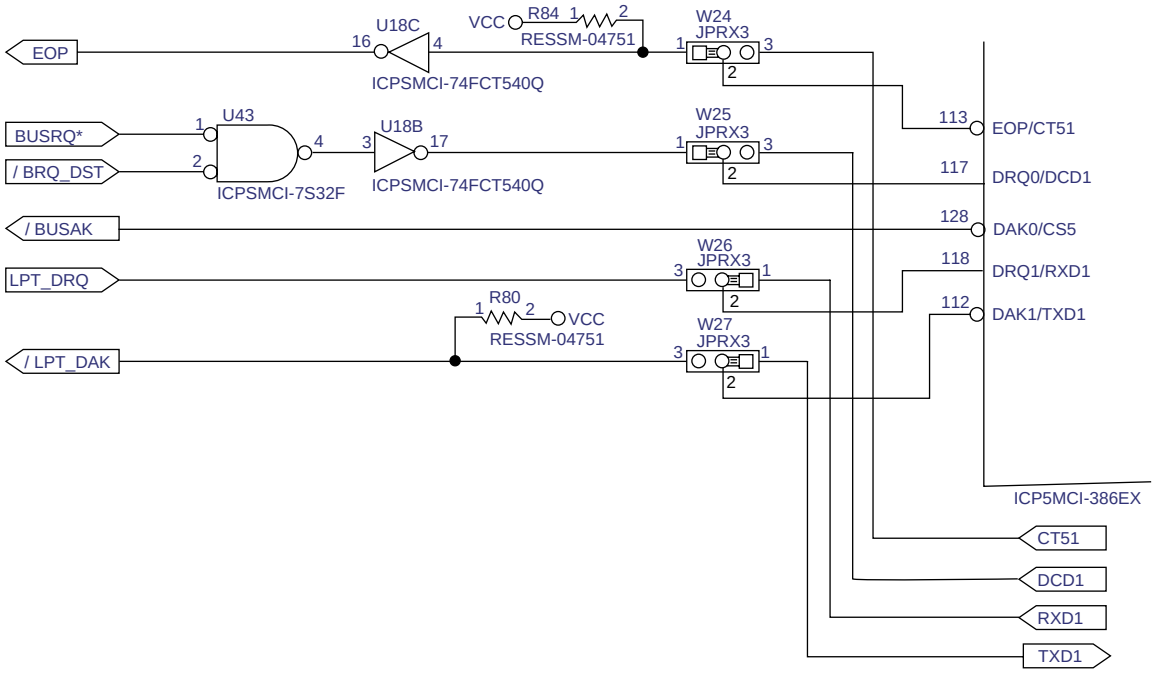
The ZT 8904 DMA architecture external to the 386 EX is illustrated in the following figure, "DMA Architecture." The ZT 8904 supports a single DMA channel for STD bus DMA slaves. STD bus DMA slaves are I/O devices that use the ZT 8904 DMA channel 0 to transfer data between backplane I/O and ZT 8904 local memory. The ZT 8904 supports the use of both DMA channels for specific 386 EX internal peripherals.

The two DMA channels supported by the ZT 8904 are implemented in the 386 EX by multiplexing multiple functions onto device pins. This causes mutual exclusion in the use of certain hardware functions. Pins with shared functions are shown in the following figure, "DMA Architecture." Note that DRQ1 and /DAK1 are shared with RXD1 and TXD1.

These shared functions prevent using COM 2 while DMA channel 1 is used. If DMA channel 0 is used but DMA channel 1 is not, COM 2 can be used, but only as a 3-wire interface (useful if the serial channel is capable of in-band flow control). Conversely, if COM 2 is used with hardware handshaking, neither DMA channel can be used.

The Ziatech industrial BIOS setup utility supports configuration of the ZT 8904 for either DMA support (floppy) or for COM 2 support. When the ZT 8904 is configured for COM2 with hardware handshake, the BIOS setup option for COM2 must be set as "ONBOARD." Note that although the 386 EX supports use of /EOP as an input, the ZT 8904 implementation does not support buffer termination on assertion of /EOP.

Specific jumper selections (W24-27) are required in order to properly configure the ZT 8904 to support DMA channel 0 or channel 1. These jumper selections are listed in Appendix A, "Jumper Configurations."



DMA Architecture

DMA TRANSFER CYCLES

The ZT 8904 supports DMA channel 0 as a channel for backplane DMA slaves. Channel 0 must be programmed using two-cycle bus transfers. This causes at least two separate bus cycles to occur for each DMA data transfer. DMA channel 1 is supported for local devices. Channel 1 can be programmed using either fly-by or two-cycle transfers.

I/O MAPPING

The 386 EX maps the DMA controller into the standard PC-AT I/O locations for DMA channel 0 and channel 1. The "386 EX DMA Controller Registers" table lists I/O addresses of the DMA controller registers. The Ziatech STD-DOS BIOS provides support for the Ziatech ZT 8954 floppy subsystem. All application software must either communicate with the floppy subsystem through the system BIOS or be coded to access the correct addresses in the DMA controller I/O map.

DMA CONTROLLER OPERATION

The 386 EX DMA controller transfers data between a requester and a target. The data can be transferred either from a requester to a target or from a target to a requester. The target and requester can be located in either memory or I/O space, and transfers can be on either a byte or a word basis. The requester can be an external device (located in external I/O) an internal peripheral (located in internal I/O), or memory.

An external device or an internal peripheral requests service by activating a channel's request input (DRQn). A requester in memory requests service through the DMA software request register. The requester either transfers data to or retrieves data from the target.

Programming a DMA Channel

A channel is programmed by writing to a set of registers including requester address, target address, byte count, and control registers. The address registers specify base addresses for the target and requester. The byte count registers specify the number of bytes that need to be transferred to or from the target.

Typically, a channel is programmed to transfer a block of data. Therefore, it is necessary to distinguish between the process of transferring one byte or word of data (data transfer) and the process of transferring an entire block of data (buffer transfer).

The byte count determines the number of data transfers that make up a buffer transfer. After each data transfer within a buffer transfer, the byte count is decremented by 1 and the requester and target addresses are either incremented, decremented, or left unchanged. When the byte count expires (reaches -1) the transfer is complete and the number of bytes transferred is the original byte count +1.

Fly-By and Two-Cycle Bus Cycles

There are two bus cycle options for data transfers, fly-by and two-cycle. Fly-by allows data transfers to occur in one bus cycle. However, it requires that the requester be in I/O external to the 386 EX and the target be in memory. The two-cycle option allows data to be transferred between any combination of memory and I/O through the use of a 4-byte temporary buffer.

The fly-by option performs either a memory write or a memory bus cycle. A write cycle transfers data from the requester to the target (memory), and a read cycle transfers data from the target (memory) to the requester. The requester should monitor the bus cycle signals to determine when to access the data bus.

The two-cycle option first fills the four-byte temporary buffer with data from the source, then writes that data to the destination. This method allows transfers between any combination of memory and I/O with any combination of data path widths (8- or 16-bit). The amount of data and the data bus widths determine the number of bus cycles required to transfer the data. For example, it takes six bus cycles to transfer four pieces of data from an 8-bit source to a 16-bit destination: four read cycles to fill the temporary buffer from the 8-bit source, and two write cycles to transfer the data to the 16-bit destination. The programmable DMA transfer direction determines whether the requester or the target is the source or destination.

386 EX DMA CONTROLLER REGISTERS

The "386 EX DMA Controller Registers" table below lists the registers associated with the DMA controller.

The following sections provide bit-level definitions for all registers associated with the DMA controller. Bit definitions in this section assume intended use of one or more DMA channels. Note that the reset state, if defined, is the hardware reset state.

The reset state bit definitions include:

0 is a bit that is set to a logical 0 by a hardware reset.

1 is a bit that is set to a logical 1 by a hardware reset.

--- is a bit that is reserved, write a '0' to these bits.

ND is a bit whose reset state is not defined after a hardware reset.

Any bit described as 'Reserved' should be written with a 0 (unless otherwise indicated.)

386 EX DMA Controller Registers

Register	Address	Expanded Address	PC/AT Description
PINCFG	0F826h	---	Pin mux configuration
DMACFG	0F830h	---	Peripheral connections and mask
DMA0REQ0	0F010h	---	Channel 0 requestor address 0-7
DMA0REQ1	0F010h	---	Channel 0 requestor address 8-15
DMA0REQ2	0F011h	---	Channel 0 requestor address 16-23
DMA0REQ3	0F011h	---	Channel 0 requestor address 24-25
DMA1REQ0	0F012h	---	Channel 1 requestor address 0-7
DMA1REQ1	0F012h	---	Channel 1 requestor address 8-15
DMA1REQ2	0F013h	---	Channel 1 requestor address 16-23
DMA1REQ3	0F013h	---	Channel 1 requestor address 24-25

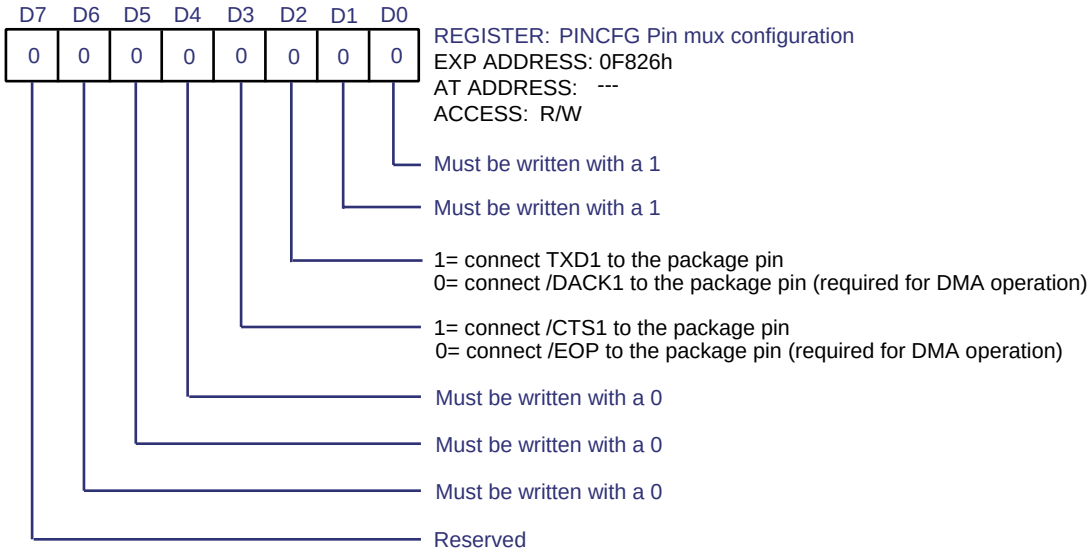
386 EX DMA Controller Registers table (continued)

DMA0TAR0	0F000h	0000h	Channel 0 target address 0-7
DMA0TAR1	0F000h	0000h	Channel 0 target address 8-15
DMA0TAR2	0F087h	0087h	Channel 0 target address 16-23

DMA0TAR3	0F086h	---	Channel 0 target address 24-25
DMA1TAR0	0F002h	0002h	Channel 1 target address 0-7
DMA1TAR1	0F002h	0002h	Channel 1 target address 8-15
DMA1TAR2	0F083h	0083h	Channel 1 target address 16-23
DMA1TAR3	0F085h	---	Channel 1 target address 24-25
DMA0BYC0	0F001h	0001h	Channel 0 byte count 0-7
DMA0BYC1	0F001h	0001h	Channel 0 byte count 8-15
DMA0BYC2	0F098h	---	Channel 0 byte count 16-23
DMA1BYC0	0F003h	0003h	Channel 1 byte count 0-7
DMA1BYC1	0F003h	0003h	Channel 1 byte count 8-15
DMA1BYC2	0F099h	---	Channel 1 byte count 16-23
DMASTS	0F008h	0008h	DMA status register
DMACMD1	0F008h	0008h	DMA command register 1
DMACMD2	0F01Ah	---	DMA command register 2
DMAMOD1	0F00Bh	000Bh	DMA mode register 1
DMAMOD2	0F01Bh	---	DMA mode register 2
DMASRR	0F009h	0009h	DMA software request register
DMAMSK	0F00Ah	000Ah	DMA single channel mask register
DMAGRPMSK	0F00Fh	000Fh	DMA group channel mask
DMABSR	0F018h	---	DMA bus size register
DMACHR	0F019h	---	DMA chaining register
DMAIEN	0F01Ch	---	DMA interrupt enable register
DMAIS	0F019h	---	DMA interrupt status register
DMAOVFE	0F01Dh	---	DMA overflow enable register

Pin Mux Configuration

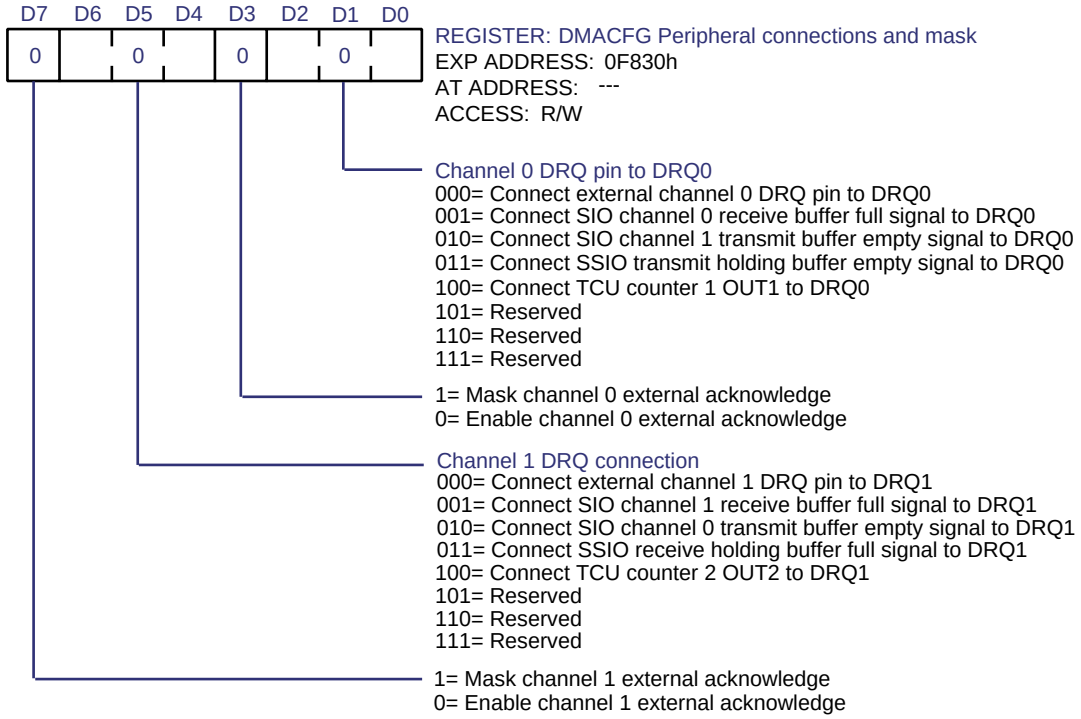
The PINCFG register is used to connect /EOP and /DACK1 to the package pins.



PINCFG Register

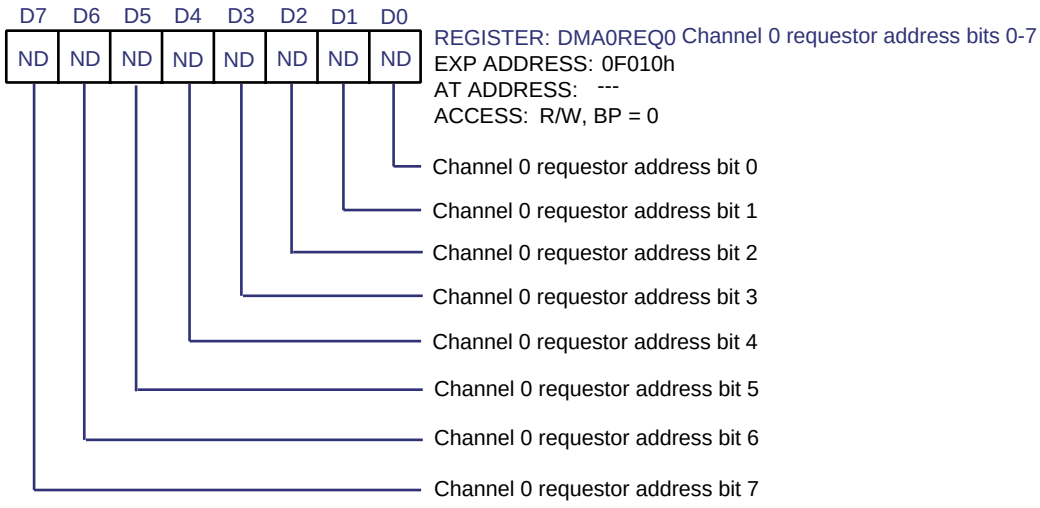
Peripheral Connections and Mask

The DMACFG register is used to select of the hardware DRQ sources for each channel and to mask the /DACKn signals at their pins when using internal requesters.

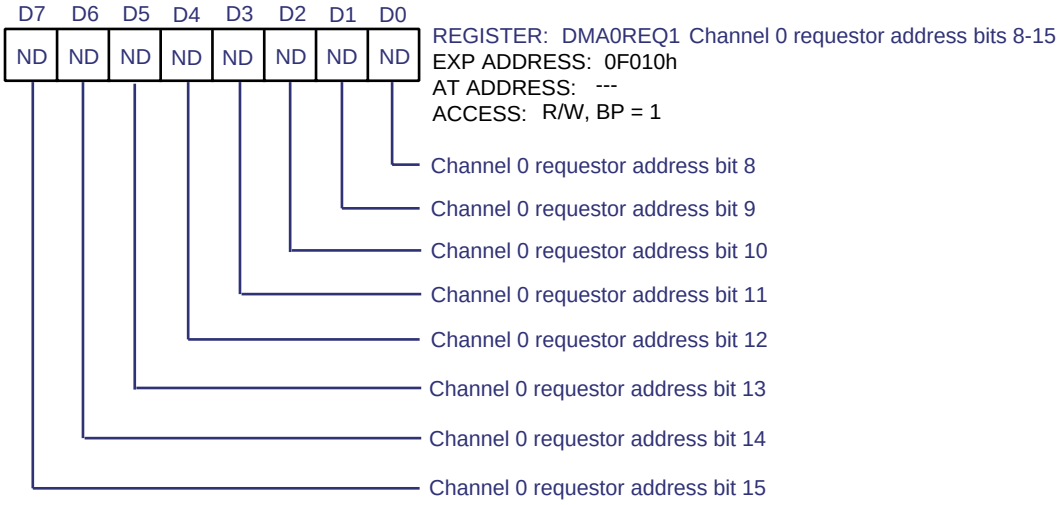


DMACFG Register

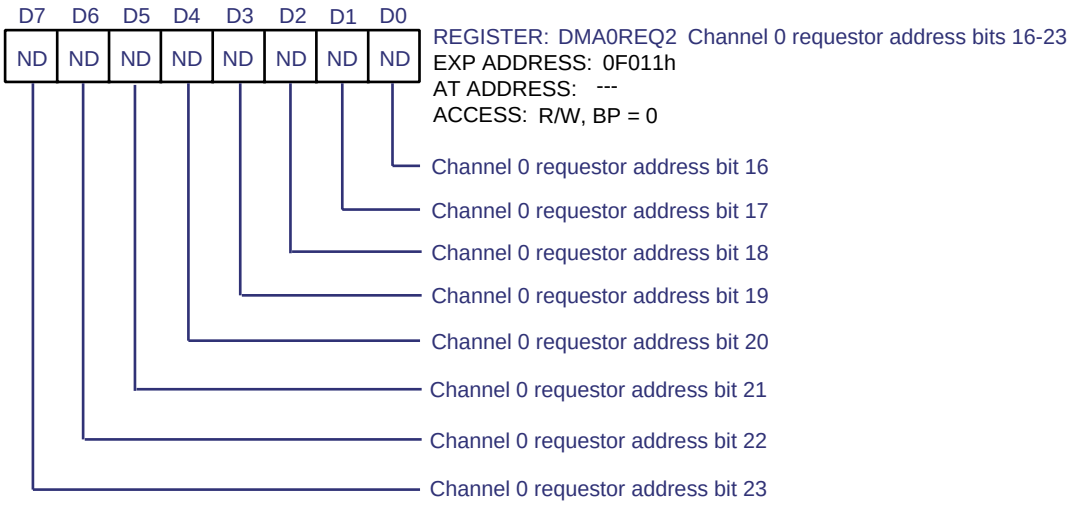
Channel 0 Requestor Address Registers



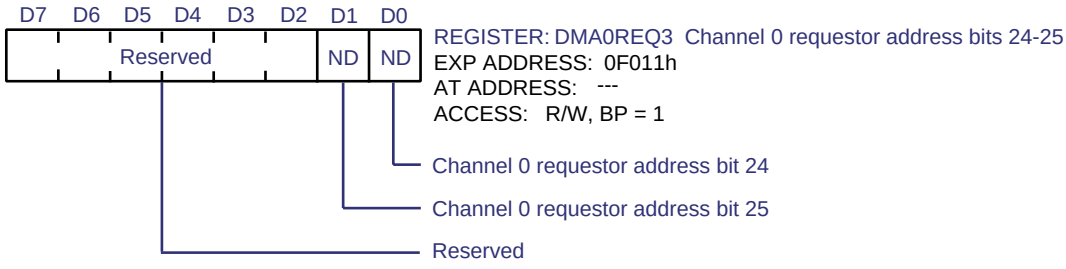
Channel 0 Requestor Address Bits 0-7



Channel 0 Requestor Address Bits 8-15

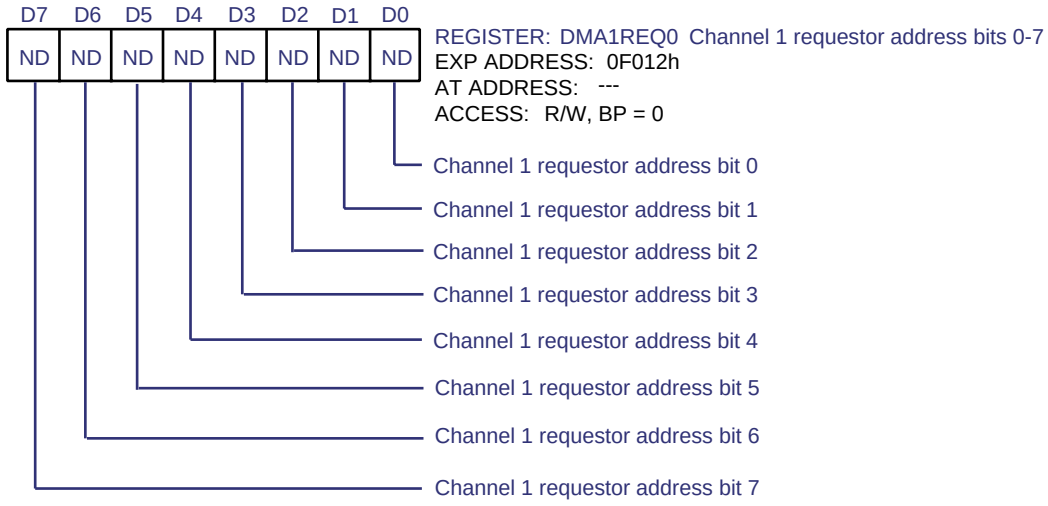


Channel 0 Requestor Address Bits 16-23

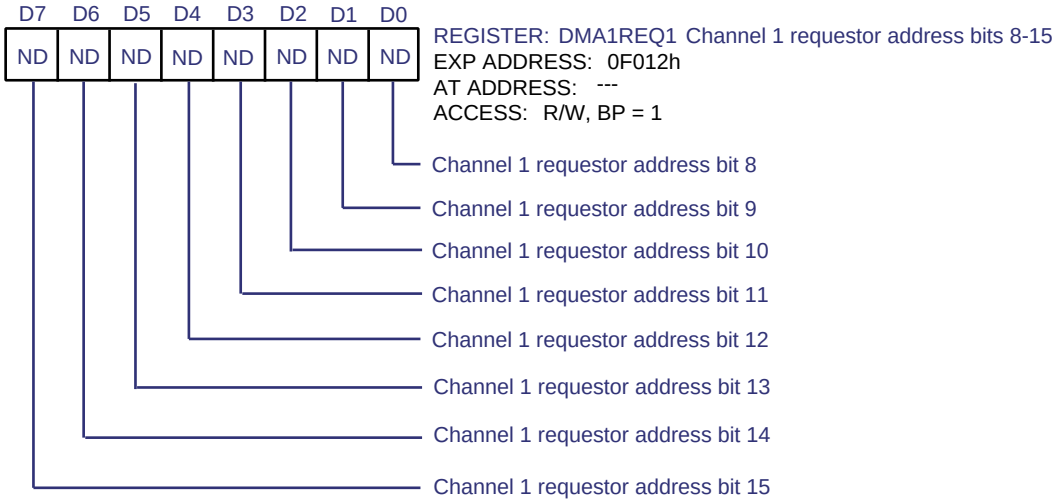


Channel 0 Requestor Address Bits 24-25

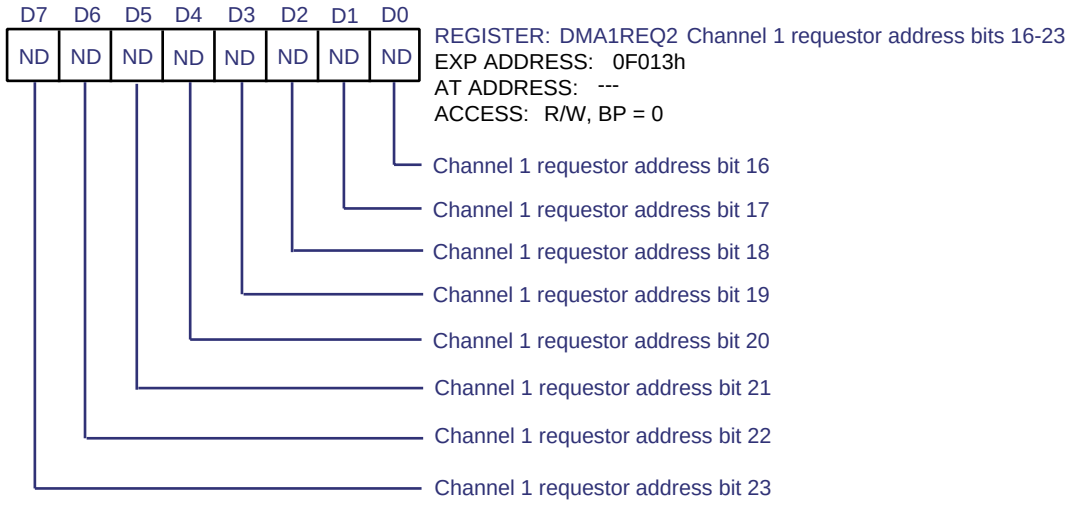
Channel 1 Requestor Address Registers



Channel 1 Requestor Address Bits 0-7



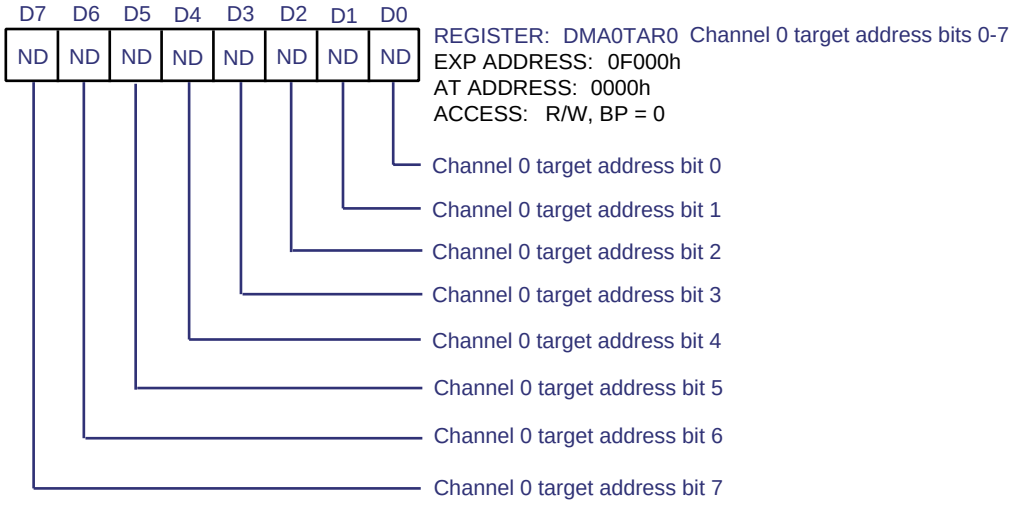
Channel 1 Requestor Address Bits 8-15



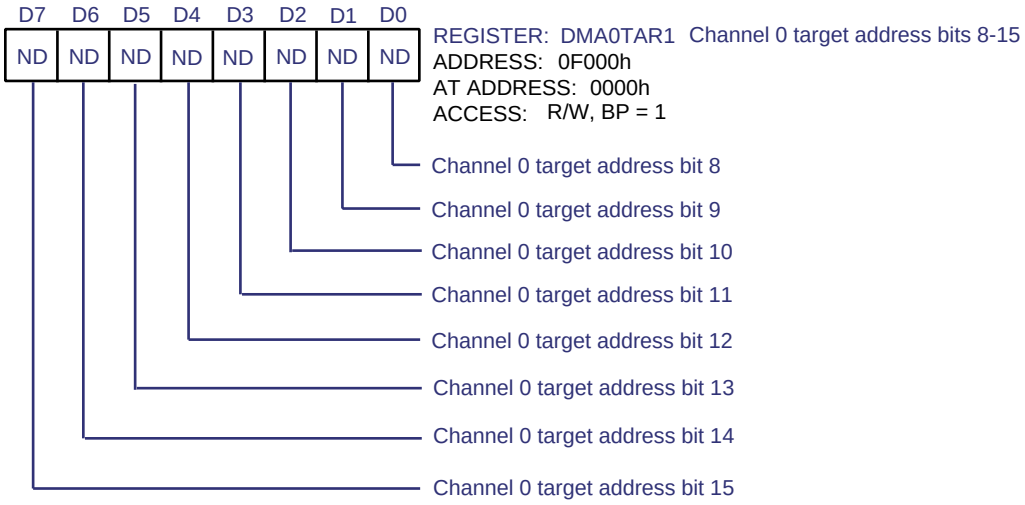
Channel 1 Requestor Address Bits 16-23

Channel 1 Requestor Address Bits 24-25

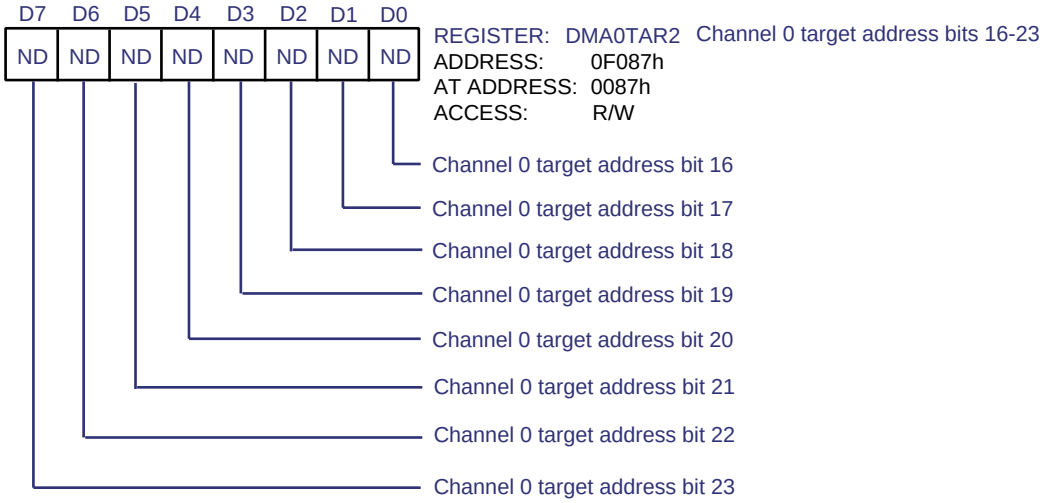
Channel 0 Target Address Registers



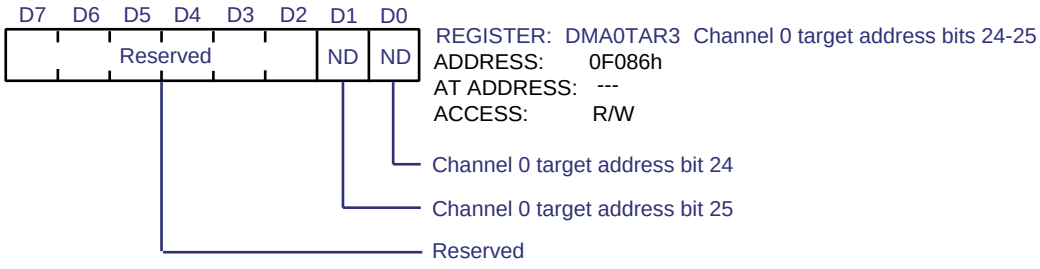
Channel 0 Target Address Bits 0-7



Channel 0 Target Address Bits 8-15

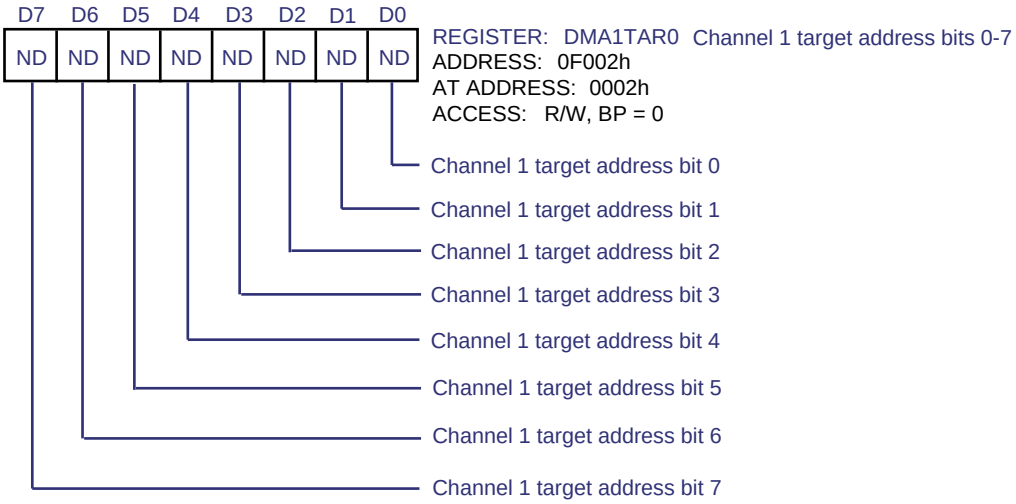


Channel 0 Target Address Bits 16-23

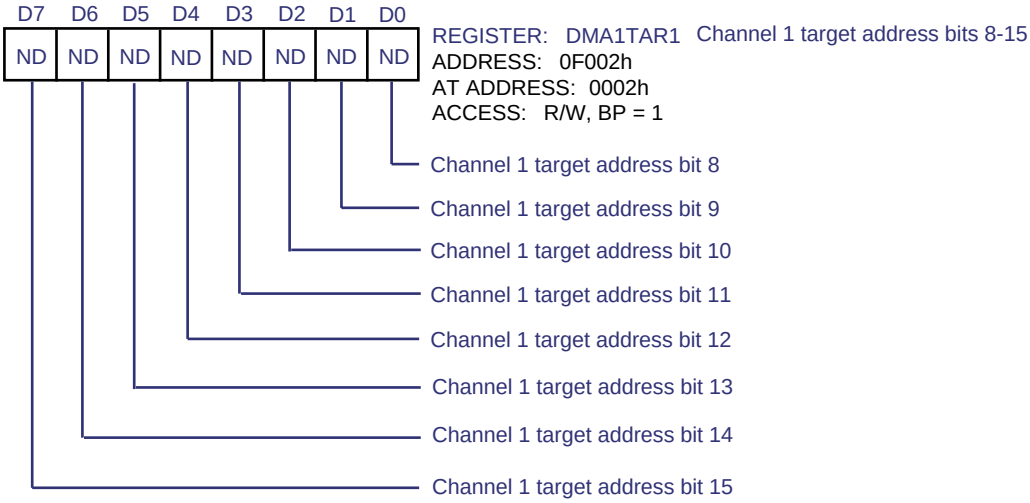


Channel 0 Target Address Bits 24-25

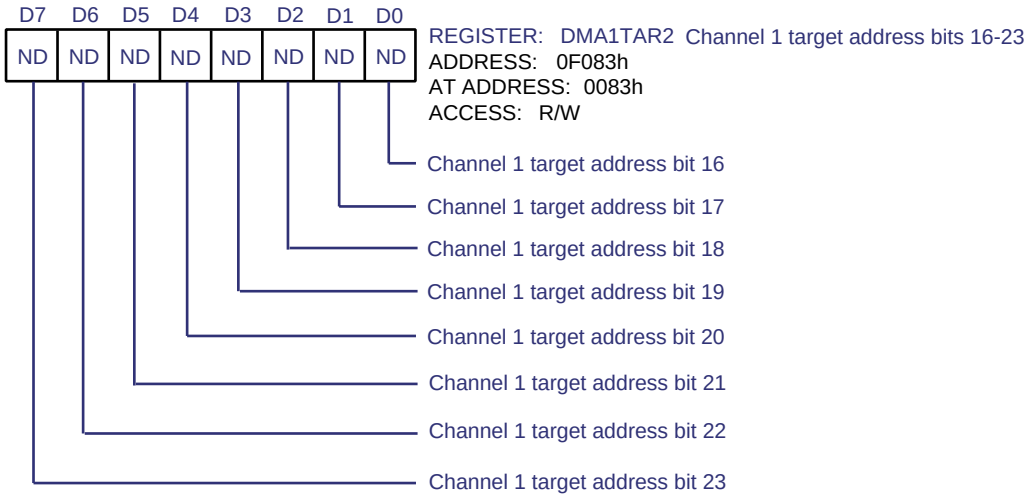
Channel 1 Target Address Registers



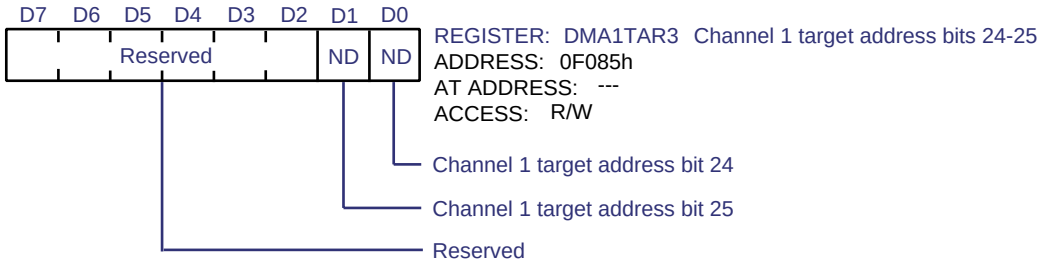
Channel 1 Target Address Bits 0-7



Channel 1 Target Address Bits 8-15

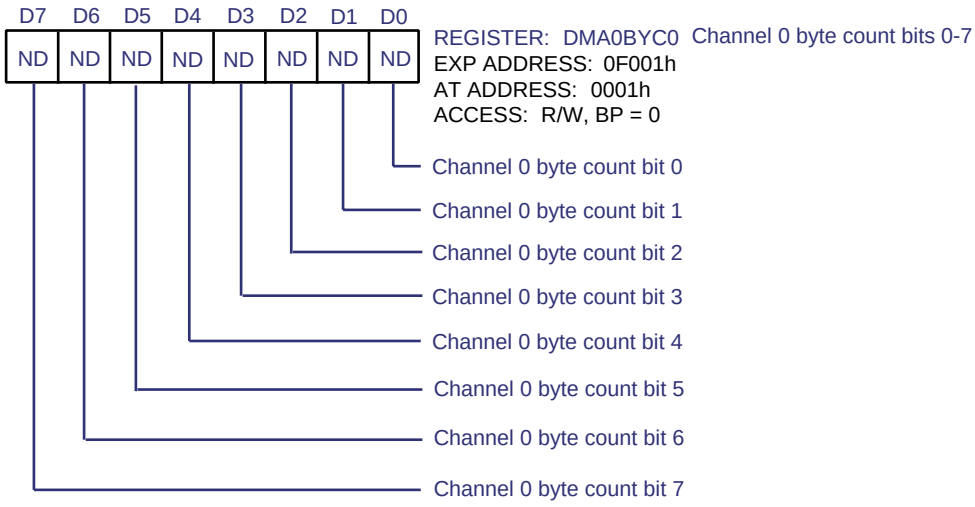


Channel 1 Target Address Bits 16-23

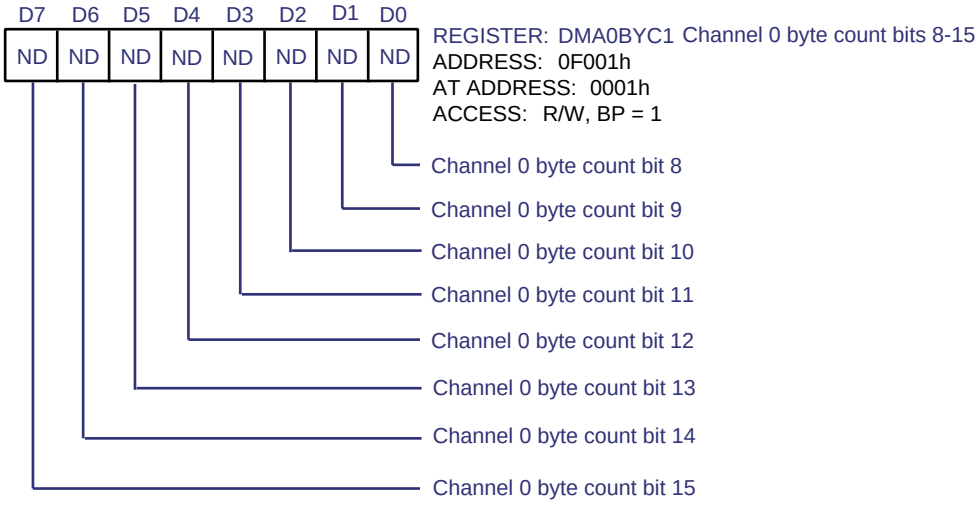


Channel 1 Target Address Bits 24-25

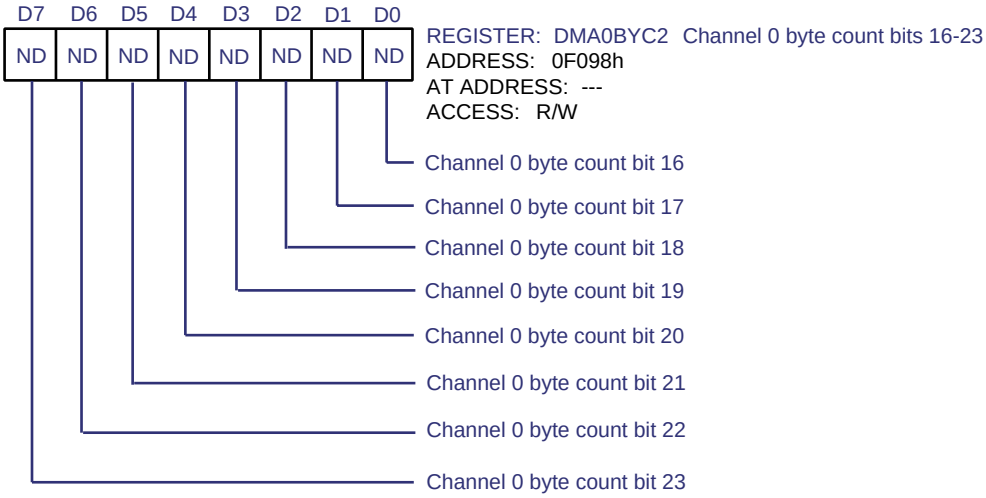
Channel 0 Byte Count Registers



Channel 0 Byte Count Bits 0-7

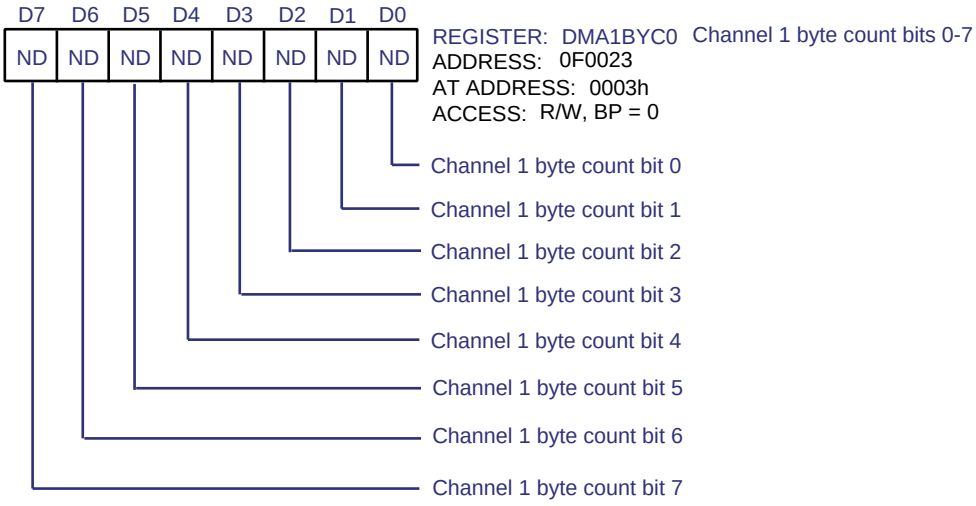


Channel 0 Byte Count Bits 8-15

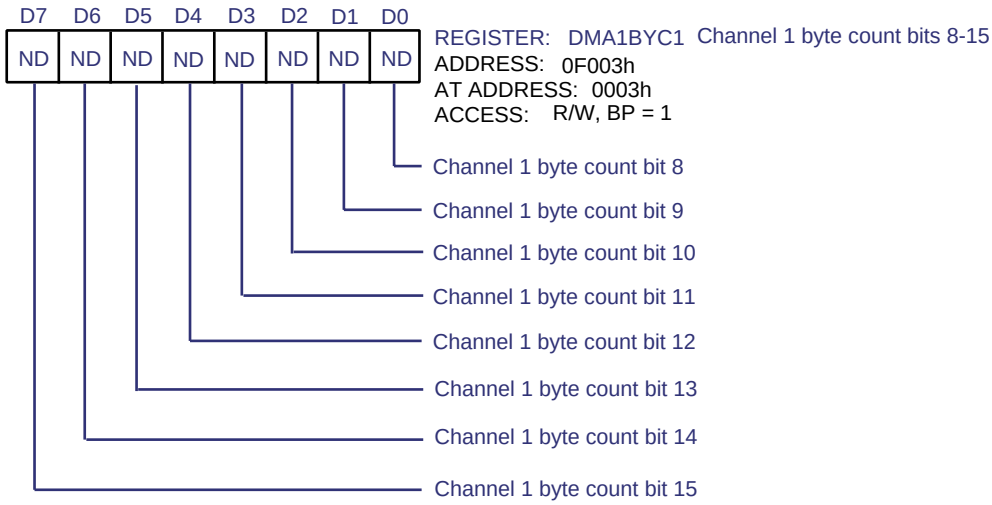


Channel 0 Byte Count Bits 16-23

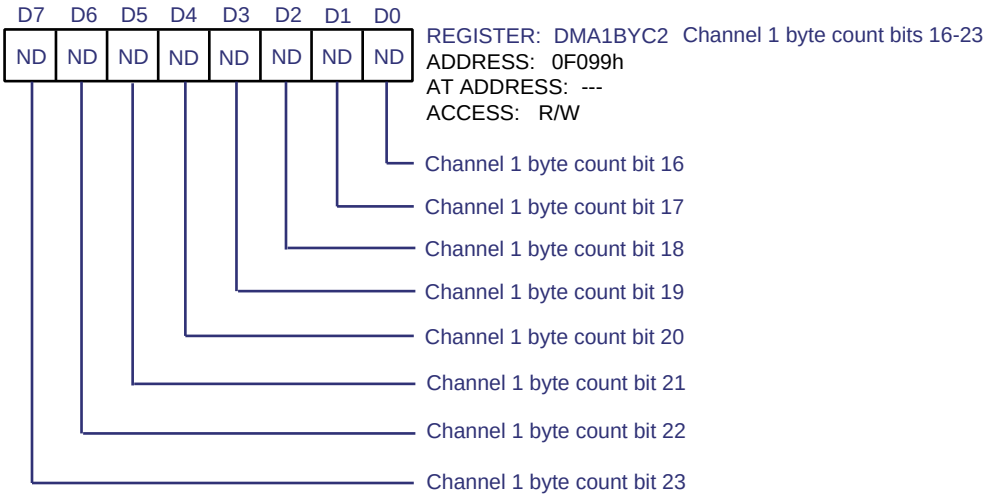
Channel 1 Byte Count Registers



Channel 1 Byte Count Bits 0-7



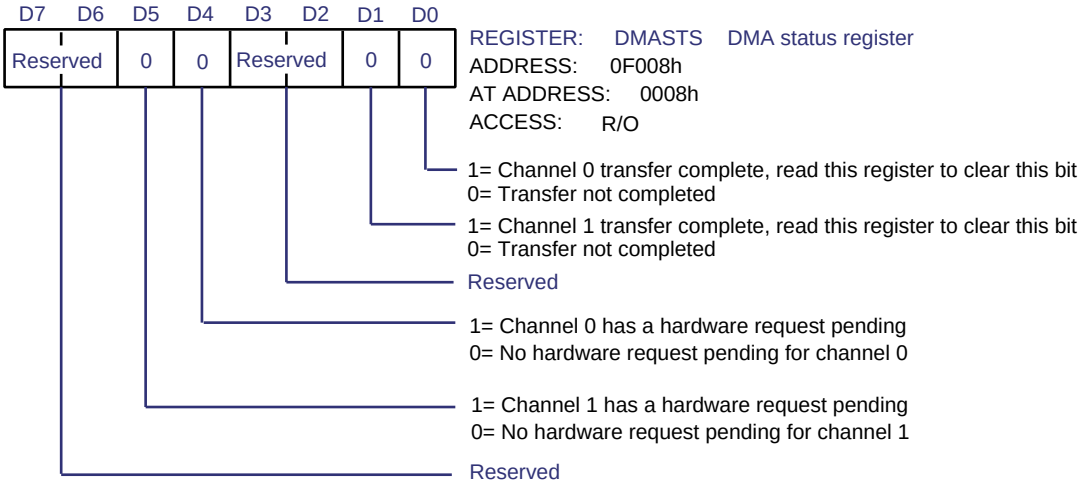
Channel 1 Byte Count Bits 8-15



Channel 1 Byte Count Bits 16-23

DMA Status Register

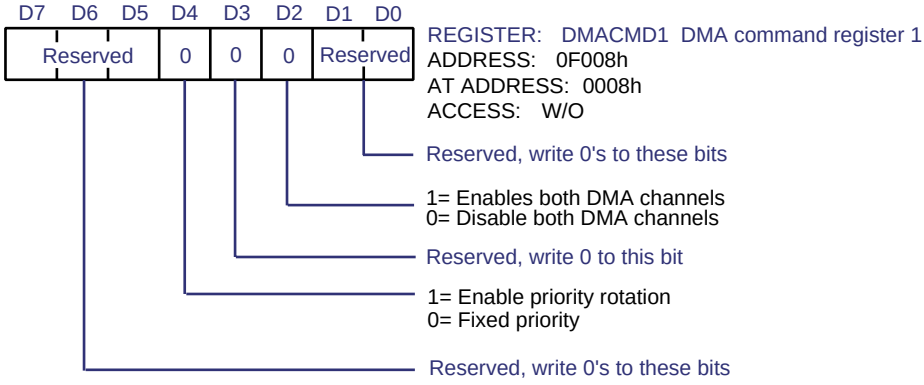
The DMASTS register is used to check channel status individually. The DMA controller sets bits in this register to indicate that a channel has a hardware request pending or that a channel's byte count has expired.



DMA Status Register

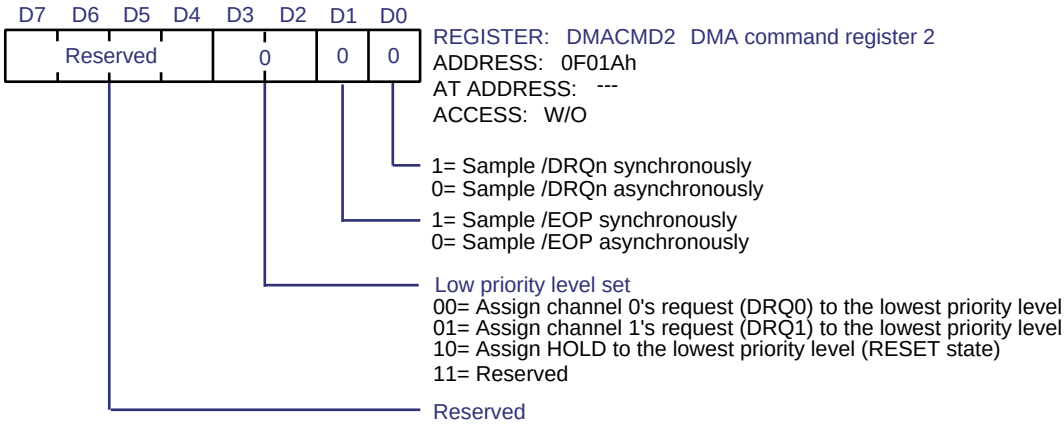
DMA Command Registers

The DMACMD1 resister is used to enable both channels and to select the rotating method for changing the bus priority control structure. Under all prioritization schemes, the DRAM refresh control unit receives highest priority.



DMA Command Register 1

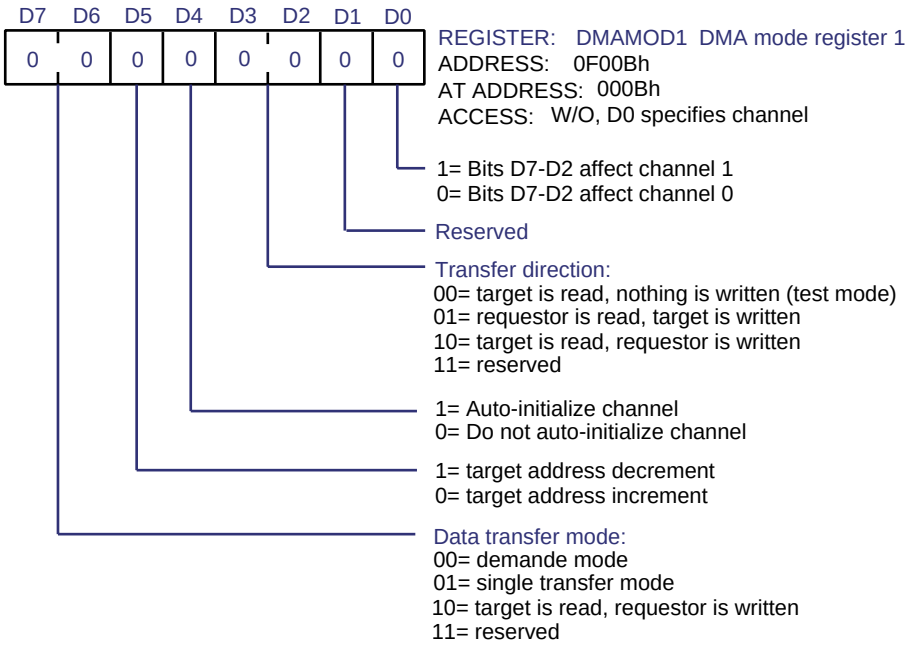
The DMACMD2 register is used to select the type of DRQn and /EOP sampling used, and to assign a particular bus request to the lowest priority level.



DMA Command Register 2

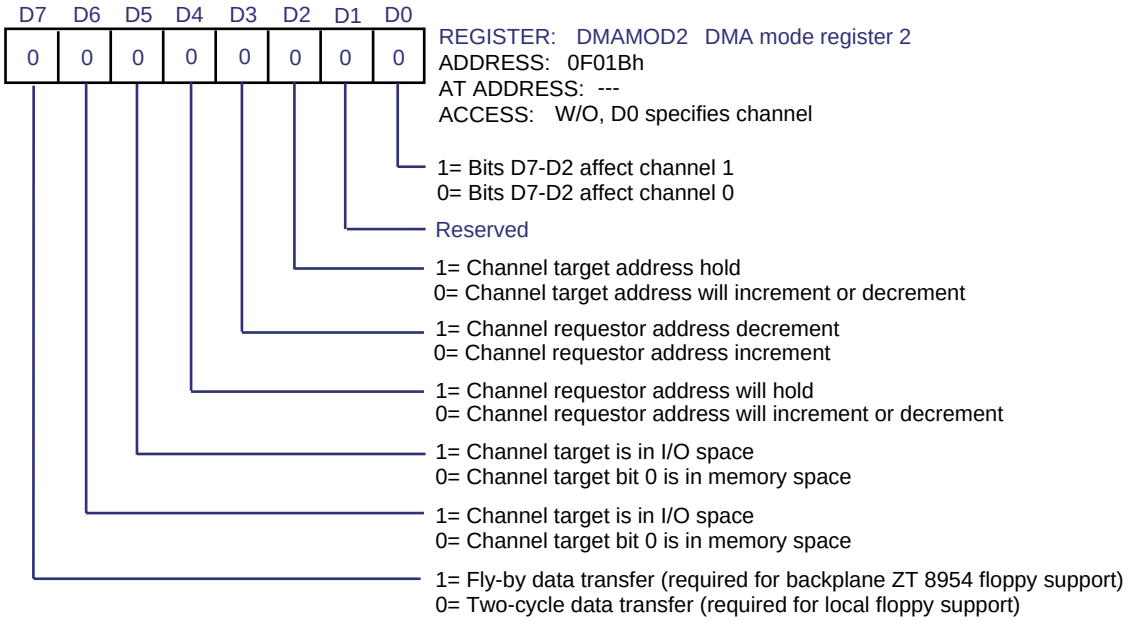
DMA Mode Registers

The DMAMOD 1 register is used to select a particular channel's data-transfer mode and transfer direction, and to enable the channel's auto-initialize buffer-transfer mode. You can configure the DMA controller to modify the target address during a buffer transfer by clearing DMAMOD2.2, then use DMAMOD1.3 to specify how the channel modifies the address.



DMA Mode Register 1

The DMAMOD2 register is used to select the data transfer bus cycle option, specify whether the requestor and target are in memory or I/O, and determine whether the DMA controller will modify the target and requestor addresses.

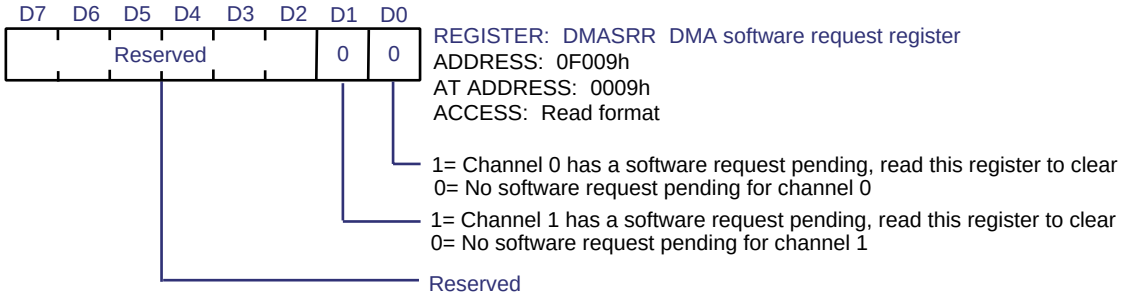


DMA Mode Register 2

DMA Software Request Register

Use the DMASRR register write format to issue software DMA service requests. Software requests are subject to bus control priority arbitration with all other software and hardware requests. A software request activates the internal channel request signal. This signal remains active until the channel completes its buffer transfer. In the demand data-transfer mode, a buffer transfer is suspended by deactivating the channel request signal. Because you cannot deactivate the internal channel request signal before the end of a buffer transfer, you cannot use software requests with demand data-transfer mode.

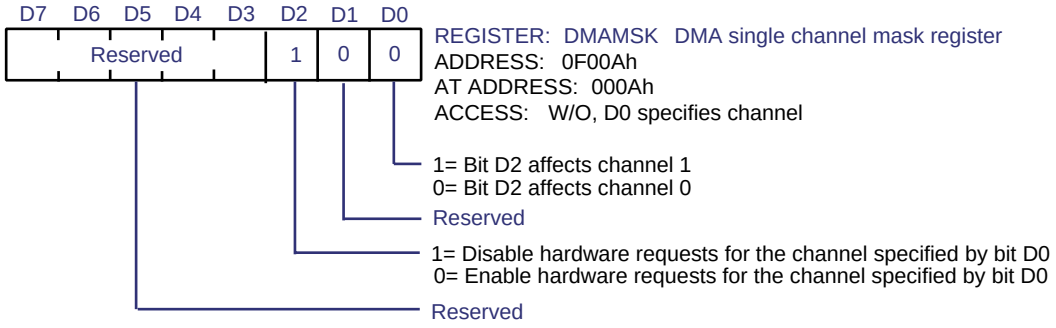
Use the DMASRR register (read format) to determine if a software request for a particular channel is pending.



DMA Software Request Register

DMA Single Channel Mask Register

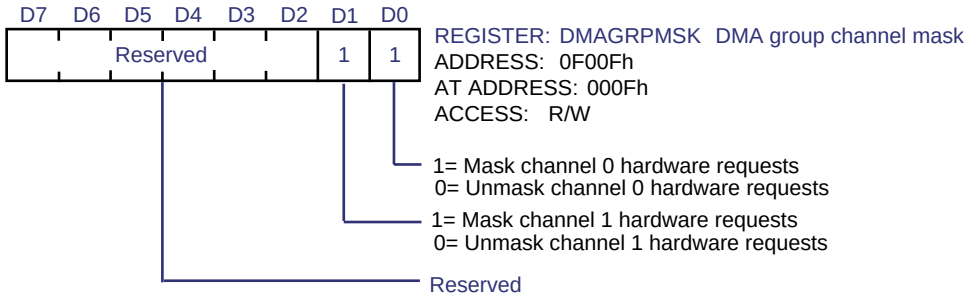
Use the DMAMSK register to enable or disable hardware requests for one channel at a time.



DMA Single Channel Mask Register

DMA Group Channel Mask

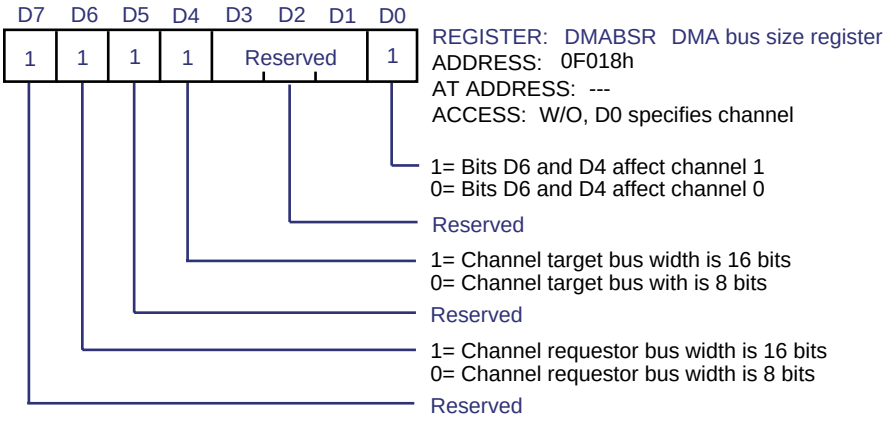
Use the DMAGRPMSK register to enable or disable hardware requests for both channels at the same time.



DMA Group Channel Mask

DMA Bus Size Register

The DMABSR register determines the requestor and target data bus widths (8 / 16 bits).

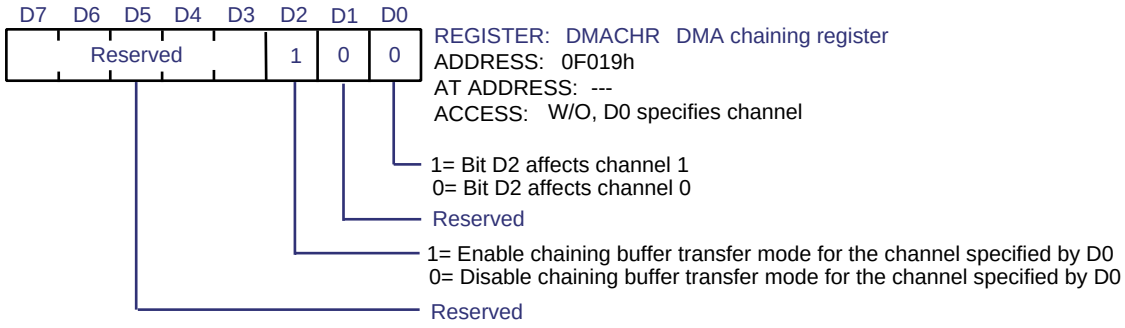


DMA Bus Size Register

DMA Chaining Register

The DMACHR register is used to enable and disable the chaining buffer-transfer mode for a selected channel. The following steps describe how to set up a channel to perform chaining buffers transfers.

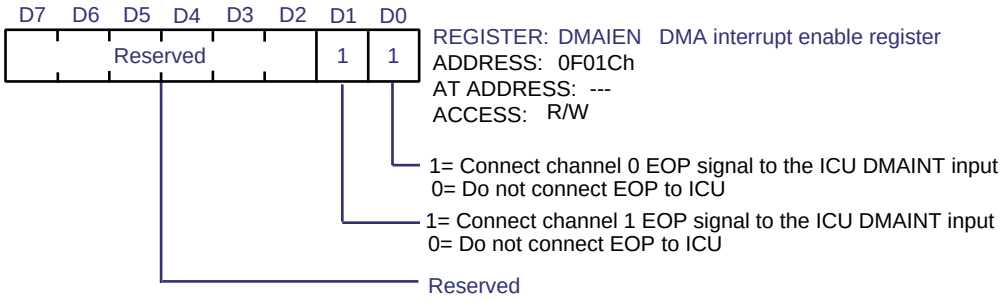
1. Set up the chaining interrupt (DMAINT) service routine.
2. Configure the channel for single buffer-transfer mode.
3. Program the mode registers.
4. Program the target address, requestor address, and byte count registers.
5. Enable the channel for the chaining buffer-transfer mode. This activates the chaining status signal.
6. Enable the DMAINT interrupt and service it. The service routine should load the transfer information for the next buffer transfer.
7. Enable the channel.



DMA Chaining Register

DMA Interrupt Enable Register

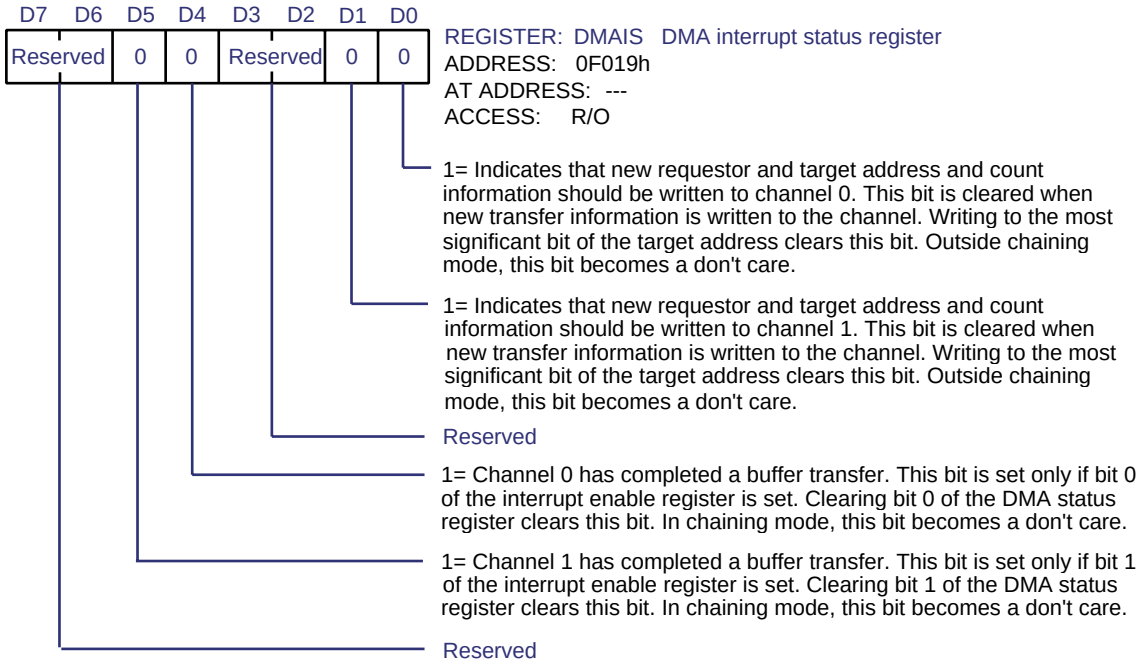
The DMAIEN register is used to individually connect channel 0 and channel 1's transfer complete signal to the ICU's DMAINT interrupt request input.



DMA Interrupt Enable Register

DMA Interrupt Status Register

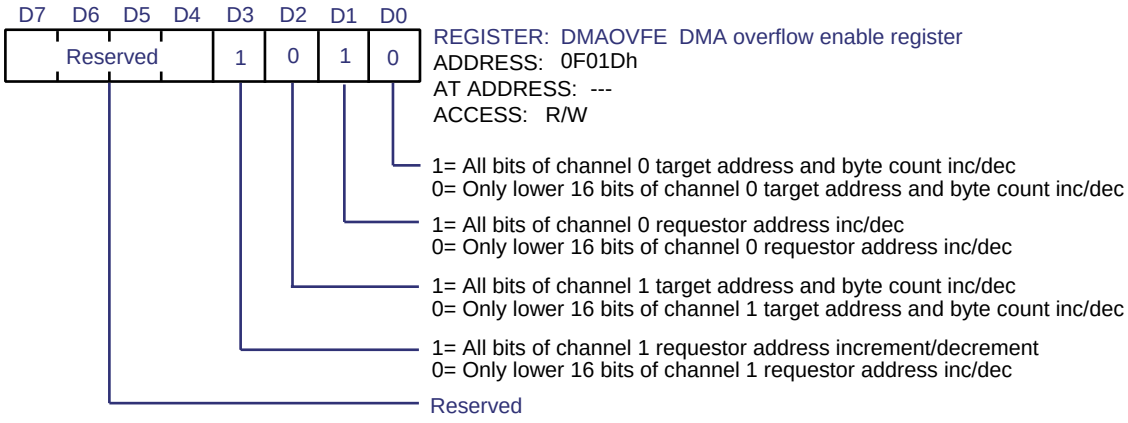
DMAIS indicates which source activated the DMA interrupt request signal (channel 0 transfer complete, channel 1 transfer complete, channel 0 chaining, or channel 1 chaining).



DMA Interrupt Status Register

DMA Overflow Enable Register

Use DMAOVFE to specify whether all 26 bits or only the lower 16 bits of the target and requestor addresses are incremented or decremented during buffer transfers and whether all 24 bits of the byte count or only the lower 16 bits of the byte count are incremented or decremented during buffer transfers. A byte count configured for 16-bit decrementing expires when it is decremented from 0000h to FFFFh.



DMA Overflow Enable Register

7. REAL-TIME CLOCK

The ZT 8904 includes one Motorola®-compatible 146818 real-time clock. The real-time clock provides clock and 100-year calendar information in addition to 242 bytes of CMOS setup static RAM. These functions are battery backed for continuous operation even in the absence of system power. The RAM is used by the operating system BIOS to store configuration information. The major features of the real-time clock are listed below.

- Timekeeping to a 1 second resolution
- More than 200 bytes of CMOS setup RAM
- Leap year compensation
- Daylight Savings Time compensation
- Periodic, Alarm, and Update Ended interrupts
- Battery backed

PROGRAMMABLE REGISTERS

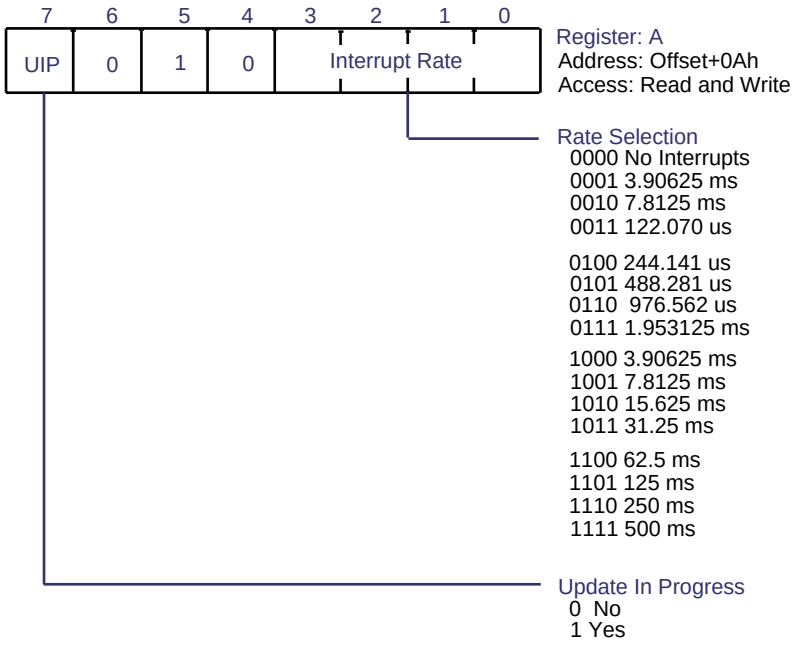
The real-time clock includes 64 register locations. These registers are accessed through I/O port locations 70h and 71h. A real-time clock register is accessed by first writing the offset address of the register to I/O port location 70h. Data is then transferred to or from the register through I/O port location 71h. This sequence must be repeated to read the same register a second time. The I/O port addressing for the real-time clock is given in the "Real-Time Clock Register Addressing" table following.

The following topics illustrate the programmable registers for the real-time clock.

Real-Time Clock Register Addressing

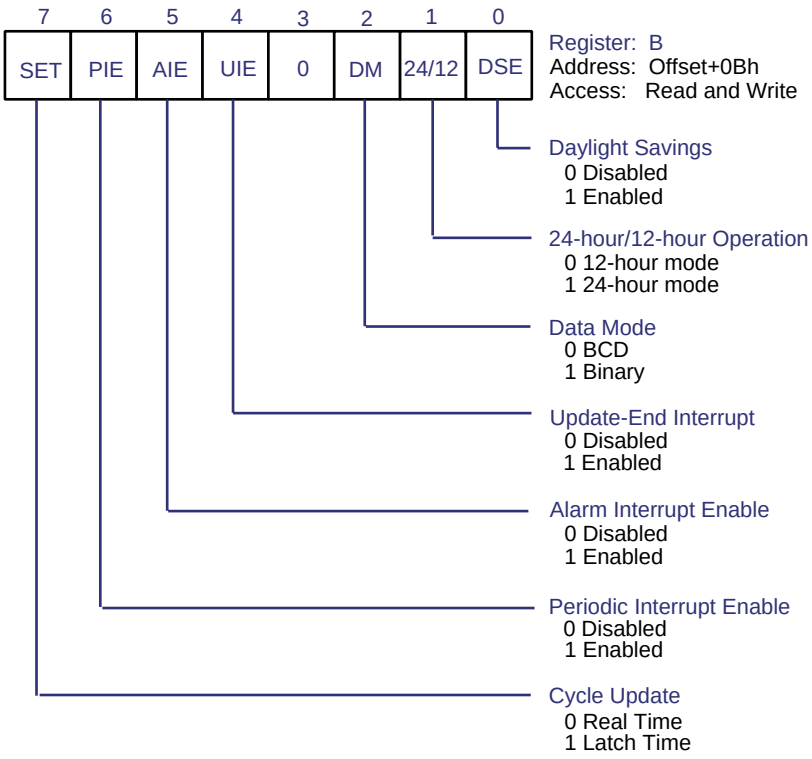
Address Offset	Function	Range
0h	Time-Seconds	0-59
1h	Alarm-Seconds	0-59
2h	Time-Minutes	0-59
3h	Alarm-Minutes	0-59
4h	Time-Hours (12 hour mode)	1-12
4h	Time-Hours (24 hour mode)	0-23
5h	Alarm-Hours	0-23
6h	Day of Week	1-7
7h	Date of Month	1-31
8h	Month	1-12
9h	Year	0-99
Ah-Dh	Register A-D	----
Eh-3Fh	General Purpose	----

Register A



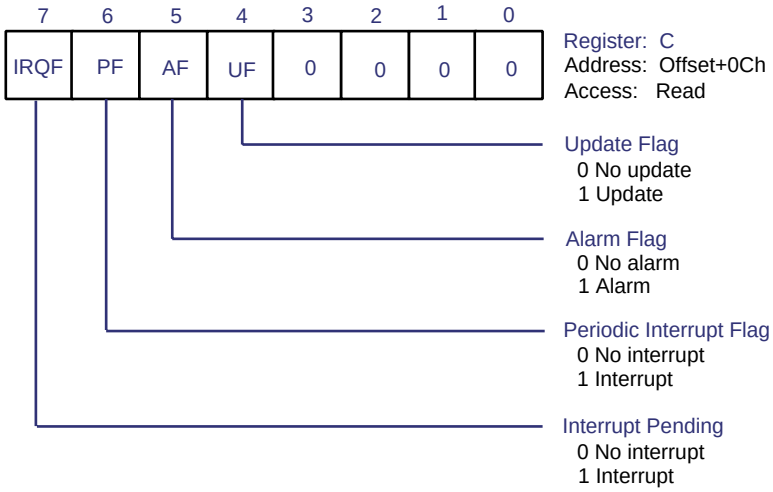
Register A

Register B



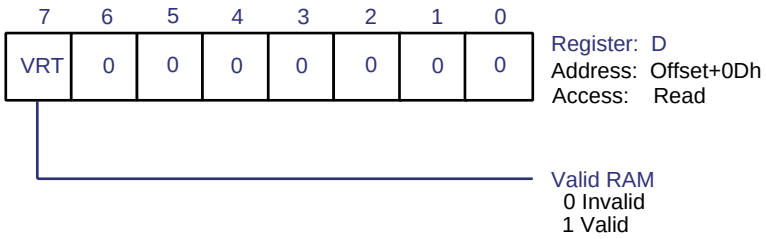
Register B

Register C



Register C

Register D



Register D

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87306 datasheet for more information on the real-time clock operating modes. The product folder for the PC87306, including the data sheet, is available on the web site http://www.national.com/pf/PC/PC87306.html.

8. SERIAL CONTROLLER

This chapter discusses operation of the four ZT 8904 serial ports. It provides descriptions of the two software-configurable serial port registers included on the ZT 8904.

ZT 8904 SPECIFICS

The ZT 8904 includes four serial ports: two serial ports (COM1 and COM2) compatible with the 16450/8250, and two serial ports (COM3 and COM4) compatible with the 16550. The ZT 8903 includes only two serial ports, COM1 and COM2. The serial ports are implemented with a 5 V charge pump technology to eliminate the need for a ±12 V supply.

The serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115 Kbaud. Two of the serial ports are software configured for either RS-232 or RS-485 operation. Several choices of RS-485 control are available.

The major features of each serial port are listed below.

- Two RS-232 channels
- Two RS-232 or RS-485 channels (ZT 8904 and ZT 89CT04 only)
- Does not require ±12 V
- Baud rates up to 115 Kbaud
- Polled and interrupt operation
- Loopback diagnostics

Architectural differences between the four serial ports on the ZT 8904 and the COM1-COM4 serial ports found in a standard PC architecture are discussed in the following topics.

Address Mapping

The address mapping for the PC standard architecture and the ZT 8904 is shown below.

Serial Channel	PC Port Address	ZT 8904 Port Address
COM1	3F8-3FF	3F8-3FF
COM2	2F8-2FF	2F8-2FF
COM3	3E8-3EF	2E0-2E7
COM4	2E8-2EF	2E8-2EF

Interrupt Selection

The interrupt mapping for the PC standard architecture and the ZT 8904 is shown below. Different interrupt levels for COM3 and COM4 interrupts are selectable through the interrupt jumper block.

Serial Channel	PC Interrupt	ZT 8904 Interrupt
COM1	IR4	IR4
COM2	IR3	IR3
COM3	IR4	IR13
COM4	IR3	IR9

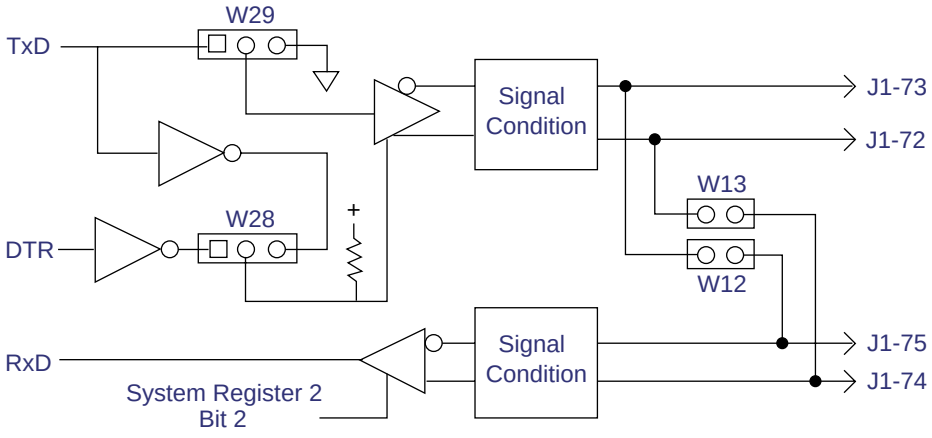
Handshake Signals

The PC architecture includes Transmit Data (TXD), Receive Data (RXD), Request To Send (RTS), Clear To Send (CTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Data Carrier Detect (DCD). The ZT 8904 COM1, COM3, and COM4 channels include a complete set of PC architecture signals.

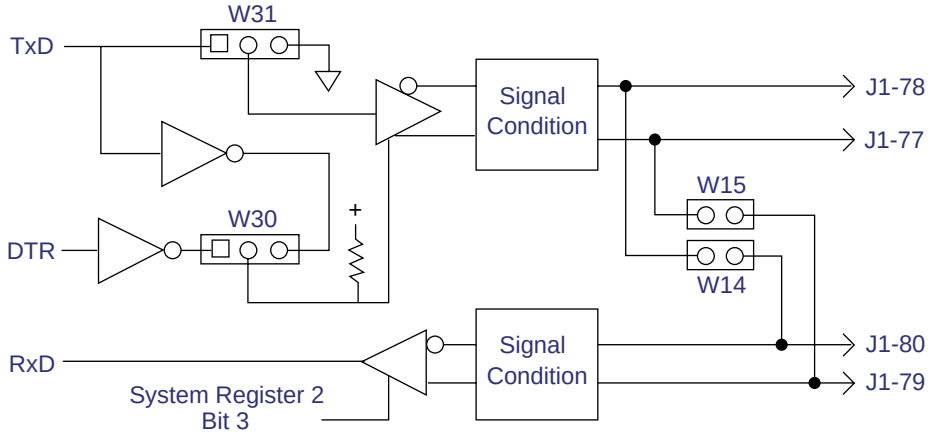
The ZT 8904 COM2 channel shares TXD, RXD, CTS, and DCD with DMA channels 0 and 1 as selected with jumpers W24-W27 and COM2 BIOS configuration. The restrictions imposed by this sharing are that COM2 is not available if printer DMA is enabled and that COM2 is available without CTS and DCD handshake lines if STD Bus DMA is enabled (for example, if an STD Bus floppy disk is installed).

RS-485 Operation

Two of the serial channels, COM1 and COM2, are software programmable for RS-232 or RS-485 operation. The RS-485 functionality is not available on the ZT 8903. The software selection is made through bits 2 and 3 of System Register 2. The RS-485 architecture is shown below.



COM1 RS-485 Architecture



COM2 RS-485 Architecture

Serial Channel Interface

The serial ports are configured as DTE and are available through the 80-pin frontplane connector (J1). Optional cables convert the serial port interface to standard 9-pin D-shell connectors. The ZT 90200 cable provides the serial interface for the ZT 8904 and ZT 89CT04. The ZT 90203 provides the serial interface for the ZT 8903. The J1 connector pin assignments are given in the "J1 Peripheral Pinout" table in Appendix B.

PROGRAMMABLE REGISTERS

Six registers are available for initializing and controlling each serial channel. The following table "Serial Controller Register Addressing" shows the I/O port addressing for the COM1 registers. The remaining serial channels are located as follows:

COM2: 2F8-2FFh

COM3: 2E0-2E7h

COM4: 2E8-2EFh

The topics that follow illustrate the 16-bit divisor latch, baud rate divisors, and the six programmable registers for each serial channel.

Serial Controller Register Addressing

Address	Register	Operation
03F8h (DIV=0)	Receive Buffer	Read
03F8h (DIV=0)	Transmit Buffer	Write
03F8h (DIV=1)	Divisor Latch LSB	Read/Write
03F9h (DIV=0)	Interrupt Control	Read/Write
03F9h (DIV=1)	Divisor Latch MSB	Read/Write
03FAh	Interrupt Status	Read
03FBh	Line Control	Read/Write
03FCh	Modem Control	Read/Write
03FDh	Line Status	Read
03FEh	Modem Status	Read
03FFh	Reserved	

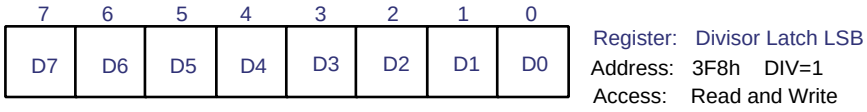
Baud Rate Divisors

The "Divisor Latch LSB" and "Divisor Latch MSB" figures that follow illustrate the 16-bit divisor latch. The "Baud Rate Divisors" table lists the divisors for popular baud rates. It also includes the percent error based on the difference between the exact divisor for a specified baud rate and the divisor obtainable with a 16-bit integer format. To guarantee proper operation, the percent error should never be greater than four.

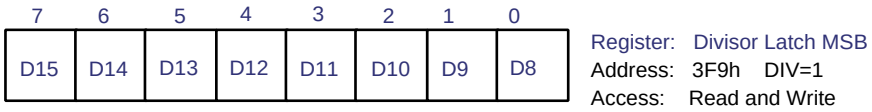
Baud Rate Divisors

Baud Rate	Divisor (dec/hex)	Percent Error
50	2304/1440h	0
75	1536/960h	0
150	768/480h	0
300	384/240h	0
600	192/120h	0
1200	96/60h	0
1800	64/40h	0
2000	58/3Ah	0.69
2400	48/30h	0
3600	32/20h	0
4800	24/18h	0
7200	16/10h	0
9600	12/Ch	0
19200	6/6h	0
38400	3/3h	0
56000	2/2h	2.86
57600	2/2h	0
115200	1/1h	0

Divisor Latch LSB and MSB

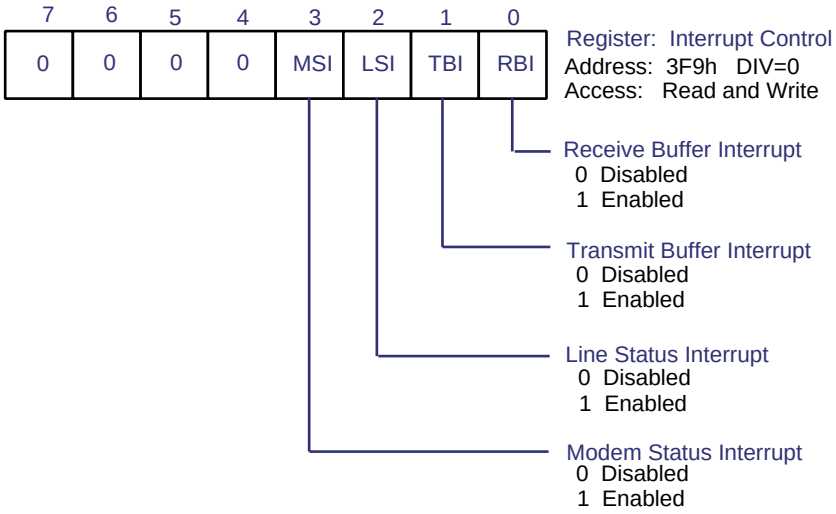


Divisor Latch LSB



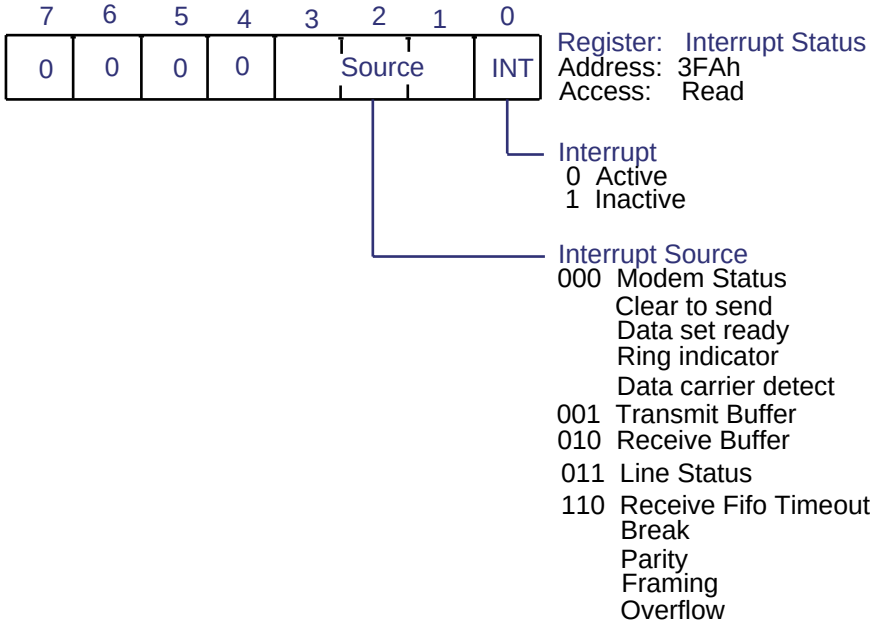
Divisor Latch MSB

Interrupt Control Register



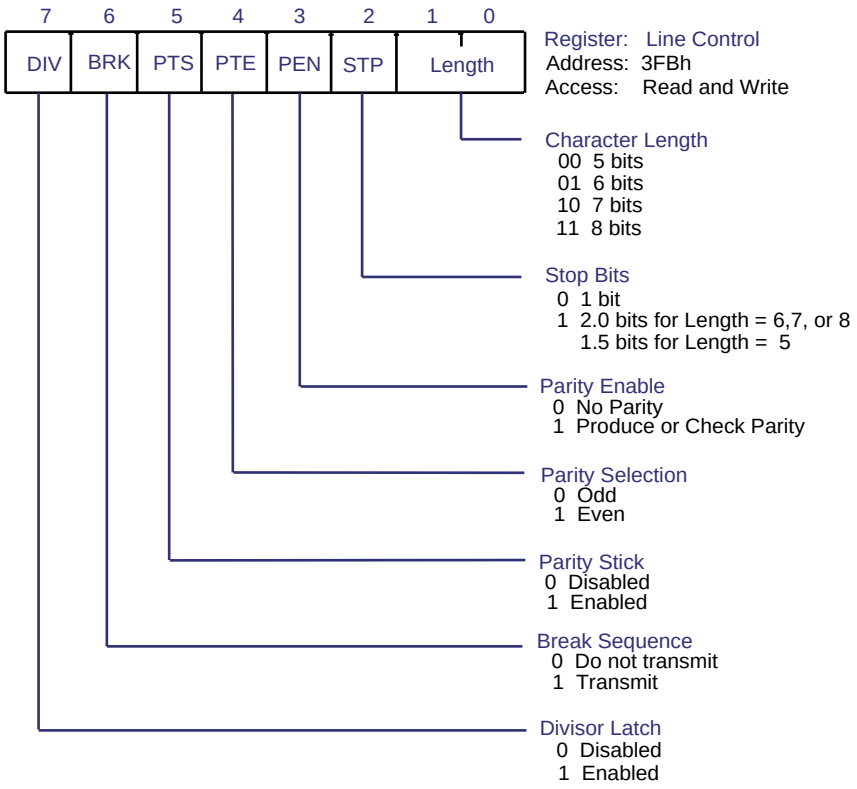
Interrupt Control Register

Interrupt Status Register



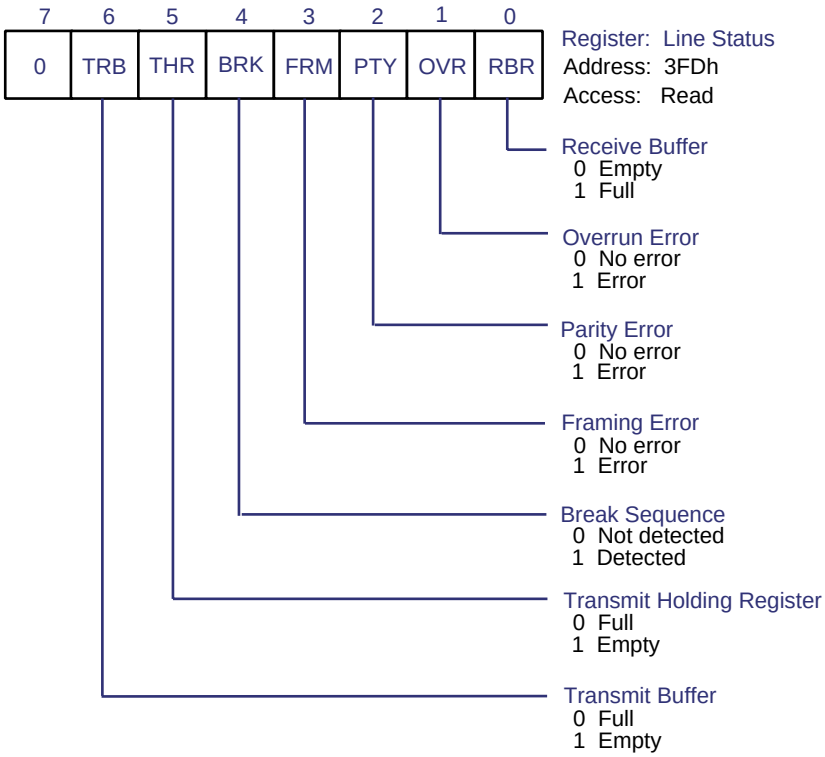
Interrupt Status Register

Line Control Register



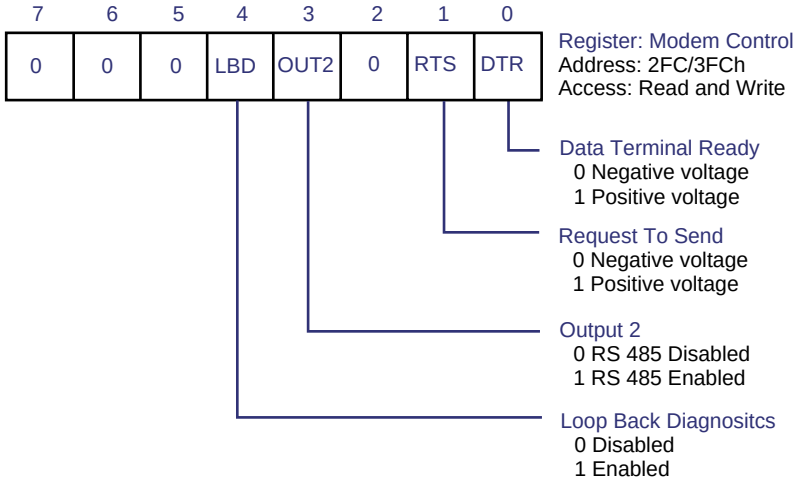
Line Control Register

Line Status Register



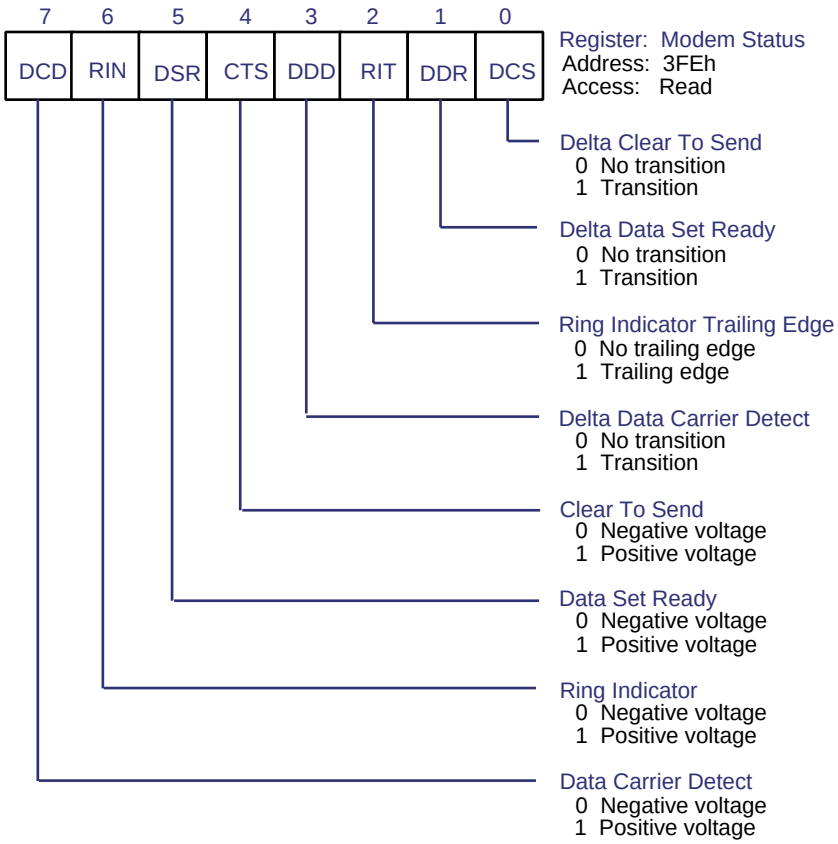
Line Status Register

Modem Control Register



Modem Control Register

Modem Status Register



Modem Status Register

ADDITIONAL INFORMATION

Refer to the Intel 386 EX data book for more information on the COM1 and COM2 serial controller operating modes. A product overview of the Intel 386 EX is available on Intel's web site at http://developer.intel.com/design/intarch/prodbref/27270903.htm.

Refer to the National Semiconductor PC87303 data book for more information on the COM3 and COM4 serial controller operating modes. National's web site is located at http://www.national.com.

9. CENTRONICS PRINTER INTERFACE

The bidirectional printer interface fully supports a Centronics-compatible printer. The Centronics interface is available through the J1 connector. Refer to the table "J1 Peripheral Pinout" in Appendix B for the connector pin assignments.

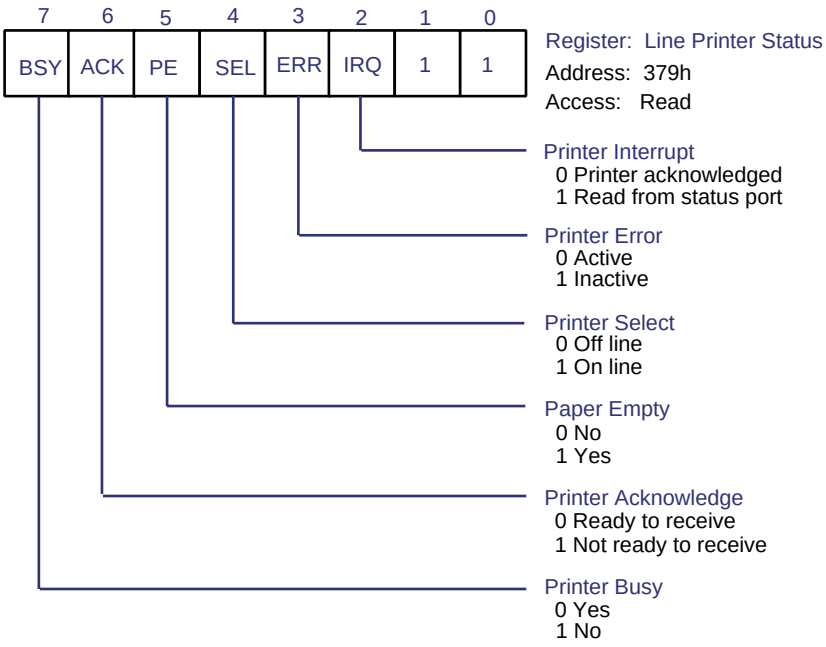
PROGRAMMABLE REGISTERS

The following topics illustrate the programmable registers for the Centronics printer interface.

Line Printer Data Register

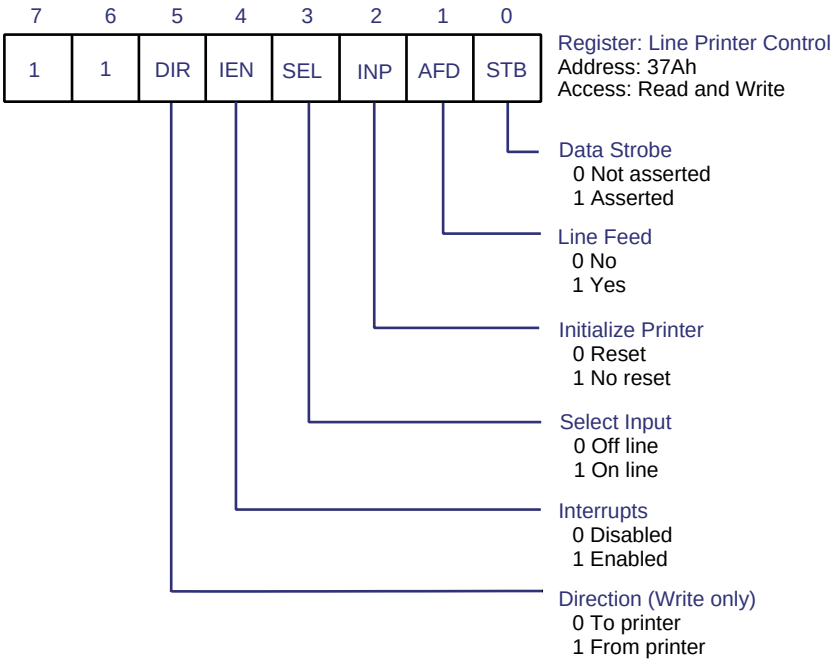
Line Printer Data Register

Line Printer Status Register



Line Printer Status Register

Line Printer Control Register



Line Printer Control Register

ADDITIONAL INFORMATION

Refer to the National Semiconductor PC87303 data book for more information on the Centronics interface operating modes. National's data book is located on the web site at http://www.national.com/pf/PC/PC87303.html.

10. PARALLEL I/O

The ZT 8904 includes six 8-bit parallel ports for a total of 48 I/O signals. Three of the parallel ports are available to the application through frontplane connector J4. The remaining three parallel ports are dedicated to controlling and monitoring local operations. The general operation of the six parallel ports is explained in this chapter. The specific features managed by the dedicated ports are explained in Chapter 11, "System Registers."

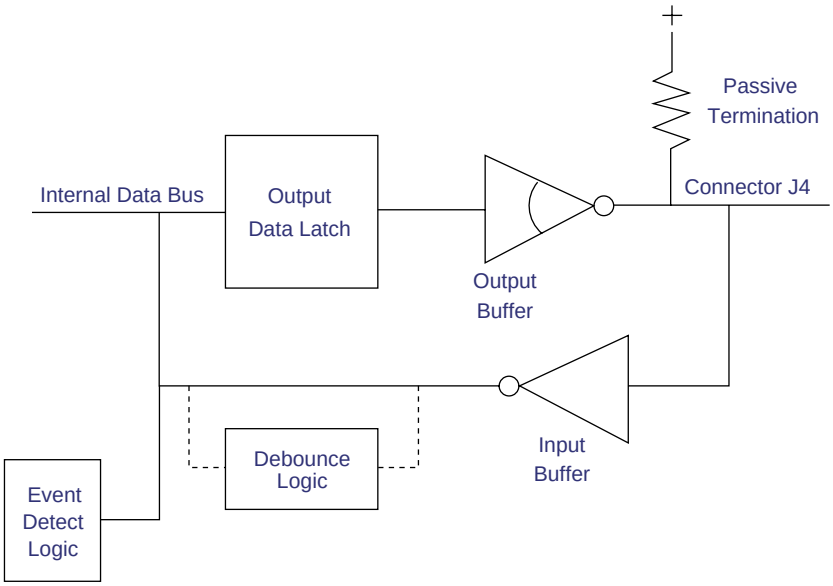
Each of the parallel I/O signals is configured as an input or an output with readback under software control. The major features of the parallel I/O are listed below.

- 12 mA sink current
- Software programmable input debounce
- Stable outputs during power up and reset
- Continuous data transfer rates up to 1 Mbyte/second
- Software programmable event sense interrupt generation
- Each I/O signal is independently programmable as an input or an output with readback
- Optional cable for direct connection to industry-standard I/O module mounting racks

FUNCTIONAL DESCRIPTION

The parallel I/O signals are supported through the 16C50A, a custom ASIC device designed by Ziatech. Refer to Appendix C, "PIA System Setup Considerations," for tips on preventing latchup from the CMOS parts in the 16C50A.

A functional diagram of each I/O signal is illustrated in the following figure. The diagram includes an output latch, an output buffer, and an input buffer. These functional blocks are described in the following topics.



Parallel Port Functional Diagram

Output Latch

The output latch stores the data present on the internal data bus during a write operation to the parallel port. The data is latched until altered by another parallel port write, until a system reset, or until the power is turned off. The output latch is initialized with a logical 0 during power on and system reset.

Output Buffer

The output buffer isolates the output latch from connector J4. The output buffer is an inverting open-collector device with 12 mA of sink current and glitch-free operation during power cycles. The inversion means that a logical 0 written to the parallel port appears as a TTL high at connector J4, and a logical 1 written to the parallel port appears as a TTL low at connector J4.

The open collector feature permits each parallel I/O signal to be software configured as an input. To use a parallel port signal as an input, a logical 0 must first be written to the output latch. This causes the output buffer to become an open-collector gate and prevents contention with the input signal. The passive termination ranges from 25k Ω minimum to 120k Ω maximum. Applications needing a predictable rise time should provide additional termination.

Input Buffer

The input buffer is enabled during read operations to transfer the data from connector J4 to the internal data bus. If the parallel port bit is configured as input, the data read is the data driven by an external device.

The input buffer is an inverting device. This means that data read from the parallel port as a logical 0 is a TTL high at connector J4, and data read from the parallel port as a logical 1 is a TTL low at connector J4.

PROGRAMMABLE REGISTERS

The 16C50A supports standard and enhanced operating modes. Each mode has a different set of registers associated with it.

- The three I/O ports at 78h, 79h, and 7Ah are available through connector J4. Refer to Appendix B, "Specifications," for the connector pin assignments.
- The three I/O ports at 7Bh, 7Ch, and 7Dh are dedicated to managing functions local to the ZT 8904. Refer to Chapter 11, "System Registers," for additional information.

16C50A Standard Operating Mode

Standard operation provides access to all six PIO ports and limited event sense. It is selected after a power cycle or reset.

Standard I/O Port Addressing

Address	Register	Read Operation	Write Operation
0078h	Port 0 Data	MOD00-MOD07	MOD00-MOD07
0079h	Port 1 Data	MOD08-MOD15	MOD08-MOD15
007Ah	Port 2 Data	MOD16-MOD23	MOD16-MOD23
007Bh	System Register 0	-----	-----
007Ch	System Register 1	-----	-----
007Dh	System Register 2	-----	-----
007Eh	Reserved	-----	-----
007Fh	Write Inhibit	Status	Control

16C50A Enhanced Operating Mode

Enhanced operation adds extended event sense and input debounce capabilities. It is selected with four consecutive writes of 07h, 0Dh, 06h, and 12h to I/O port address 7Dh immediately after a power cycle or a reset. Three enhanced register banks are selected by programming bits 6 and 7 of I/O port 7Fh with a 00 for bank 0, a 01 for bank 1, and a 10 for bank 2. Ziatech Industrial Computer Systems software configures the 16C50A for enhanced operation. The Ziatech BIOS initializes the ZT 8904 for enhanced operation at BIOS revision 4.41 or later.

Enhanced Bank 0 I/O Port Addressing

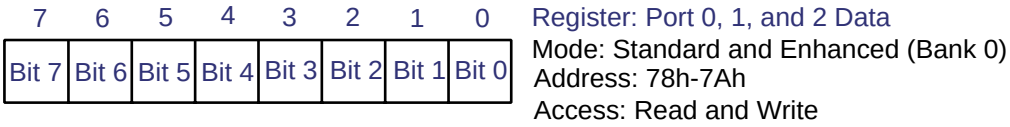
Address	Register	Read Operation	Write Operation
0078h	Port 0 Data	MOD00-MOD07	MOD00-MOD07
0079h	Port 1 Data	MOD08-MOD15	MOD08-MOD15
007Ah	Port 2 Data	MOD16-MOD23	MOD16-MOD23
007Bh	System Register 0	-----	-----
007Ch	System Register 1	-----	-----
007Dh	System Register 2	-----	-----
007Eh	Reserved	-----	-----
007Fh	Write Inhibit/Bank Address	Status	Control

Enhanced Bank 1 I/O Port Addressing

Address	Register	Read Operation	Write Operation
0078h	Port 0 Event Sense	Status	Control
0079h	Port 1 Event Sense	Status	Control
007Ah	Port 2 Event Sense	Status	Control
007Bh	Reserved	-----	-----
007Ch	Reserved	-----	-----
007Dh	Reserved	-----	-----
007Eh	Event Sense Manage	Status	Control
007Fh	Bank Address	Status	Control

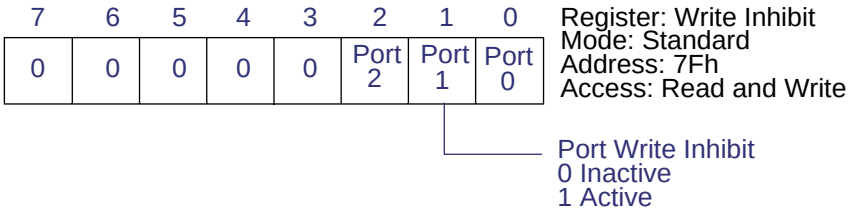
Enhanced Bank 2 I/O Port Addressing

Address	Register	Read Operation	Write Operation
0078h	Debounce Configure	Status	Control
0079h	Debounce Duration	Status	Control
007Ah	Reserved	-----	-----
007Bh	Debounce Clock	-----	Control
007Ch	Reserved	-----	-----
007Dh	Reserved	-----	-----
007Eh	Reserved	-----	-----
007Fh	Bank Address	Status	Control

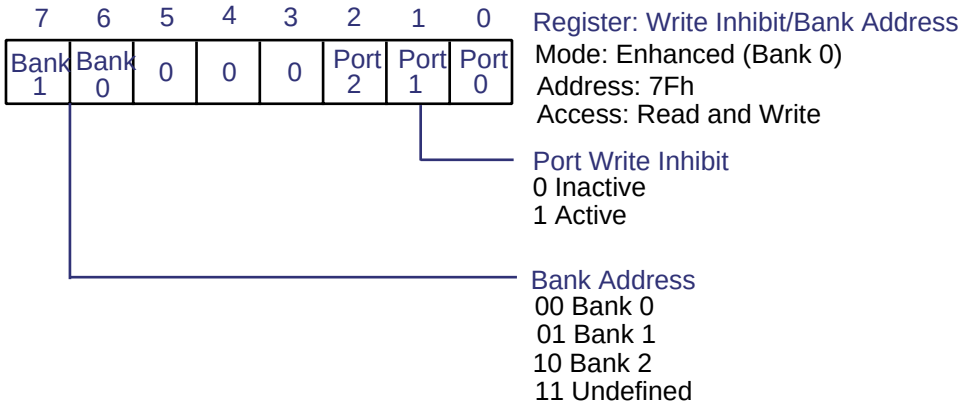


Port Data Register

Note: On a power up or reset, the ports are reset to 0, forcing the outputs to be set high.

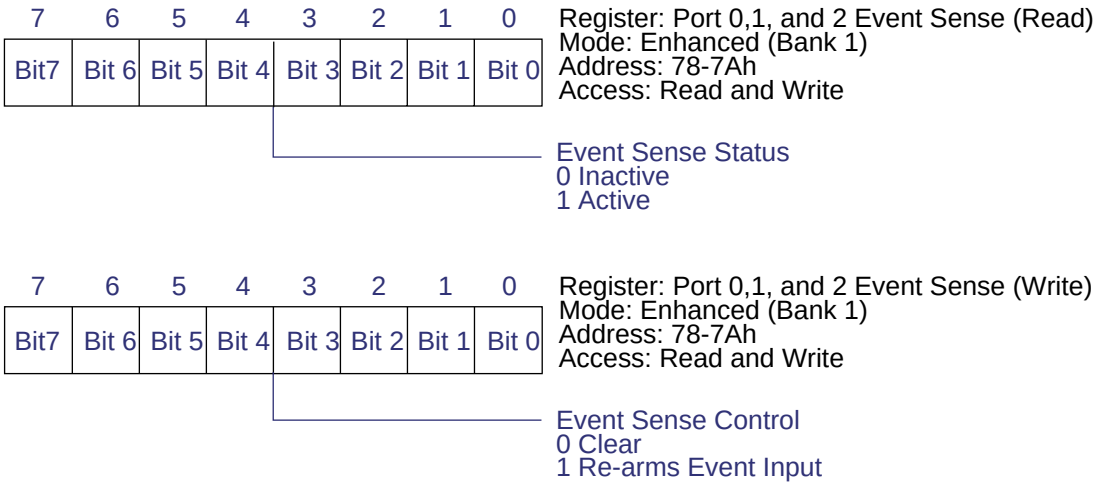


Write Inhibit Register

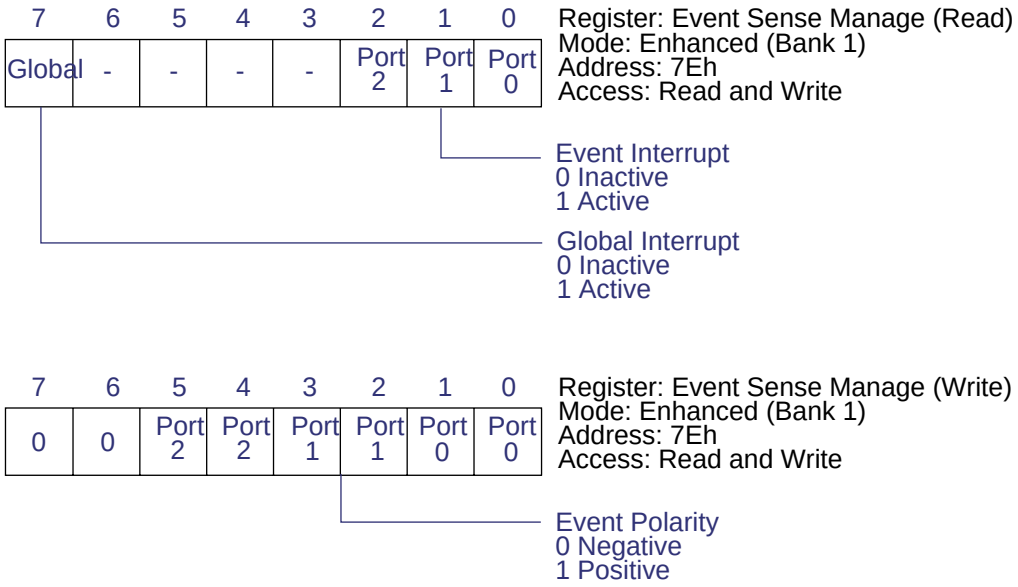


Write Inhibit /Bank Address Register

Note: A 11b is an invalid state and should never be written to the Mask Register.

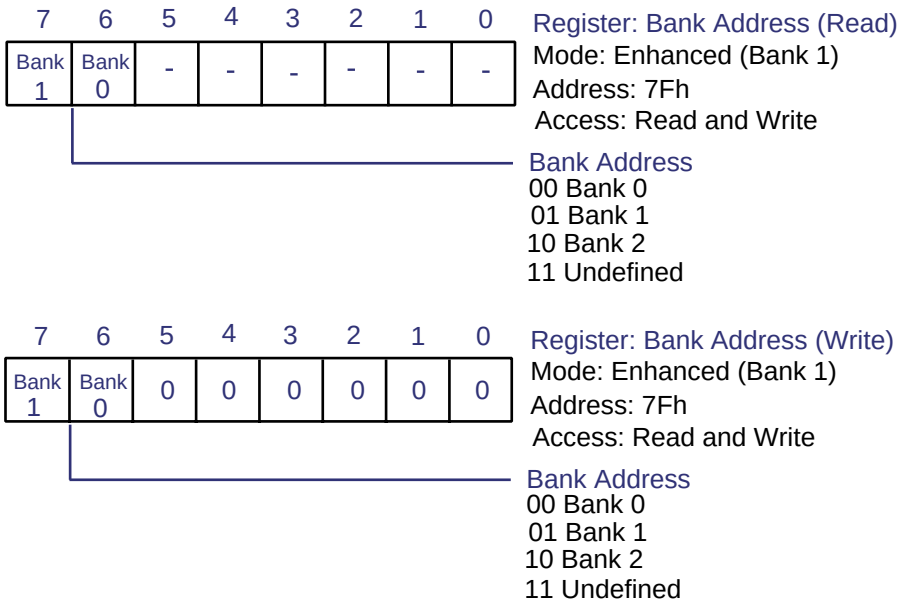


Port Event Sense Register



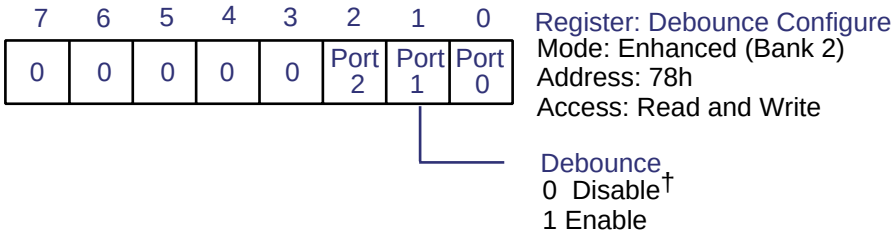
Event Sense Manage Register

Note: The polarity of the event sense logic must be set prior to enabling the event input logic (in enhanced mode).



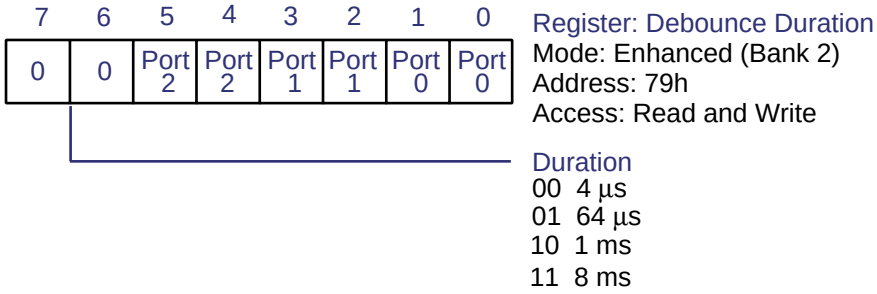
Bank Address Register

Note: A read from this register will return only the bank you are in.



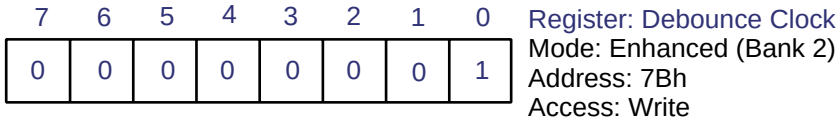
Debounce Configure Register

Note: This register controls whether each individual port or the external sense inputs are passed through the debounce logic before being recognized.



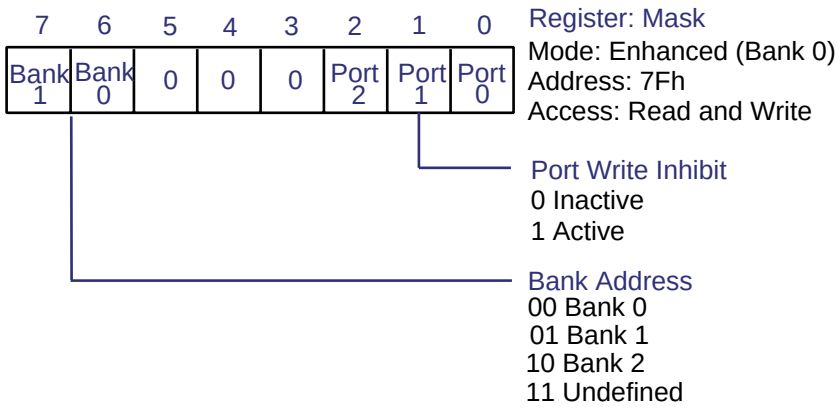
Debounce Duration Register

Note: This register controls the duration required by each input signal before it is recognized by each individual input. Default values are 00, setting a 4µm debounce period.



Debounce Clock Register

† On power up or reset, these bits are set to 0.



Mask Register

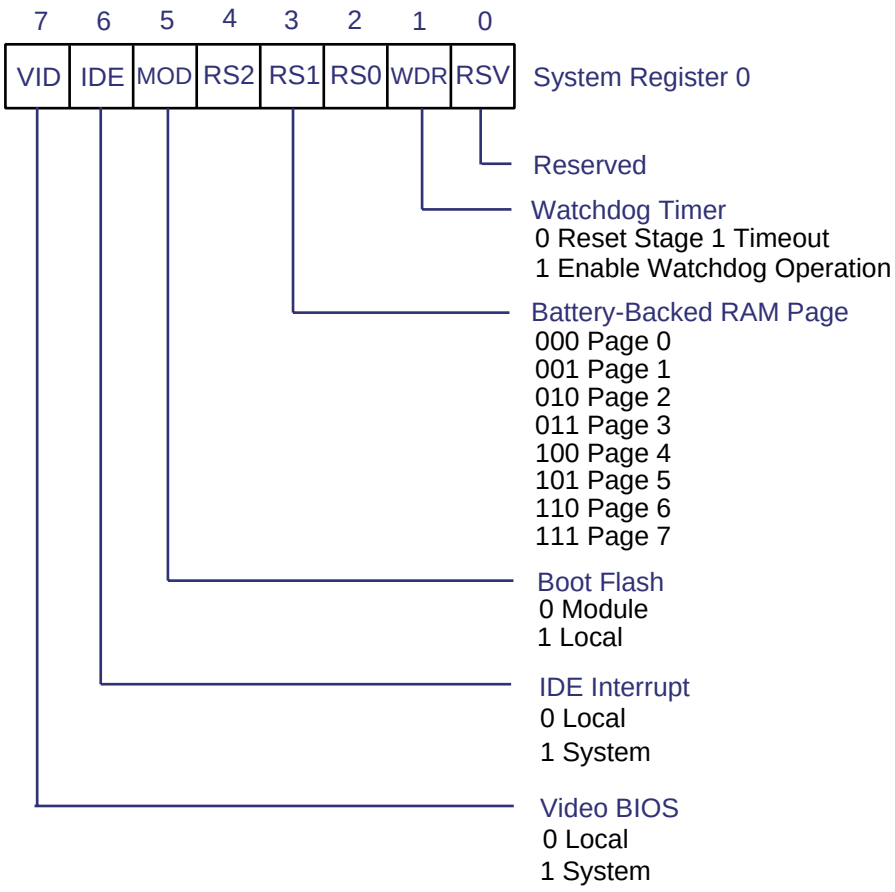
11. SYSTEM REGISTERS

Three system registers are used to control and monitor a variety of functions on the ZT 8904. These registers are implemented with the same Ziatech 16C50A ASIC that implements the 24 parallel I/O lines discussed in "Parallel I/O," Chapter 10. The 16C50A operating instructions are outlined below. Refer to "Parallel I/O" for a complete discussion.

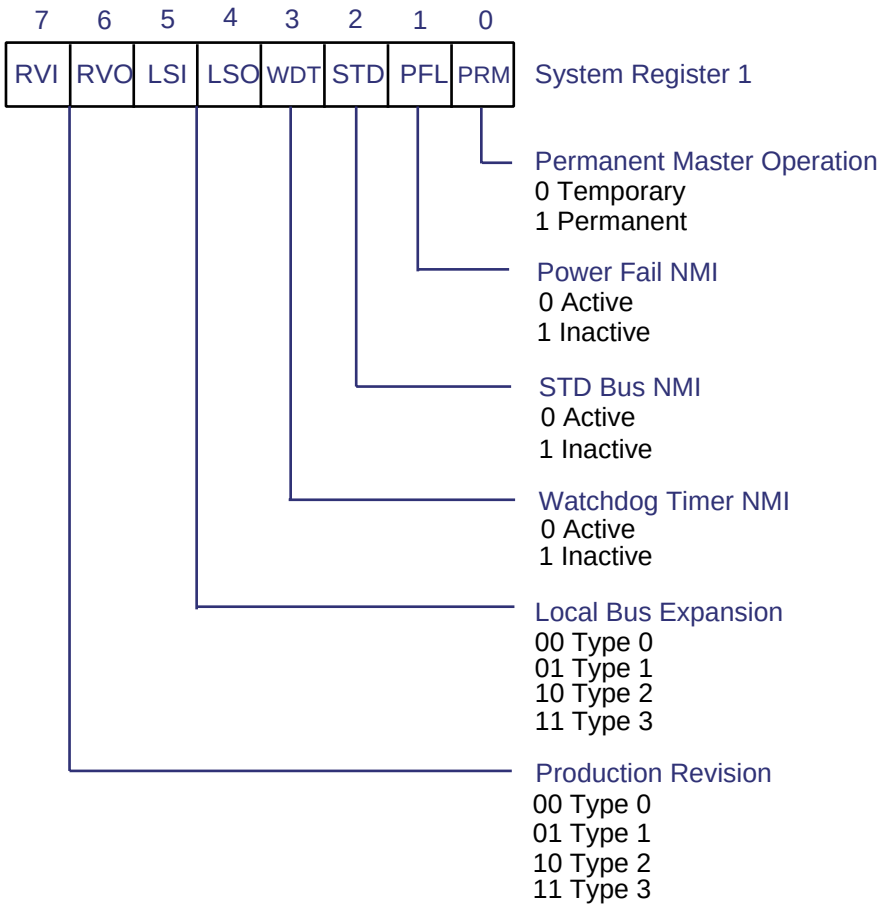
- The reset state for all bits is a logical 0.
- Bits dedicated to input operation must remain programmed with a logical 0 to prevent contention with the input device.
- Bits dedicated to output operation have readback capabilities.

PROGRAMMABLE REGISTERS

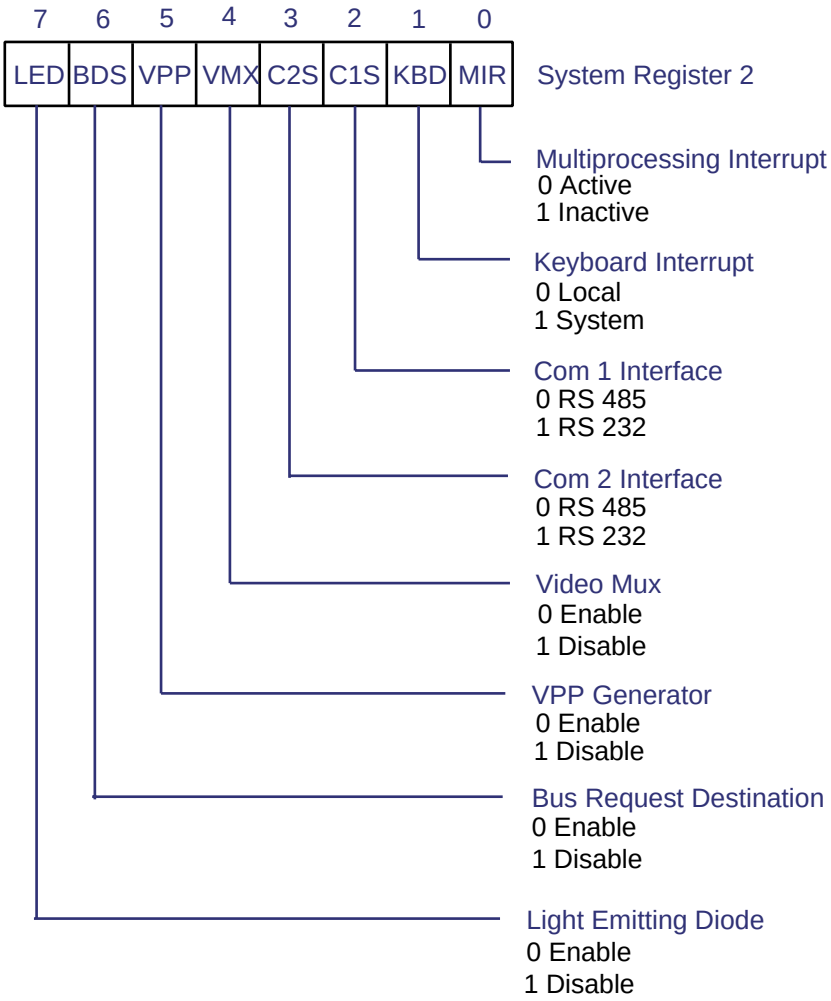
The following illustrate the three System registers.



System Register 0



System Register 1



System Register 2

ADDITIONAL INFORMATION

See Chapter 10, "Parallel I/O," for additional details.

12. WATCHDOG TIMER

The primary function of the watchdog timer is to monitor ZT 8904 operation and take corrective action if the system fails to function as programmed. The major features of the watchdog timer are listed below.

- Single-stage or two-stage operation
- Enabled and disabled through software control
- Armed and strobed through software control

WATCHDOG TIMER OPERATION

The watchdog timer architecture is illustrated in the "Watchdog Timer Architecture" figure. The first stage is implemented in the Intel 386 EX CPU and the second stage is implemented in the Dallas Semiconductor DS1236 system monitor.

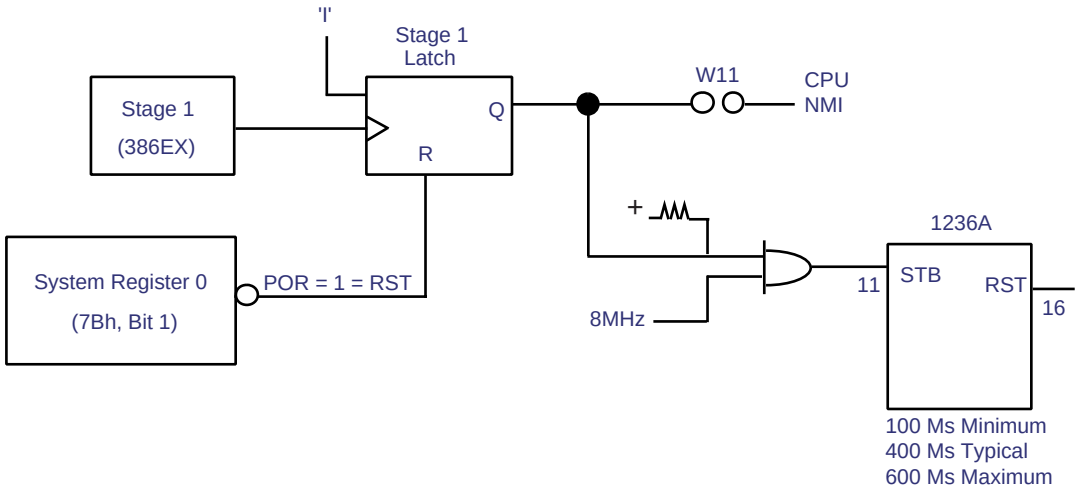
After power on or reset, the output of the first stage latch is a logical one, which enables the 8 MHz signal to strobe the second stage. Also after power on or reset, the first stage begins counting down. After the first stage counts down to zero, a non-maskable interrupt is generated and the second stage begins counting down.

Jumper W11 must be installed to generate a non-maskable interrupt. Bit 1 of System Register 0 (7Bh) must be programmed with a logical one to enable the second stage to begin counting. After the second stage counts down to zero, a reset is generated. If the ZT 8904 is configured as a permanent master, the reset extends to the STD Bus. If the ZT 8904 is configured as a temporary master, the reset remains local.

The CPU watchdog timer must be disabled or periodically programmed with a new count to prevent the first stage from counting to zero. The first stage watchdog timer is based on a 32-bit counter clocked with a 25 MHz clock. The first stage watchdog registers are described in the following topic.

After power on or reset the first stage will count to zero after 2.6 ms (64K clock cycles * 40 ns per clock). The first stage is automatically disabled in idle mode. The first stage is also automatically disabled by the system BIOS in a Ziatech system with DOS.

The non-maskable interrupt service routine must program bit 1 of System Register 0 (7Bh) with a logical zero followed by a logical one to prevent the second stage from counting to zero. The second stage timeout period is fixed at 100 ms minimum and 600 ms maximum. This means that the non-maskable interrupt service routine must strobe the second stage within 100 ms to guarantee that a reset does not occur.



Watchdog Timer Architecture

PROGRAMMABLE REGISTERS

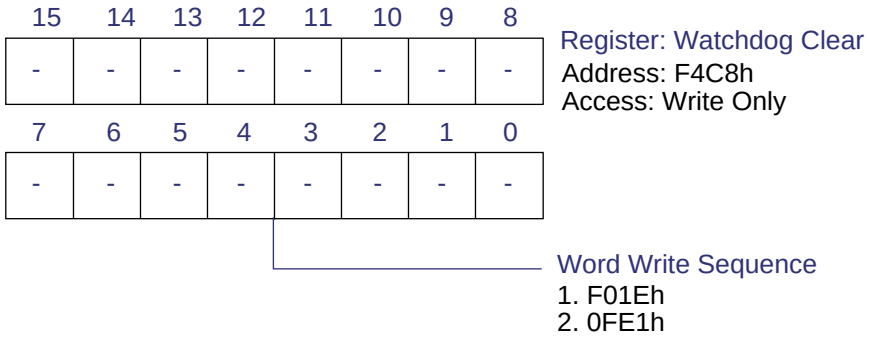
The four register groups associated with the first stage of the watchdog timer are the following:

- Watchdog Timer Clear
- Watchdog Timer Status
- Watchdog Timer Counter
- Watchdog Timer Reload

Watchdog Timer Clear Register

The Watchdog Timer Clear register is programmed with a lockout sequence to enable watchdog timer mode and to reload the counter. The lockout sequence is shown below.

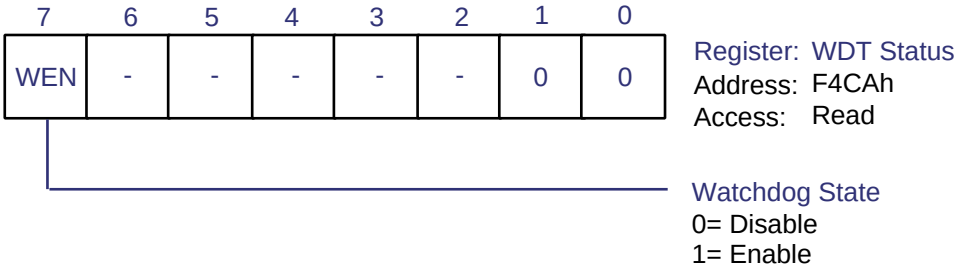
- Word write of F01Eh to F4C8h
- Word write of 0FE1h to F4C8h



Watchdog Timer Clear Register

Watchdog Timer Status Register

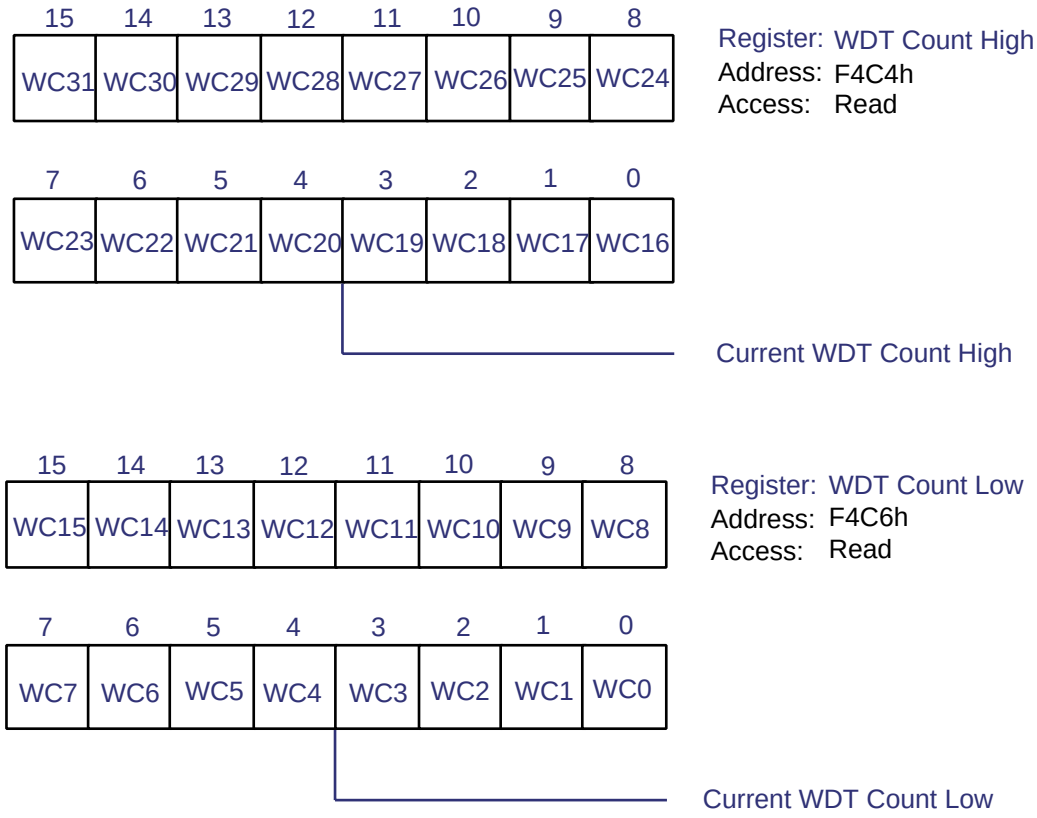
The Watchdog Timer Status register contains a status bit that is automatically set after a lockout sequence to indicate that the watchdog timer is active. The status bit is cleared until the next reset or power cycle.



Watchdog Timer Status Register

Watchdog Timer Counter Registers

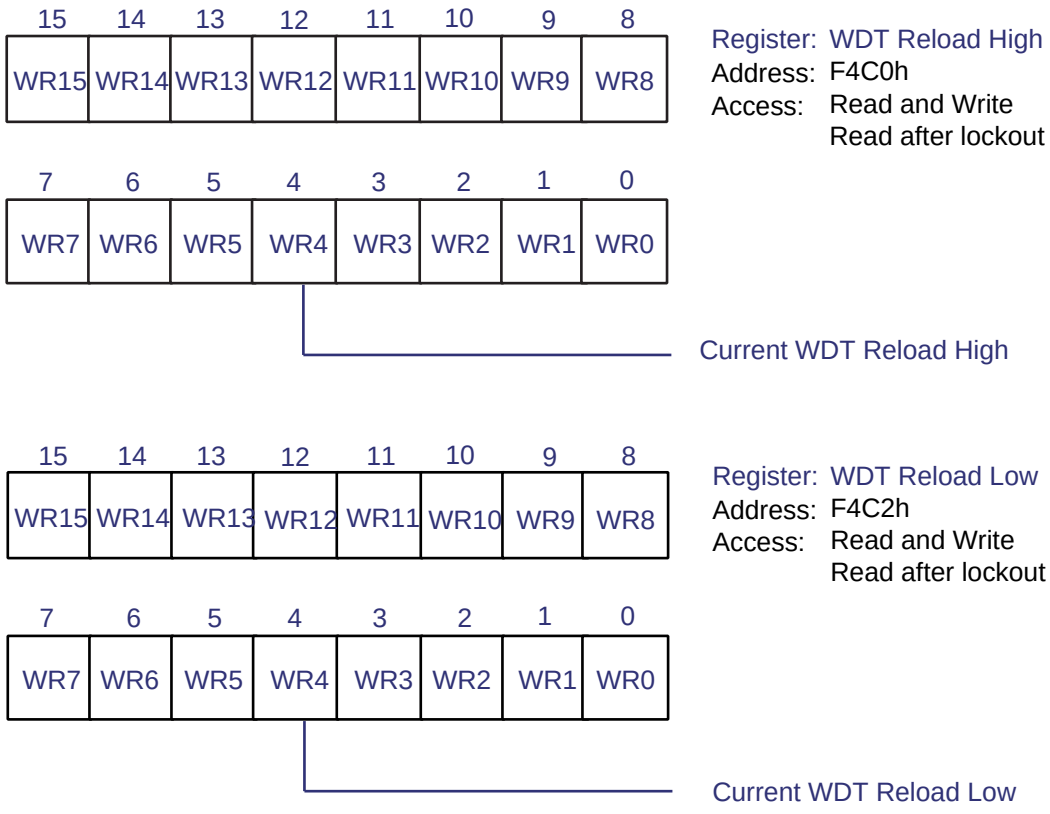
The Watchdog Timer Counter registers hold the current value of the down counter. Application software reads these registers to determine the current count value. A reload operation automatically transfers the contents of the Watchdog Reload registers to the Watchdog Timer registers.



Watchdog Timer Counter Registers

Watchdog Timer Reload Registers

The Watchdog Timer Reload registers are programmed with two word operations to set the reload value. After a lockout sequence, these registers are write protected until after the next reset or power cycle. A reload operation automatically transfers the contents of the Watchdog Reload registers to the Watchdog Timer registers.



Watchdog Timer Reload Registers

ADDITIONAL INFORMATION

Refer to the Intel 386 EX data book for more information on the watchdog timer and the associated operating modes. A product overview of the Intel 386 EX is available on Intel's web site at http://developer.intel.com/design/intarch/prodbref/27270903.htm.

13. LOCAL BUS VIDEO

The ZT 8904 includes a local bus interface to permit high speed peripherals direct access to the CPU bus. This bus operates synchronously at CPU speeds of 25 MHz. Ziatech offers zVID video adapters designed specifically for this local bus interface. These adapters give superior performance over STD bus video solutions by running with four times the data width and more than four times the operating frequency. Major features of the video adapters are listed below. Refer to the zVID manual for installation and operating instructions.

- Up to 300 times the performance of STD bus solutions
- Reduces STD bus traffic by keeping all video operations local
- Combined single-slot occupancy for both the ZT 8904 and zVID
- Flat panel and feature connector support
- Keyboard support
- Resolutions up to 1024 x 768 x 256 colors

14. NUMERIC DATA PROCESSOR

The ZT 8904 includes a socket at location U26 designed to accept an 80387 numeric data processor. The numeric data processor extends the CPU instruction set to include trigonometric, logarithmic, and exponential functions.

Adding a numeric data processor increases the application performance by as much as 10% on Whetstone and Livermore benchmarks. The numeric data processors qualified to work in the ZT 8904 are listed below. Note that neither of these devices meet the extended temperature requirements of the ZT 89CT04.

Manufacturer	**Part Number**
Intel	BOX387SX-33
IIT	387SX-33

To install the 80387, make sure the pin 1 indicator lines up with the pin 1 indicator of the socket. Apply an even downward pressure until the 80387 is completely seated in the socket. Install jumper W8.

15. PROGRAMMABLE LED

The ZT 8904 includes two Light-Emitting Diodes (LEDs) located immediately below the board extractor. The green LED is for the optional IDE disk drive; the red LED is general purpose. The red LED is software programmable through the LED bit in System Register 2. Writing a logical 0 to the LED bit turns the LED off and writing a logical 1 to the LED bit turns the LED on. The LED is turned off after a power cycle or a reset.

The LED bit is in the same register as the multiple master interrupt. The following code demonstrates how to turn the red LED on and off without corrupting the multiple master interrupt.

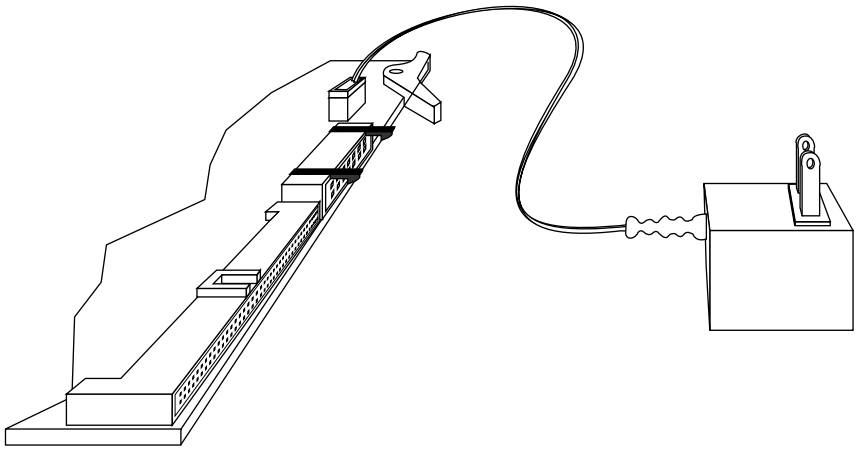
```
;-------------------------------------------------------------
; The multiple master interrupt is a bidirectional
; bit. The current software state of multiple
; master interrupt is maintained in a separate
: multiple master state bit. Input_7d updates the
; multiple master bit with the current software
; state maintained in the multiple master state bit.
;-------------------------------------------------------------
input_7d
          macro
          local     star_int_on
          in   al,7dh
          mov  ah,al
          push dx
          mov  dx,f42eh
          in   al,dx
          pop  dx
          test al,01h
          jnz  star_int_on
           and ah,not 01h
star_int_on:
          mov  al,ah
          endm

;-------------------------------------------------------------
; led_on turns on the led.
;-------------------------------------------------------------
led_on:
          pushf
          cli
          input_7d
          or   al,80h
          out  07dh,al
          popf
          ret
```

```
;---------------------------------------------------------------
; led_off turns off the led.
;---------------------------------------------------------------
led_off:
          pushf
          cli
          input_7d
          and  al,not 80h
          out  07dh,al
          popf
          ret
```

16. AC POWER FAIL

The ZT 8904 supports AC power-fail detection as a means for giving the application advanced warning of an impending power failure. The advanced warning may be used by the application for performing operations such as saving critical data and entering a dormant state.

The ZT 8904 requires a transformer-isolated AC voltage of no more than 30 V from the same source that provides the system power. Ziatech's optional AC wall transformer (ZT 90071) meets these requirements. The wall transformer is connected to the J3 frontplane connector, as shown in the following figure. The pin assignments for connector J3 are given in Appendix B, "Specifications."



AC Wall Transformer Installation

In operation, a non-maskable interrupt is generated when AC power falls below 95 VRMS. The non-maskable interrupt must be enabled through jumper selection (W9). The application software must include a non-maskable interrupt service routine to perform the following:

- Determine if the AC power fail is the source of the interrupt request. The three sources of non-maskable interrupts are AC power fail, STD bus NMIRQ*, and Parity Error.
- Preserve any critical information into Flash memory, either for failure analysis or for system restart.
- Place the CPU in a dormant state using a halt instruction or a looping sequence that is not reading or writing critical data to memory or I/O.

A. JUMPER CONFIGURATIONS

The ZT 8904 includes several options that tailor the operation of the board to requirements of specific applications. Options are made by installing and removing shorting receptacles (jumpers).

JUMPER OPTIONS

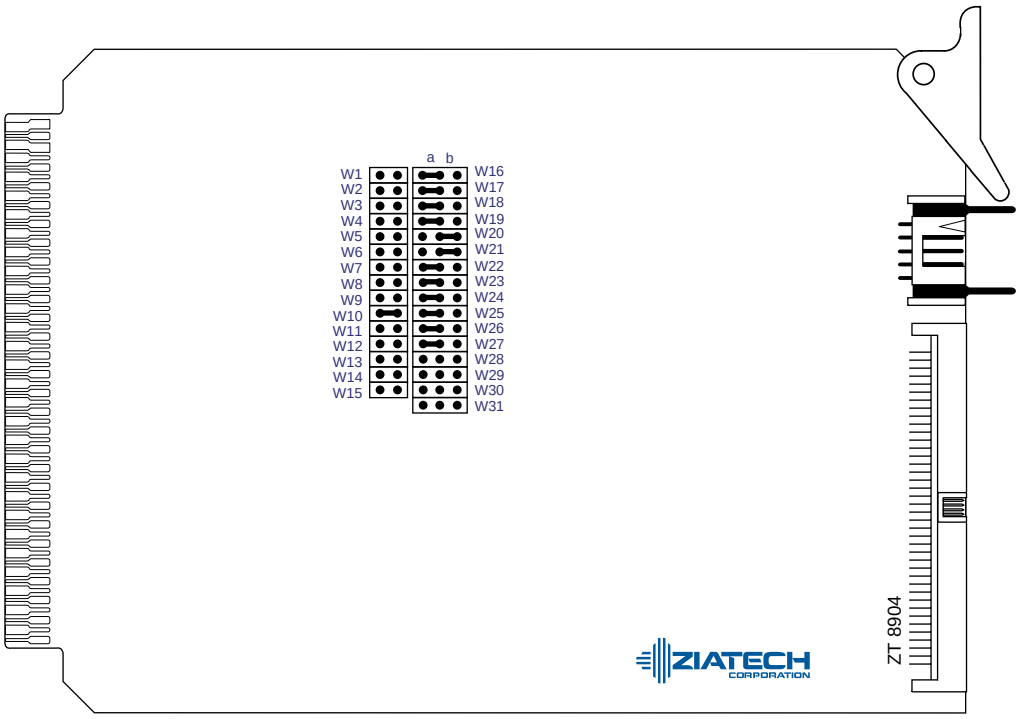
The ZT 8904 includes jumpers with two posts and jumpers with three posts. Jumpers having only two posts are labeled Wx, where x defines the jumper number (for example, W12). Jumpers having three posts are labeled Wx "a" and "b" (for example, W16a and W16b). These jumpers have two possible selections, where "a" is one selection and "b" is another.

Jumper locations are illustrated in the "Customer Jumper Configuration" figure following; use this figure to document your jumper configuration if it differs from the factory default. The "DOS Factory Default Configuration" figure illustrates the factory default jumper configuration for ZT 8904 boards purchased in a DOS system.

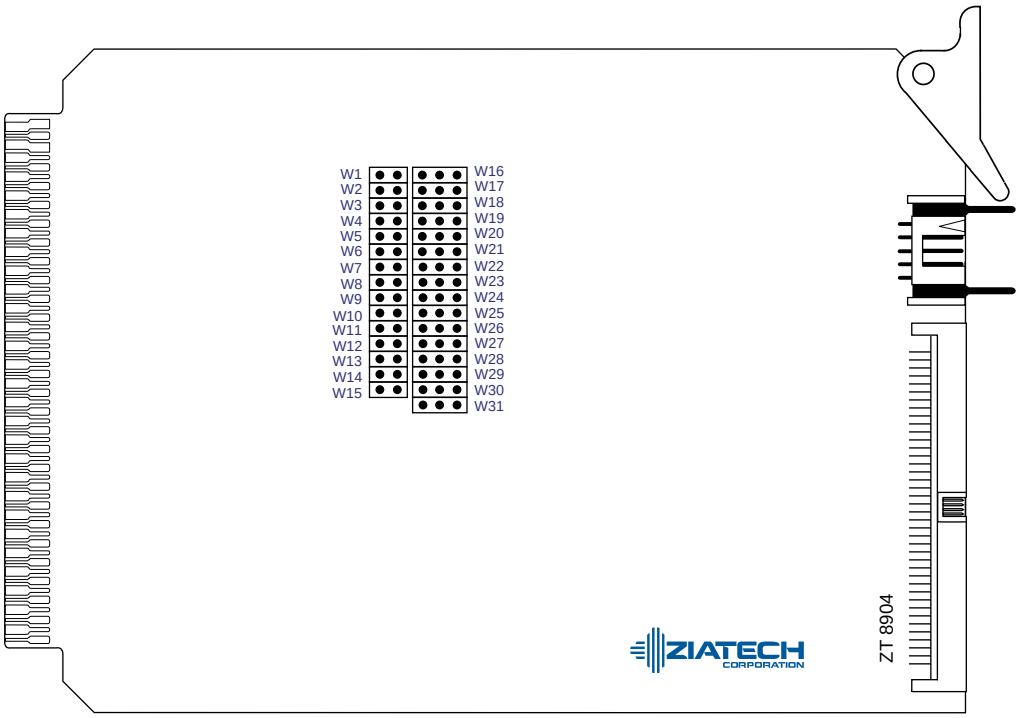
The "Jumper Cross Reference" table below divides the jumper options into functional groups.

Jumper Cross Reference

Function	Jumpers
CMOS RAM	W16
CPU Configuration	W24-27
DRQ1 Source Selection	W23
Maskable Interrupts	W17-22
Non-Maskable Interrupts	W9-11
Numeric Coprocessor	W8
Reserved	W1-7
RS-485 Duplex Selection	W12-15
RS-485 Transmitter Configuration	W28-31



DOS Factory Default Configuration



Customer Jumper Configuration

Jumper Descriptions

The following topics list the jumpers in numerical order and provide a detailed description of each jumper. A dagger (†) indicates the default jumper configuration.

W1-7

Reserved for Ziatech use. Do not install these jumpers.

W8

Numeric Coprocessor - indicates the presence of a numeric coprocessor.

	W8	Numeric Coprocessor
	IN	Installed
†	OUT	Removed

W9-11

Non-Maskable Interrupts - arm the AC power-fail, STD bus, and watchdog timer interrupts for non-maskable interrupt generation. Jumper installation connects the non-maskable interrupt source to the CPU non-maskable interrupt input. System Register 1 provides status to determine which source generated the interrupt when more than one source is enabled.

	W9	AC Power Fail NMI
	IN	Enabled
†	OUT	Disabled
	W10	**STD bus NMIRQ***
†	IN	Enabled
	OUT	Disabled
	W11	**Watchdog timer**
	IN	Enabled
†	OUT	Disabled

† Factory default configuration for DOS systems.

W12-15

RS-485 Duplex Selection - independently selects half duplex or full duplex for each RS-485 channel. The COM1 and COM2 serial ports are software configured for RS-232 or RS-485 operation through System Register 2. If configured for RS-485, the following jumpers adjust the RS-485 architecture to a specific application. These jumpers do not apply to the ZT 8903.

	W12	W13	COM1 Duplex
†	IN	IN	Half duplex (two wire)
	OUT	OUT	Full Duplex (four wire)
	W14	**W15**	**COM2 Duplex**
†	IN	IN	Half Duplex (two wire)
	OUT	OUT	Full Duplex (four wire)

W16

CMOS RAM Erase - removes the contents of the battery-backed CMOS configuration RAM. The CMOS RAM is erased by turning off the power and moving the W16a shorting jumper to position W16b and back to W16a again.

	W16a	W16b	CMOS Configuration RAM
†	IN	OUT	Normal operation
	OUT	IN	Erase

† Factory default configuration for DOS systems.

W17-22

Maskable Interrupts - assigns up to nine interrupt sources to the interrupt controller inputs. Each interrupt input has two possible sources selected by installing a jumper in position "a" or position "b." Other combinations are possible with wire wrap techniques. Interrupt inputs not used in the application must be masked in software.

	Jumper Installed	Interrupt Source	Interrupt
†	W17a	STD bus INTRQ4*	IR5
	W17b	J2 pin 6	IR5
†	W18a	STD bus INTRQ2*	IR6
	W18b	J2 pin 8	IR6
†	W19a	Printer	IR7
	W19b	J2 pin 10	IR7
	W20a	Parallel I/O	IR8
†	W20b	Real Time Clock	IR8
	W21a	Serial COM4	IR9
†	W21b	STD bus INTRQ*	IR9
†	W22a	Serial COM3	IR13
	W22b	Math Coprocessor	IR13

W23

When W26B is installed:

- W23A is reserved.
- W23B connects the 1284 port DMA request to the 386 EX DRQ1.

† Factory default configuration for DOS systems.

W24-27

CPU Configuration - connects external hardware functions to multiplexed CPU pins. The CPU multiplexes DMA channel 0 and DMA channel 1 with serial port COM2 signals. In short, if DMA channel 0 is used to support STD bus DMA (such as the Ziatech ZT 8954 floppy disk controller), Data Carrier Detect and Clear To Send are not available for COM2. If DMA channel 1 is used to support local DMA (such as the 1284 printer port), Transmit Data and Receive Data are not available for COM2. When W24 and W25 are configured for COM2 CTS and CDC, the BIOS setup option for COM2 must be "ONBOARD."

	W24a	W24b	W25a	W25b	CPU Configuration
†	IN	OUT	IN	OUT	DMA channel 0
	OUT	IN	OUT	IN	COM2 CTS and DCD

	W26a	W26b	W27a	W27b	CPU Configuration
†	IN	OUT	IN	OUT	COM2 TXD and RXD
	OUT	IN	OUT	IN	DMA channel 1

† Factory default configuration for DOS systems.

W28-31

RS-485 Transmitter Configuration - independently configures the transmitter input source and transmitter enable for the RS-485 channels. The COM1 and COM2 serial ports are software configured for RS-232 or RS-485 operation through System Register 2. If configured for RS-485, the following jumpers adjust the RS-485 architecture to a specific application. These jumpers do not apply to the ZT 8903.

	W28a	W28b	COM1 Transmit Enable
†	IN	OUT	COM1 DTR
	OUT	IN	COM1 TXD (J1708)
	OUT	OUT	Enabled
	W29a	**W29b**	**COM1 Transmit Input**
†	IN	OUT	COM1 TXD
	OUT	IN	Logical 0 (J1708)
	W30a	**W30b**	**COM2 Transmit Enable**
†	IN	OUT	COM2 DTR
	OUT	IN	COM2 TXD (J1708)
	OUT	OUT	Enabled
	W31a	**W31b**	**COM2 Transmit Input**
†	IN	OUT	COM2 TXD
	OUT	IN	Logical 0 (J1708)

† Factory default configuration for DOS systems.

B. SPECIFICATIONS

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 8904. It also includes illustrations of the board dimensions, the P/E connector pinouts, and cables commonly used with the ZT 8904, as well as tables showing the pin assignments for the ZT 8904's 10 connectors.

ELECTRICAL AND ENVIRONMENTAL SPECIFICATIONS

The following topics list electrical and environmental specifications, including absolute maximum ratings, DC operating characteristics, battery backup characteristics, and STD bus loading characteristics.

Absolute Maximum Ratings

Supply Voltage, Vcc: 0 to 7 V

Supply Voltage, AUX +V: Not used

Supply Voltage, AUX -V: Not used

Storage Temperature: -40° to +85° Celsius

Operating Temperature:

ZT 8903:	0° to +65° Celsius
ZT 8904:	0° to +65° Celsius
ZT 89CT04:	-40° to +85° Celsius

Non-Condensing Relative Humidity: <95% at 40° Celsius

DC Operating Characteristics

DC operating characteristics are specified for boards loaded with 5 Mbytes of RAM and a Math Coprocessor.

Supply Voltage, Vcc: 4.75 to 5.25 V

Supply Voltage, AUX +V: Not used

Supply Voltage, AUX -V: Not used

Supply Current, Icc: 0.8A typ, 1.2A max

Supply Current, AUX +V: Not used

Battery Backup Characteristics

Battery Voltage: 3 V

Battery Capacity: 255 mAH

Real-time clock requirements: 5 µA maximum (when Vcc is below acceptable operating limits)

Real-time clock data retention: 5 years minimum, 10 years typical

Electrochemical Construction: Poly-carbonmonofluoride

STD-80 Compatibility

The ZT 8904 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8904 is not guaranteed to work in all system topologies.

STD Bus Loading Characteristics

The unit load is a convenient method for specifying the input and output drive capability of STD bus cards. With this method, one unit load is equal to one LSTTL load as follows:

- Current for single input load: 20 µA
- Current for single output drive:-400 µA

The unit load reflects current requirements at worst case conditions over the recommended supply voltage and operating temperature ranges. An output drive of 60 unit loads drives 60 STD bus cards having input ratings of one unit load. The table "STD Bus Signal Loading, P Connector" includes load values for STD-80 connections. The "STD Bus Signal Loading, E Connector" table includes load values for STD 32 connections.

STD Bus Signal Loading, P Connector

PIN (CIRCUIT SIDE)							PIN (COMPONENT SIDE)
OUTPUT DRIVE							OUTPUT DRIVE
INPUT LOAD							INPUT LOAD
MNEMONIC							MNEMONIC
+5 VDC	REQ		P2	P1		REQ	+5 VDC
GND	REQ		P4	P3		REQ	GND
DCPDN*		40	P6	P5	55	1	VBAT (INTRQ4)
D7/A13 [1]	1	55	P8	P7	55	1	D3/A19 [1]
D6/A22 [1]	1	55	P10	P9	55	1	D2/A18 [1]
D5/A21 [1]	1	55	P12	P11	55	1	D1/A17 [1]
D4/A20 [1]	1	55	P14	P13	55	1	D0/A16 [1]
A15		55	P16	P15	55		A7
A14		55	P18	P17	55		A6
A13		55	P20	P19	55		A5
A12		55	P22	P21	55		A4
A11		55	P24	P23	55		A3
A10		55	P26	P25	55		A2
A9		55	P28	P27	55		A1
A8		55	P30	P29	55		A0
RD*		55	P32	P31	55		WR*
MEMRQ*		55	P34	P33	55		IORQ*
BHE		55	P36	P35	55		IOEXP
ALE*		55	P38	P37		1	INTRQ1*
STATUS 0*		55	P40	P39	55		STATUS 1*
BUSRQ*	1		P42	P41	55		BUSAK*
INTRQ*	1		P44	P43			INTAK*
NMIRQ*	1		P46	P45		1	WAITRQ*
PBRESET*	1		P48	P47	55	1	SYSRESET* [2]
INTRQ2* (CNTRL*)	1		P50	P49	55	1	CLOCK* [2]
PCI [3]			P52	P51			PCO [3]
AUX GND			P54	P53			AUX GND
AUX-V			P56	P55			AUX+V

Notes:

REQ indicates required connection.

[1] High order address bits multiplied over the data bus.

[2] SYSRESET* and CLOCK* are outputs in permanent master configuration and inputs in temporary master configuration.

[3] PCI is connected to PCO.

STD Bus Signal Loading, E Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
LOCK*			E2	E1			GND
XA23			E4	E3			XA19
XA22			E6	E5			XA18
XA21			E8	E7			XA17
XA20			E10	E9			XA16
RSVD			E12	E11			NOWS*
+5 VDC	REQ		E14	E13		REQ	+5 VDC
DREQx*		55	E16	E15		1	DAKx*
GND	REQ		E18	E17		REQ	GND
D31			E20	E19			D27
D30			E22	E21			D26
D29			E24	E23			D25
D28			E26	E25			D24
GND	REQ		E28	E27			D23
D15	1	55	E30	E29			D22
D14	1	55	E32	E31			D21
D13	1	55	E34	E33			D20
D12	1	55	E36	E35		REQ	GND
D11	1	55	E38	E37			D19
D10	1	55	E40	E39			D18
D9			E42	E41			D17
D8			E44	E43			D16
MASTER16*			E46	E45		REQ	GND
AENx*			E48	E47			IRQx
BE3*			E50	E49			BE1*
BE2*			E52	E51			BE0*
GND	REQ		E54	E53		1	MEM16*
W-R			E56	E55			M-IO
DMAIOR*		55	E58	E57	55		DMAIOW*
EX8*			E60	E59		1	IO16*
START*			E62	E61			CMD*
EX32*			E64	E63			EX16*
T-C		55	E66	E65			EXRDY
+5 VDC	REQ		E68	E67		1	INTRQ3*
MREQx*			E70	E69			MAKx*
MSBURST*			E72	E71			SLBURST*
XA31*			E74	E73			XA27*
XA30*			E76	E75			XA26*
XA29*			E78	E77			XA25*
XA28*			E80	E79			XA24*

MECHANICAL SPECIFICATIONS

The following topics list mechanical specifications, including card dimensions and weight, connectors, and cables.

Card Dimensions and Weight

The ZT 8904 meets the *STD-80 Series Bus Specification* for all mechanical parameters. In a card cage with 0.625 inch spacing, the ZT 8904 requires one card slot with or without the zVID local bus video adapter installed. Mechanical dimensions are shown in the "Board Dimensions" figure following and are outlined below.

Board Length: 16.51 ± 0.063 cm (6.500 ± 0.025 inches)

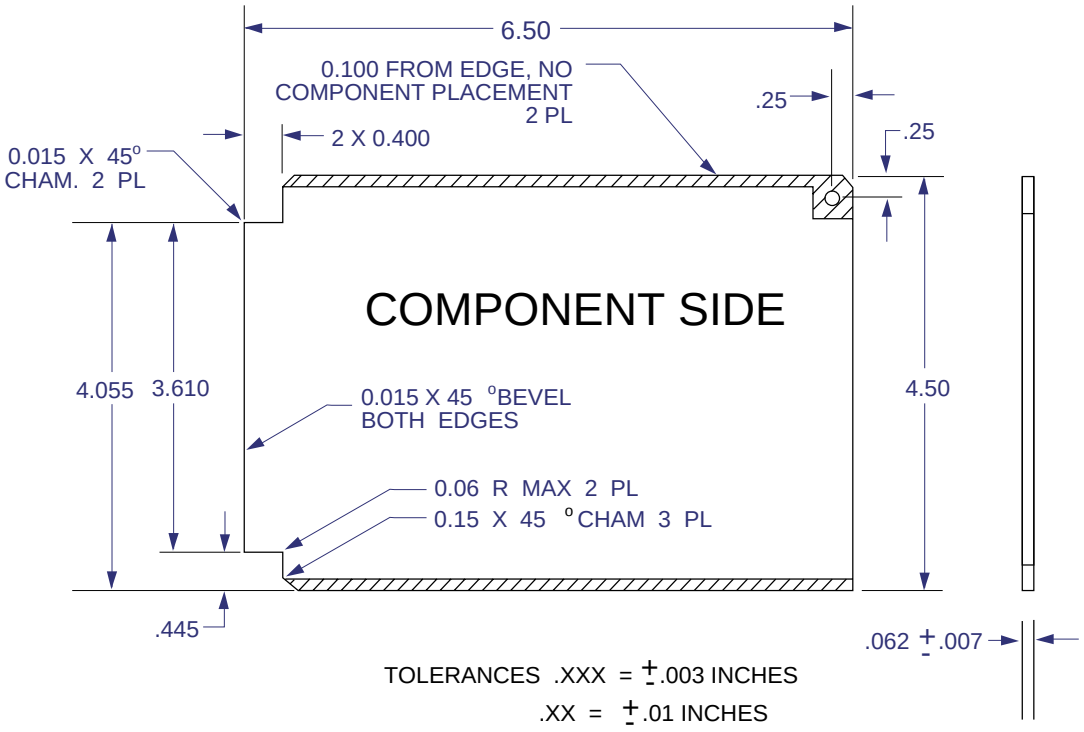
Board Width: 11.43 ± 0.038 cm (4.500 ± 0.015 inches)

Board Thickness: 0.158 ± 0.013 cm (0.062 ± 0.005 inches)

Board Weight: 200 grams (7 ounces)

Board Height From Top Surface: 1.27 cm (0.5 inches)

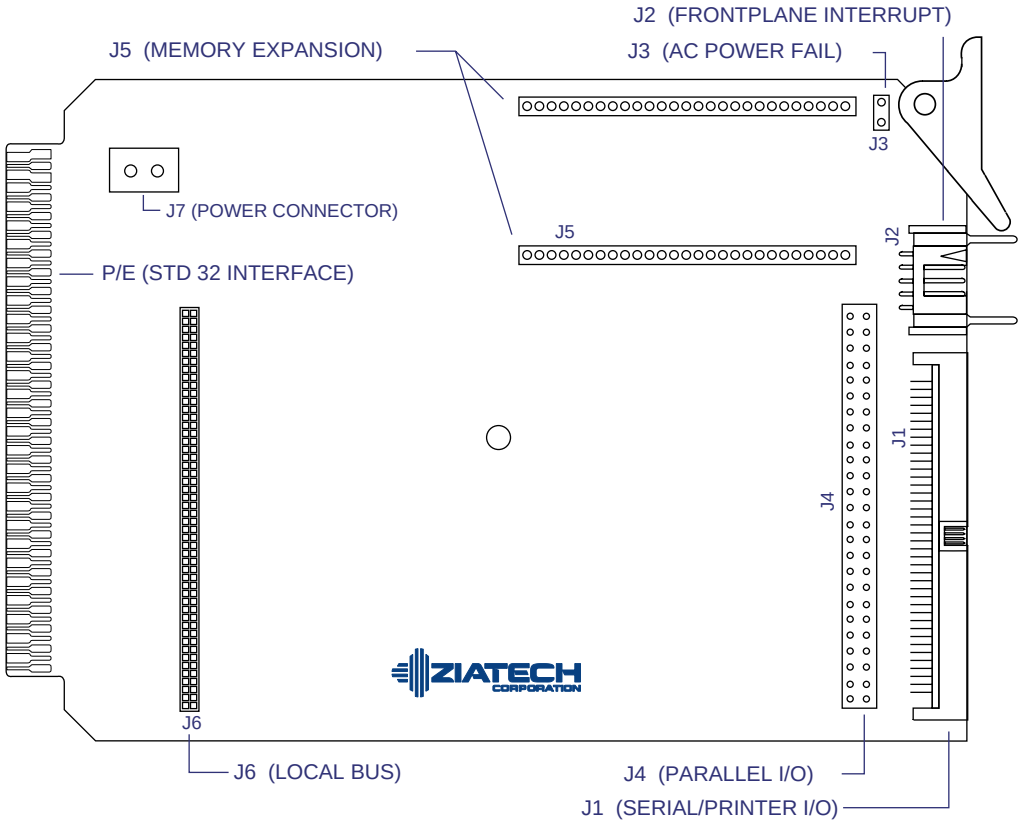
Board Height From Bottom Surface without optional IDE: 0.18 cm (0.06 inches)



Board Dimensions

Connectors

The ZT 8904 includes 9 connectors to interface to the STD bus and application specific devices. Connector positions are illustrated in the "Connector Locations" figure below. A description and pin map for each connector is given in the following topics.



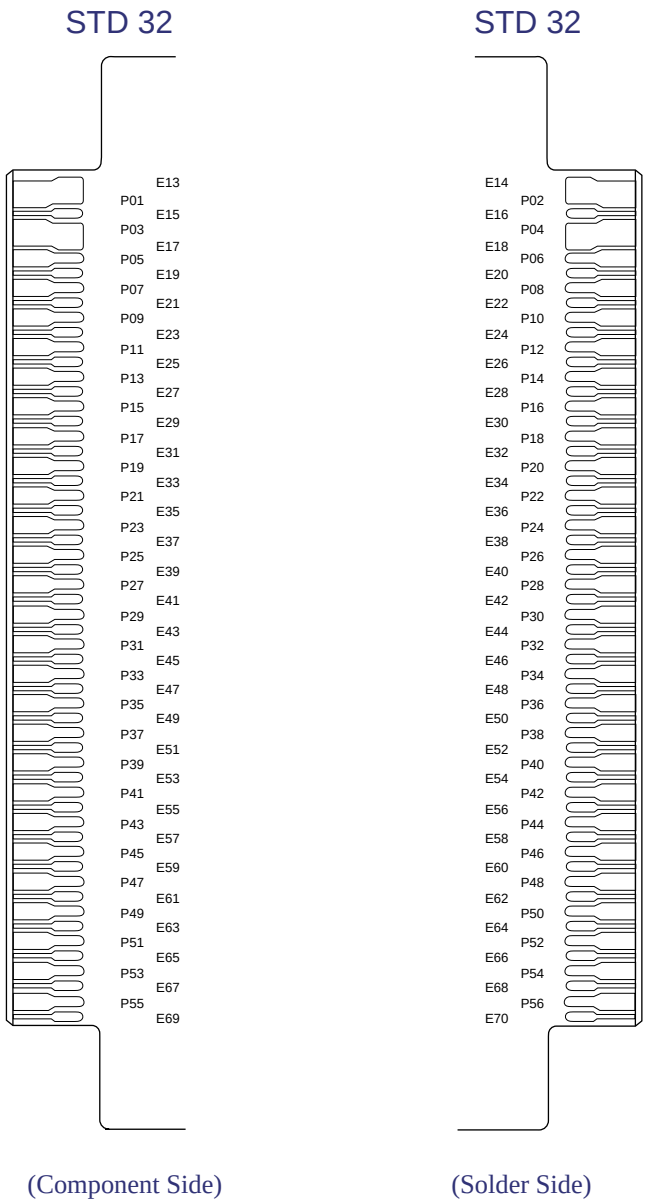
Connector Locations

STD 32 P/E Connector

P: The P connector is the interface between the ZT 8904 and the STD-80 bus. This connector is a 56-pin (dual 28-pin) card-edge connector with fingers on 0.125 inch contact spacing. The mating connector is a Viking 3VH28/1CNK5 or equivalent for the solder tail, or a Viking 3VH28/1CND5 or equivalent for a three-level wire wrap. The "P/E Connector Pinout" figure shows pin assignments for the P connector and the "STD Bus Signal Loading, P Connector" table shows signal assignments.

E: The E connector extends the P connector to interface the ZT 8904 to the STD 32 bus. This connector combines with the P connector to make a 114-pin (dual 57-pin) card-edge connector with fingers on 0.0625 inch contact spacing. The mating connector is a Viking S3VT68/5DP12 or equivalent for the solder tail, or a

Viking S3VT68/5DE12 or equivalent for the card extender. The figure below, "P/E Connector Pinout," shows pin assignments for the E connector and the table "STD Bus Signal Loading, E Connector" shows signal assignments.



P/E Connector Pinout

Connector Descriptions

Connector	Function
J1	Peripheral
J2	Frontplane Interrupt
J3	AC Power Fail
J4	Parallel I/O
J5	Memory Expansion
J6	Local Bus
J7	Auxiliary Power
J8	Optional IDE
J9	Reserved

J1 (Peripheral)

J1 is a latching 80-pin (dual 40-pin) male transition connector with 0.05 inch contact spacing. The serial ports, 1284 parallel port, and an external battery connection are available through J1. The pin assignments are given in the "J1 Peripheral Pinout" table following. The pin assignments enable standard D-shell termination for the serial and 1284 parallel ports. The mating connector is an AMP 104892-8 or equivalent.

J1 Peripheral Pinout

Pin	Signal	Type	Description	Pin	Signal	Type	Description
1	COM4 DCD	In	Data Carrier Detect	41	AUX BAT	In	Auxiliary Battery
2	COM4 DSR	In	Data Set Ready	42	GND	Out	Ground
3	COM4 RXD	In	Receive Data	43	RSV	------	Reserved
4	COM4 RTS	Out	Request To Send	44	RSV	------	Reserved
5	COM4 TXD	Out	Transmit Data	45	RSV	------	Reserved
6	COM4 CTS	In	Clear To Send	46	RSV	------	Reserved
7	COM4 DTR	Out	Data Terminal Ready	47	/STB	Out	Strobe
8	COM4 RIN	In	Ring Indicator	48	/AFD	Out	Autofeed
9	GND	------	Ground	49	PD0	In/Out	Data 0
10	VCC	Out	+5V	50	/ERR	In	Error
11	COM3 DCD	In	Data Carrier Detect	51	PD1	In/Out	Data 1
12	COM3 DSR	In	Data Set Ready	52	/INIT	Out	Initialize

J1 Peripheral Pinout (continued)

Pin	Signal	Type	Description	Pin	Signal	Type	Description
13	COM3 RXD	In	Receive Data	53	PD2	In/Out	Data 2
14	COM3 RTS	Out	Request To Send	54	/SLIN	Out	Select To Printer
15	COM3 TXD	Out	Transmit Data	55	PD3	In/Out	Data 3
16	COM3 CTS	In	Clear To Send	56	GND	------	Ground
17	COM3 DTR	Out	Data Terminal Ready	57	PD4	In/Out	Data 4
18	COM3 RIN	In	Ring Indicator	58	GND	------	Ground
19	GND	------	Ground	59	PD5	In/Out	Data 5
20	VCC	Out	+5V	60	GND	------	Ground
21	COM2 DCD	In	Data Carrier Detect	61	PD6	In/Out	Data 6
22	COM2 DSR	In	Data Set Ready	62	GND	------	Ground
23	COM2 RXD	In	Receive Data	63	PD7	In/Out	Data 7
24	COM2 RTS	Out	Request To Send	64	GND	------	Ground
25	COM2 TXD	Out	Transmit Data	65	/ACK	In	Acknowledge
26	COM2 CTS	In	Clear To Send	66	GND	------	Ground
27	COM2 DTR	Out	Data Terminal Ready	67	BUSY	In	Busy
28	COM2 RIN	In	Ring Indicator	68	GND	------	Ground
29	GND	------	Ground	69	PE	In	Paper Error
30	VCC	Out	Power	70	GND	------	Ground
31	COM1 DCD	In	Data Carrier Detect	71	SLCT	In	Select From Printer
32	COM1 DSR	In	Data Set Ready	72	TXDA+	Out	COM1 Transmit Data +
33	COM1 RXD	In	Receive Data	73	TXDA-	Out	COM1 Transmit Data -
34	COM1 RTS	Out	Request To Send	74	RXDA+	In	COM1 Receive Data +
35	COM1 TXD	Out	Transmit Data	75	RXDA-	In	COM1 Receive Data -
36	COM1 CTS	In	Clear To Send	76	GND	------	Ground
37	COM1 DTR	Out	Data Terminal Ready	77	TXDB+	Out	COM2 Transmit Data +
38	COM1 RIN	In	Ring Indicator	78	TXDB-	Out	COM2 Transmit Data -
39	GND	------	Ground	79	RXDB+	In	COM2 Receive Data +
40	VCC	Out	Power	80	RXDB-	In	COM2 Receive Data -

J2 (Frontplane Interrupt)

J2 is a latching 10-pin (dual 5-pin) male transition connector with 0.1 inch contact spacing. Frontplane interrupts are available through this connector. The pin assignments are given in the “J2 Frontplane Interrupt Pinout” table below. The mating connector is a T&B Ansley #622-1030 or equivalent.

J2 Frontplane Interrupt Pinout

Pin #	Signal	Type	Description
1	GND	------	Ground
2	NC	In	Not connected
3	GND	------	Ground
4	NC	In	Not connected
5	GND	------	Ground
6	FP5*	In	Interrupt level 5
7	GND	------	Ground
8	FP6*	In	Interrupt level 6
9	GND	------	Ground
10	FP7*	In	Interrupt level 7

Notes:

1. The interrupt levels shown are the most common configuration. Refer to the "Interrupt Architecture" figure in Chapter 4, "Interrupt Controller," for other possibilities.

2. The frontplane interrupts are active low inputs that are routed through an inverter before being applied to the interrupt controller.

J3 (AC Power Fail)

J3 is a latching 2-pin male low-profile header with 0.1 inch contact spacing. The AC input signals for the optional power-fail detection feature are available through this connector. The pin assignments are given in the “J3 AC Power Fail Pinout” table following. The mating connector is a Molex 39-01-0023 or equivalent. The mating connector also requires two Molex 39-01-0031 terminals or equivalent.

J3 AC Power Fail Pinout

Pin #	Signal	Type	Description
1	AC1	In	AC power
2	AC2	In	AC power

J4 (Parallel I/O)

J4 is a 50-pin (dual 25-pin) vertical male header with 0.1 inch contact spacing. The 24 general purpose parallel I/O signals are included in this connector. The pin assignments are given in the “J4 Parallel I/O Pinout” table following. The pin assignments are chosen for direct connection to an I/O module mounting rack, such as those offered by Ziatech and Opto 22. The mating connector is a T&B Ansley #622-5030 or equivalent.

J4 Parallel I/O Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	MOD23	In/Out	Port 7A, bit 7	26	GND	------	Ground
2	GND	------	Ground	27	MOD10	In/Out	Port 79, bit 2
3	MOD22	In/Out	Port 7A, bit 6	28	GND	------	Ground
4	GND	------	Ground	29	MOD09	In/Out	Port 79, bit 1
5	MOD21	In/Out	Port 7A, bit 5	30	GND	------	Ground
6	GND	------	Ground	31	MOD08	In/Out	Port 79, bit 0
7	MOD20	In/Out	Port 7A, bit 4	32	GND	------	Ground
8	GND	------	Ground	33	MOD07	In/Out	Port 78, bit 7
9	MOD19	In/Out	Port 7A, bit 3	34	GND	------	Ground
10	GND	------	Ground	35	MOD06	In/Out	Port 78, bit 6
11	MOD18	In/Out	Port 7A, bit 2	36	GND	------	Ground
12	GND	------	Ground	37	MOD05	In/Out	Port 78, bit 5
13	MOD17	In/Out	Port 7A, bit 1	38	GND	------	Ground
14	GND	------	Ground	39	MOD04	In/Out	Port 78, bit 4
15	MOD16	In/Out	Port 7A, bit 0	40	GND	------	Ground
16	GND	------	Ground	41	MOD03	In/Out	Port 78, bit 3
17	MOD15	In/Out	Port 79, bit 7	42	GND	------	Ground
18	GND	------	Ground	43	MOD02	In/Out	Port 78, bit 2
19	MOD14	In/Out	Port 79, bit 6	44	GND	------	Ground
20	GND	------	Ground	45	MOD01	In/Out	Port 78, bit 1
21	MOD13	In/Out	Port 79, bit 5	46	GND	------	Ground
22	GND	------	Ground	47	MOD00	In/Out	Port 78, bit 0
23	MOD12	In/Out	Port 79, bit 4	48	GND	------	Ground
24	GND	------	Ground	49	VCC	------	+5 Volts
25	MOD11	In/Out	Port 79, bit 3	50	GND	------	Ground

J5 (Memory Expansion)

J5 is a 54-pin (dual 27-pin) socket with 0.1 inch contact spacing. J5 includes memory address, data, and control signals for supporting RAM memory expansion and Flash boot modules. The pin assignments are given in the "J5 Memory Expansion Pinout" table below. The mating modules are the Ziatech ZT 96047 for an additional 4 Mbytes of RAM and the Ziatech ZT 95190 for a flash boot module.

J5 Memory Expansion Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	A1	Out	CPU Address	28	/RD	Out	Read enable
2	A2	Out	CPU Address	29	/MCS	Out	Module select
3	A3	Out	CPU Address	30	/CE4	Out	Chip select 4
4	A4	Out	CPU Address	31	/CE5	Out	Chip select 5
5	A5	Out	CPU Address	32	/CE6	Out	Chip select 6
6	A6	Out	CPU Address	33	/CE7	Out	Chip select 7
7	A7	Out	CPU Address	34	/WE	Out	Write strobe
8	A8	Out	CPU Address	35	/OE	Out	Output enable
9	A9	Out	CPU Address	36	RSV	------	Reserved
10	A10	Out	CPU Address	37	D15	In/Out	Data 15
11	A11	Out	CPU Address	38	D14	In/Out	Data 14
12	GND	------	Ground	39	D13	In/Out	Data 13
13	VCC	------	+5 Volts	40	D12	In/Out	Data 12
14	A12	Out	CPU Address	41	D11	In/Out	Data 11
15	A13	Out	CPU Address	42	VCC	------	+5 Volts
16	A14	Out	CPU Address	43	GND	------	Ground
17	A15	Out	CPU Address	44	D10	In/Out	Data 10
18	A16	Out	CPU Address	45	D9	In/Out	Data 9
19	A17	Out	CPU Address	46	D8	In/Out	Data 8
20	A18	Out	CPU Address	47	D7	In/Out	Data 7
21	A19	Out	CPU Address	48	D6	In/Out	Data 6
22	/CE0	Out	Chip select 0	49	D5	In/Out	Data 5
23	/CE1	Out	Chip select 1	50	D4	In/Out	Data 4
24	/CE2	Out	Chip select 2	51	D3	In/Out	Data 3
25	/CE3	Out	Chip select 3	52	D2	In/Out	Data 2
26	/BLE	Out	Byte Low Enable	53	D1	In/Out	Data 1
27	/MPR	Out	Module present	54	D0	In/Out	Data 0

J6 (Local Bus)

J6 is a 100-pin (dual 50-pin) vertical receptacle with 0.05 inch contact spacing. This connector includes the signals needed for a local bus interface. This interface is used by optional piggyback adapters, such as the Ziatech zVID video adapters. The pin assignments are given in the “J6 Local Bus Video Pinout” table below. The mating connector is an AMP 1-104655-1 (0.250 inch mated height), 1-10456-0 (0.320 inch mated height), or 1-104693-0 (0.0390 inch mated height).

J6 Local Bus Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	VCC	------	+5 Volts	51	D12	In/Out	CPU Data
2	VCC	------	+5 Volts	52	D13	In/Out	CPU Data
3	A02	Out	CPU Address	53	D14	In/Out	CPU Data
4	GND	------	Ground	54	D15	In/Out	CPU Data
5	A04	Out	CPU Address	55	D16	In/Out	CPU Data
6	A03	Out	CPU Address	56	D17	In/Out	CPU Data
7	A06	Out	CPU Address	57	D18	In/Out	CPU Data
8	A05	Out	CPU Address	58	VCC	------	+5 Volts
9	A08	Out	CPU Address	59	D20	In/Out	CPU Data
10	A07	Out	CPU Address	60	D19	In/Out	CPU Data
11	GND	------	Ground	61	D22	In/Out	CPU Data
12	A09	Out	CPU Address	62	D21	In/Out	CPU Data
13	A10	Out	CPU Address	63	D24	In/Out	CPU Data
14	A11	Out	CPU Address	64	D23	In/Out	CPU Data
15	A12	Out	CPU Address	65	GND	------	Ground
16	A13	Out	CPU Address	66	D25	In/Out	CPU Data
17	A14	Out	CPU Address	67	D26	In/Out	CPU Data
18	A15	Out	CPU Address	68	D27	In/Out	CPU Data
19	A16	Out	CPU Address	69	D28	In/Out	CPU Data
20	A17	Out	CPU Address	70	D29	In/Out	CPU Data
21	A18	Out	CPU Address	71	D30	In/Out	CPU Data
22	GND	------	Ground	72	D31	In/Out	CPU Data
23	A20	Out	CPU Address	73	/BE0	Out	Byte Enable

J6 Local Bus Pinout (continued)

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
24	A19	Out	CPU Address	74	GND	------	Ground
25	A22	Out	CPU Address	75	/BE1	Out	Byte Enable
26	A21	Out	CPU Address	76	/SLCT	In	Module Select
27	A24	Out	CPU Address	77	/BE2	Out	Byte Enable
28	A23	Out	CPU Address	78	/PRES	In	Module Present
29	VCC	------	+5 Volts	79	/BE3	Out	Byte Enable
30	A25	Out	CPU Address	80	/RDY	In	Ready
31	A26	Out	CPU Address	81	GND	------	Ground
32	A27	Out	CPU Address	82	/BRDY	In	Burst Ready
33	A28	Out	CPU Address	83	ADS	Out	Address Status
34	A29	Out	CPU Address	84	/BLAST	Out	Burst Last
35	A30	Out	CPU Address	85	M/I	Out	Memory/I/O
36	A31	Out	CPU Address	86	/LBA	In	Local Bus Ack.
37	D00	In/Out	CPU Data	87	W/R	Out	Write/Read
38	GND	------	Ground	88	/KEN	Out	Cache Enable
39	D02	In/Out	CPU Data	89	D/C	Out	Data/Control
40	D01	In/Out	CPU Data	90	/VIDEN	Out	Video Enable
41	D04	In/Out	CPU Data	91	RESET	Out	CPU Reset
42	D03	In/Out	CPU Data	92	KBD	Out	Keyboard Data
43	D06	In/Out	CPU Data	93	RSVD	------	Reserved
44	D05	In/Out	CPU Data	94	KBC	Out	Keyboard Clock
45	D08	In/Out	CPU Data	95	GND	------	Ground
46	D07	In/Out	CPU Data	96	GND	------	Ground
47	GND	------	Ground	97	CLK14	Out	14.318 MHz Clock
48	D09	In/Out	CPU Data	98	CLK	Out	CPU Clock
49	D10	In/Out	CPU Data	99	VCC	------	+5 Volts
50	D11	In/Out	CPU Data	100	VCC	------	+5 Volts

J7 (Auxiliary Power)

J7 is a location for a 2-pin latching COMBICON connector with 0.2 inch contact spacing. J7 includes the power and ground connections needed to power the ZT 8904 when the STD bus connection is not used. The pin assignments are given in the following table, "J7 Auxiliary Power Pinout." The multiple-source board mount connectors and associated mating connectors are shown below.

Board Connector	Mating Connector
Augat 5EHDV-02	Augat 5ESDV-02
Phoenix Contact MSTBVA2.5/2-G	Phoenix Contact MVSTBR2.5/2-ST
Riacon 31020102	Riacon 31049102

J7 Auxiliary Power Pinout

Pin #	Signal	Type	Description
1	VCC	In	+5 Volts
2	GND	In	Ground

J8 (Optional IDE)

J8 is an optional 44-pin (dual 22-pin) vertical receptacle with 2 mm contact spacing. An IDE interface is provided through this connector. The pin assignments are given in the "J8 Optional IDE Pinout" table below. The board connector is a SAMTEC STMM-122-01-S-D-SM or equivalent.

J8 Optional IDE Pinout

Pin#	Signal	Type	Description	Pin#	Signal	Type	Description
1	/RST1	Out	Reset	23	/IOW	Out	I/O Write
2	GND	------	Ground	24	GND	------	Ground
3	D7	In/Out	Latched Data	25	/IOR	Out	I/O Read
4	D8	In/Out	Latched Data	26	GND	------	Ground
5	D6	In/Out	Latched Data	27	RSVD	------	Reserved
6	D9	In/Out	Latched Data	28	ALE	Out	Address Latch
7	D5	In/Out	Latched Data	29	RSVD	------	Reserved
8	D10	In/Out	Latched Data	30	GND	------	Ground
9	D4	In/Out	Latched Data	31	IRQ	In	Interrupt
10	D11	In/Out	Latched Data	32	/IOCS16	In	16 Bit I/O Access
11	D3	In/Out	Latched Data	33	ADDR1	Out	Address Bit 1
12	D12	In/Out	Latched Data	34	NC	------	Not connected
13	D2	In/Out	Latched Data	35	ADDR0	Out	Address bit 0
14	D13	In/Out	Latched Data	36	ADDR2	Out	Address bit 2
15	D1	In/Out	Latched Data	37	/CS0	Out	Chip Select 0
16	D14	In/Out	Latched Data	38	/CS1	Out	Chip Select 1
17	D0	In/Out	Latched Data	39	/ACT	Out	Activity LED
18	D15	In/Out	Latched Data	40	GND	------	Ground
19	GND	------	Ground	41	VCC	------	+5 Volts
20	KEY	------	Not Connected	42	VCC	------	+5 Volts
21	RSVD	------	Reserved	43	GND	------	Ground
22	GND	------	Ground	44	XT/AT	Out	Interface Type

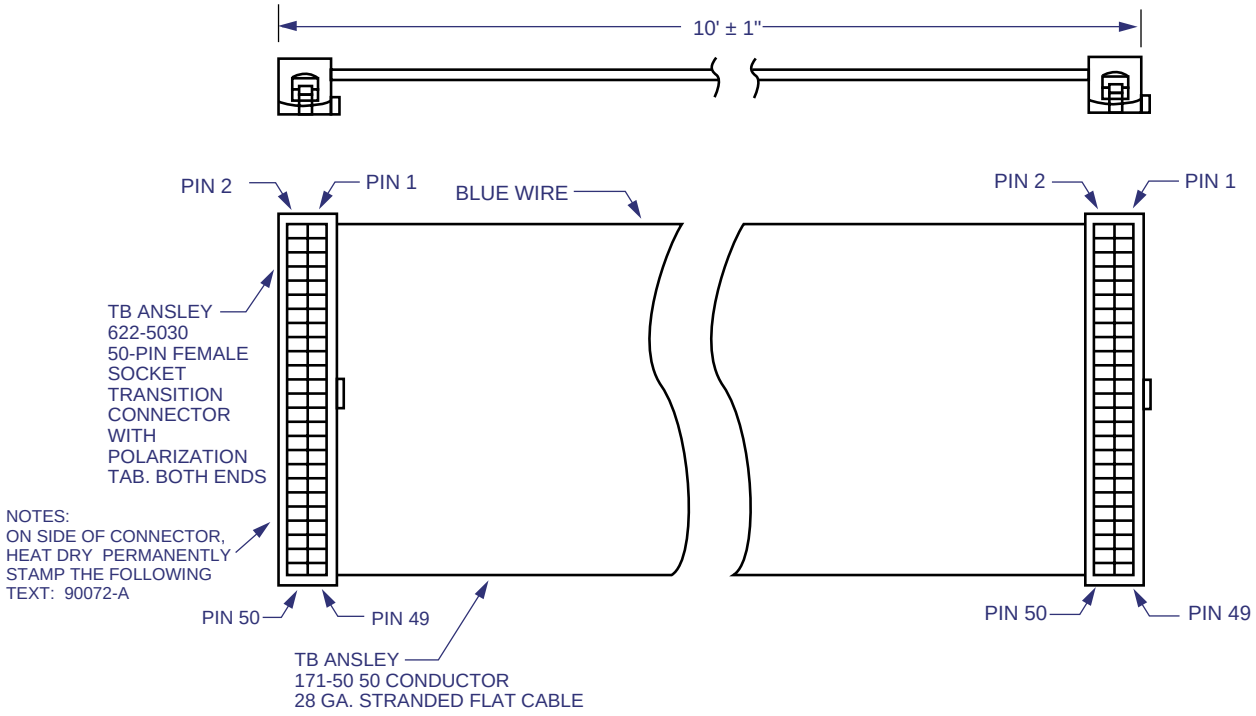
J9 (Reserved)

J9 is reserved for Ziatech test purposes.

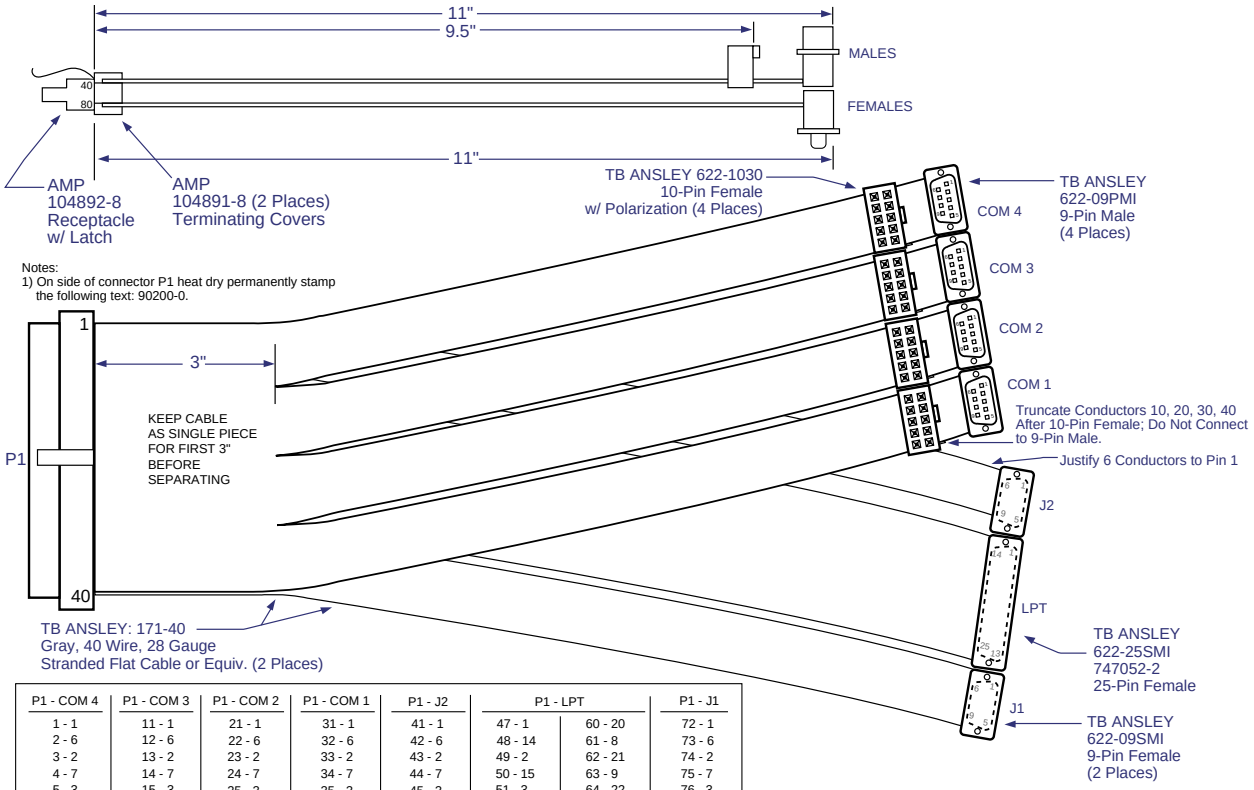
Cables

The following cables are available from Ziatech Corporation. They are included here for those who wish to make their own cables:

- ZT 90072 Digital I/O Cable
- ZT 90166 zVID2 Panel Mount Video and Keyboard Cable
- ZT 90167 zVID2 Desktop Video and Keyboard Cable
- ZT 90168 Multiple zVID2
- ZT 90200 Quad Serial and Printer Cable for ZT 8904 and ZT 89CT04
- ZT 90203 Dual Serial and Printer Cable for the ZT 8903



ZT 90072 Digital I/O Cable

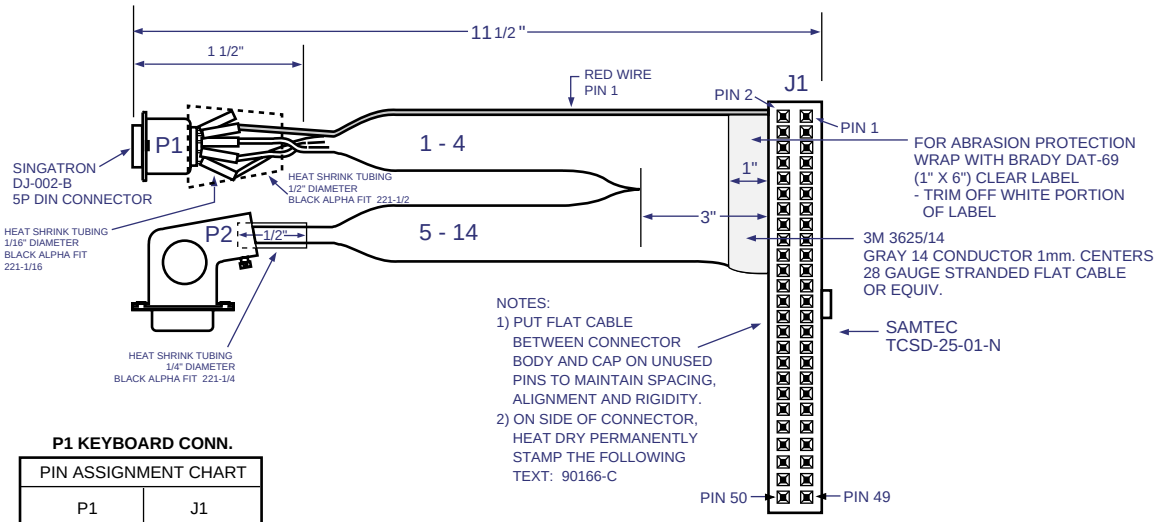


P1 - COM 4	P1 - COM 3	P1 - COM 2	P1 - COM 1	P1 - J2	P1 - LPT		P1 - J1
1 - 1	11 - 1	21 - 1	31 - 1	41 - 1	47 - 1	60 - 20	72 - 1
2 - 6	12 - 6	22 - 6	32 - 6	42 - 6	48 - 14	61 - 8	73 - 6
3 - 2	13 - 2	23 - 2	33 - 2	43 - 2	49 - 2	62 - 21	74 - 2
4 - 7	14 - 7	24 - 7	34 - 7	44 - 7	50 - 15	63 - 9	75 - 7
5 - 3	15 - 3	25 - 3	35 - 3	45 - 3	51 - 3	64 - 22	76 - 3
6 - 8	16 - 8	26 - 8	36 - 8	46 - 8	52 - 16	65 - 10	77 - 8
7 - 4	17 - 4	27 - 4	37 - 4	NC - 4 [2]	53 - 4	66 - 23	78 - 4
8 - 9	18 - 9	28 - 9	38 - 9	NC - 9 [2]	54 - 17	67 - 11	79 - 9
9 - 5	19 - 5	29 - 5	39 - 5	NC - 5 [2]	55 - 5	68 - 24	80 - 5
10 - NC(+5) [1]	20 - NC(+5) [1]	30 - NC(+5) [1]	40 - NC(+5) [1]		56 - 18	69 - 12	
					57 - 6	70 - 25	
					58 - 19	71 - 13	
					59 - 7		

[1] *Connect to 10-Pin Female for +5V, no connection to 9-Pin Male (COM1-4)*

[2] *Justify 6 Conductors toward Pin 1.*

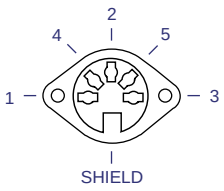
ZT 90200 Quad Serial and Printer Cable For ZT 8904 and ZT 89CT04



P1 KEYBOARD CONN.

PIN ASSIGNMENT CHART	
P1	J1
1	2
2	4
3	-
4	3
5	1
SHIELD	-

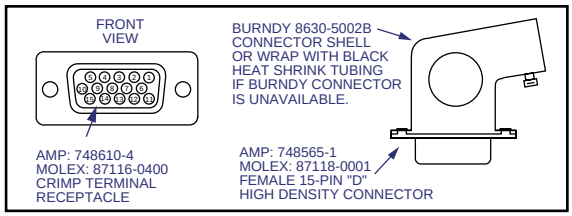
FRONT VIEW



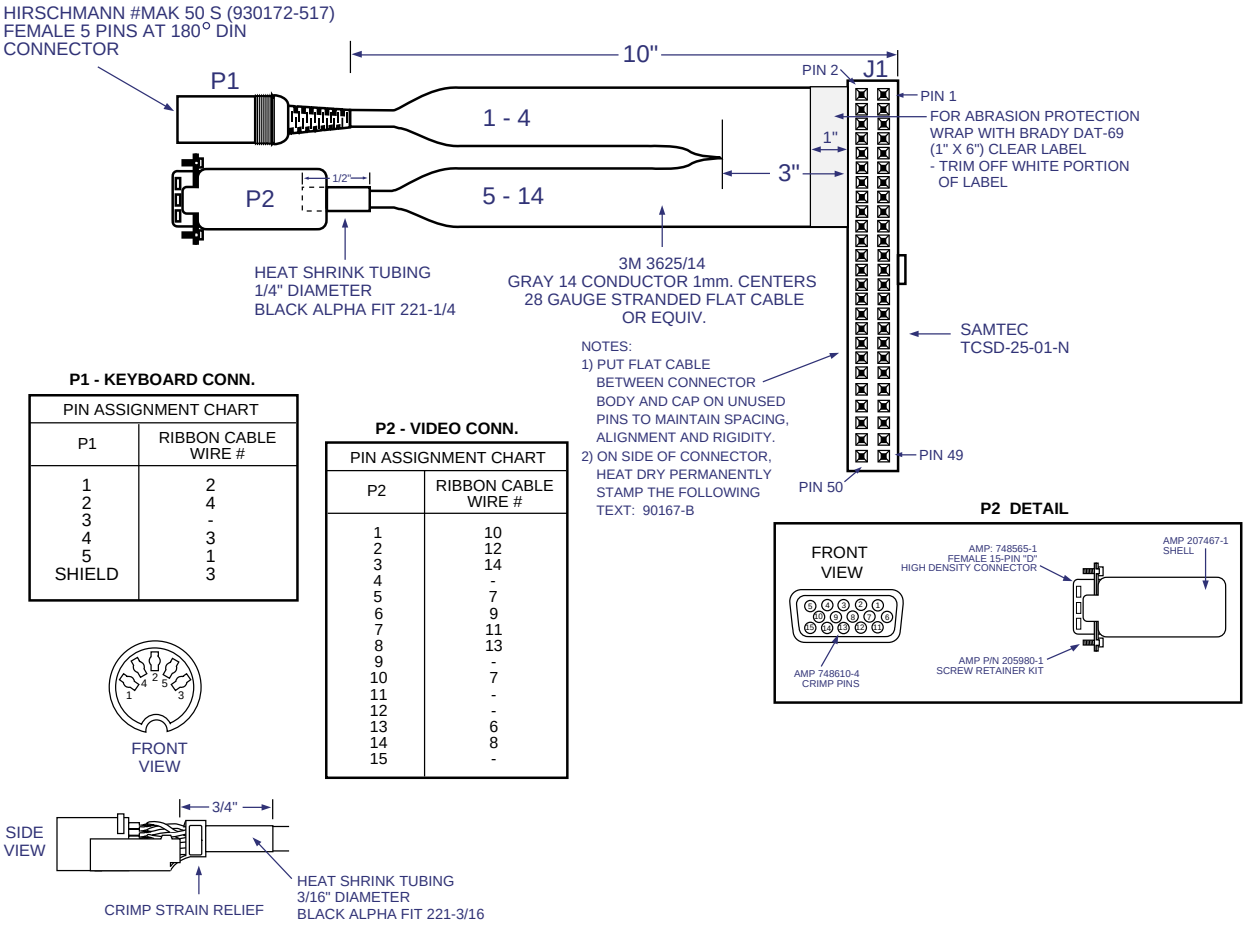
P2 VIDEO CONN.

PIN ASSIGNMENT CHART	
P2	J1
1	10
2	12
3	14
4	-
5	7
6	9
7	11
8	13
9	-
10	7
11	-
12	-
13	6
14	8
15	-

P2 DETAIL



ZT 90166 zVID2 Panel Mount Video and Keyboard Cable



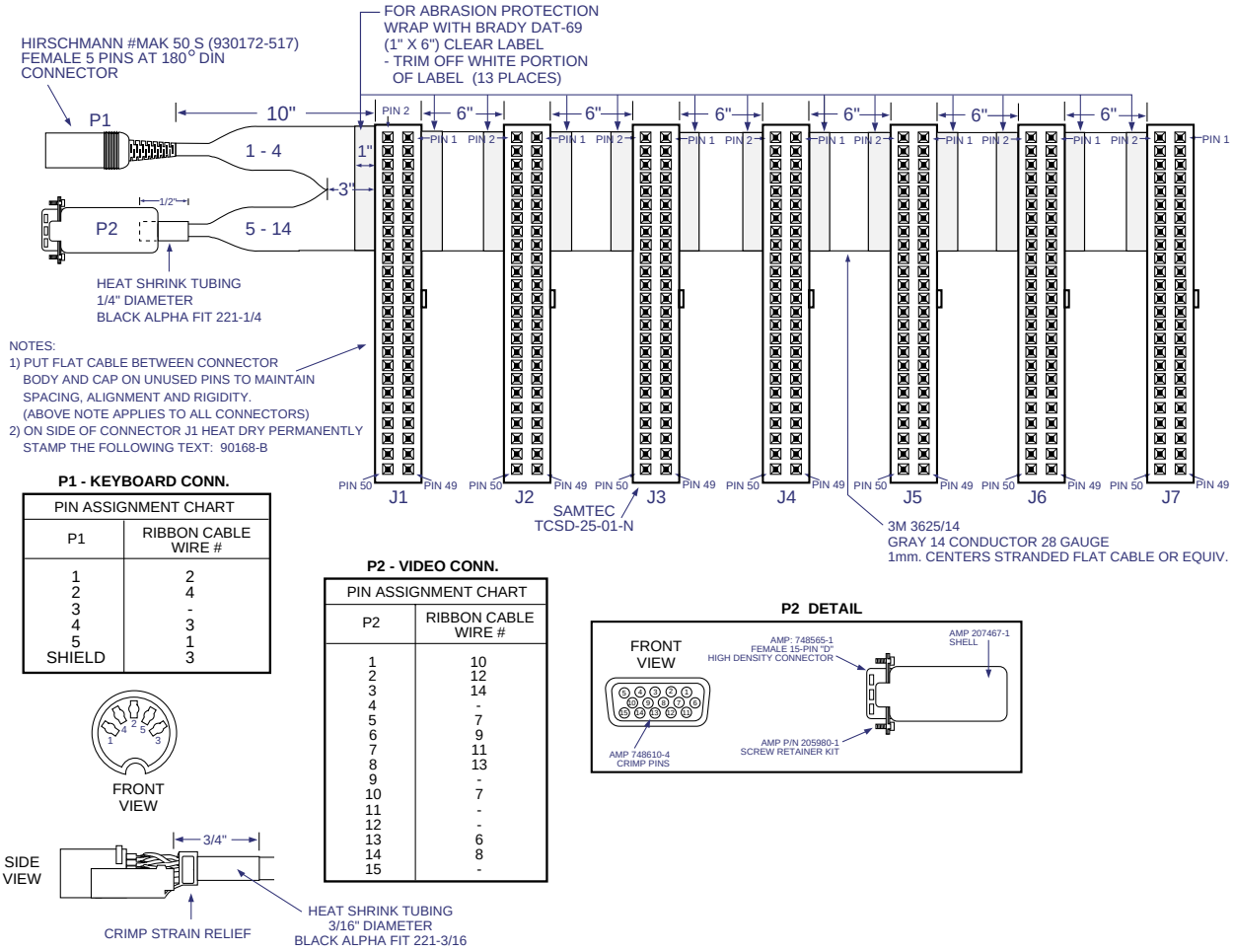
P1 - KEYBOARD CONN.

PIN ASSIGNMENT CHART	
P1	RIBBON CABLE WIRE #
1	2
2	4
3	-
4	3
5	1
SHIELD	3

P2 - VIDEO CONN.

PIN ASSIGNMENT CHART	
P2	RIBBON CABLE WIRE #
1	10
2	12
3	14
4	-
5	7
6	9
7	11
8	13
9	-
10	7
11	-
12	-
13	6
14	8
15	-

ZT 90167 zVID2 Desktop Video and Keyboard Cable



P1 - KEYBOARD CONN.

PIN ASSIGNMENT CHART	
P1	RIBBON CABLE WIRE #
1	2
2	4
3	-
4	3
5	1
SHIELD	3

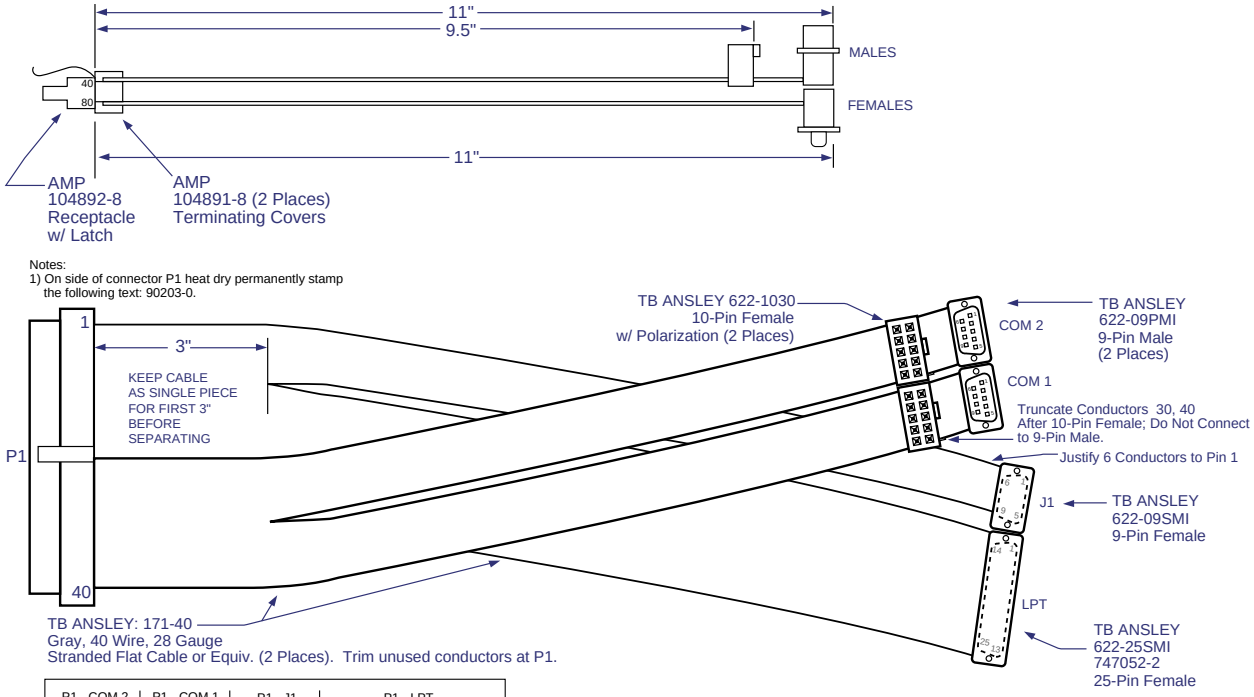
FRONT VIEW

P2 - VIDEO CONN.

PIN ASSIGNMENT CHART	
P2	RIBBON CABLE WIRE #
1	10
2	12
3	14
4	-
5	7
6	9
7	11
8	13
9	-
10	7
11	-
12	-
13	6
14	8
15	-

P2 DETAIL

ZT 90168 Multiple zVID2 Cable



Notes:
1) On side of connector P1 heat dry permanently stamp the following text: 90203-0.

P1 - COM 2	P1 - COM 1	P1 - J1	P1 - LPT	
21 - 1	31 - 1	41 - 1	47 - 1	60 - 20
22 - 6	32 - 6	42 - 6	48 - 14	61 - 8
23 - 2	33 - 2	43 - 2	49 - 2	62 - 21
24 - 7	34 - 7	44 - 7	50 - 15	63 - 9
25 - 3	35 - 3	45 - 3	51 - 3	64 - 22
26 - 8	36 - 8	46 - 8	52 - 16	65 - 10
27 - 4	37 - 4	NC - 4 [2]	53 - 4	66 - 23
28 - 9	38 - 9	NC - 9 [2]	54 - 17	67 - 11
29 - 5	39 - 5	NC - 5 [2]	55 - 5	68 - 24
30 - NC(+5) [1]	40 - NC(+5) [1]		56 - 18	69 - 12
			57 - 6	70 - 25
			58 - 19	71 - 13
			59 - 7	

[1] *Connect to 10-Pin Female for +5V, no connection to 9-Pin Male (COM1-2)*
[2] *Justify 6 Conductors toward Pin 1.*

ZT 90203 Dual Serial and Printer Cable for the ZT 8903

C. PIA SYSTEM SETUP CONSIDERATIONS

The 16C50A Parallel Interface Adapter (PIA) device used on the ZT 8904 is designed by Ziatech to offer bidirectional I/O signals with or without event sense capability. This device features low power, high speed, wide temperature operation achievable only by utilizing CMOS technology.

Although CMOS technology offers many advantages, you must observe a few cautions when interfacing to any CMOS parts.

CMOS inputs and outputs can exhibit latchup characteristics. These inherent characteristics of any CMOS technology can result in the formation of a Silicon-Controlled Rectifier (SCR) that appears between Vcc and ground when voltages greater than Vcc or less than ground are applied to inputs or outputs.

When this happens, Vcc is effectively shorted to ground. The only way to remove the latchup condition is to shut off the power supply. If a large current is allowed to flow through the chip, its operating temperature may increase, it may exhibit intermittent operation, or it may be damaged.

CMOS inputs must be protected from slow rising signals and inductive coupling on their inputs. Failure to do so will allow a potentially large current to flow through the chip, damaging the chip.

The purpose of this appendix is to illustrate precautions you should take to prevent latchup conditions and protect inputs.

PREVENTING SYSTEM LATCHUP

The most common causes of latchup are:

- Input signals applied before the input circuitry is powered, resulting in a signal to power supply sequence mismatch
- Input signals greater than Vcc or less than ground, resulting in a signal level mismatch

Each of these conditions is covered in the following topics.

Power Supply Sequence Mismatch

A common application is to interface to a 24-position ZT 2226, Opto 22, or equivalent I/O module rack. Vcc and ground are provided from the ZT 8904 through connector J4 with Vcc protected by a 1 A fuse. This application is illustrated in Figure 1 below. In this application, no power supply sequence mismatch exists because the power supplying the input circuitry within the PIA is applied before or at the same time as the power supplying the external signals. Proper system operation will result.

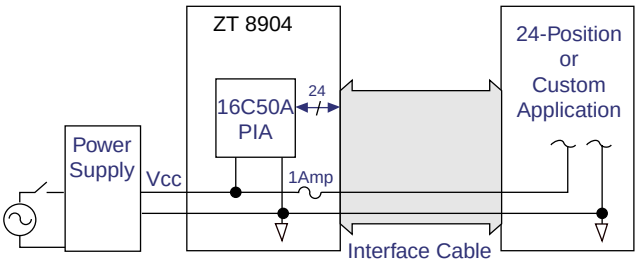


Figure 1. I/O Rack Vcc and Ground Supplied through Interface Cable

Correct Power Supply Sequence, Signal Level Matched

However, if a power source other than that supplying the PIA is used to power the external signals, then a power sequence mismatch could occur, resulting in a latchup condition. An external power source might be required if the external circuitry requires more than the 1 A supplied by the cable or if a custom interface is being designed. Refer to Figure 2 below for an example.

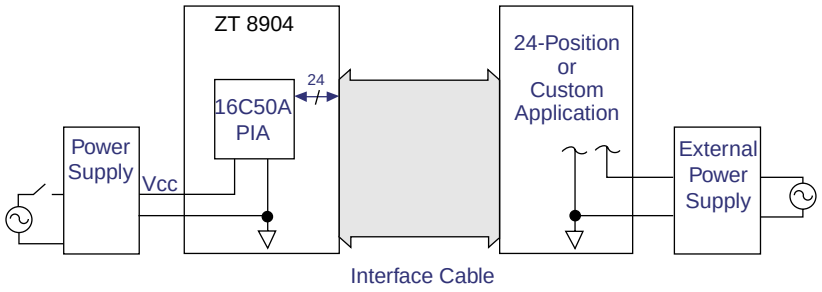


Figure 2. I/O Rack Vcc and Ground Supplied Externally

Potential Power Supply Sequence Mismatch, Signal Level Mismatch

One solution is to switch the external signals' power supply with an output that is controlled by the computer. In this manner, if the computer is off, so is the external power supply. This solution is illustrated in Figure 3 following.

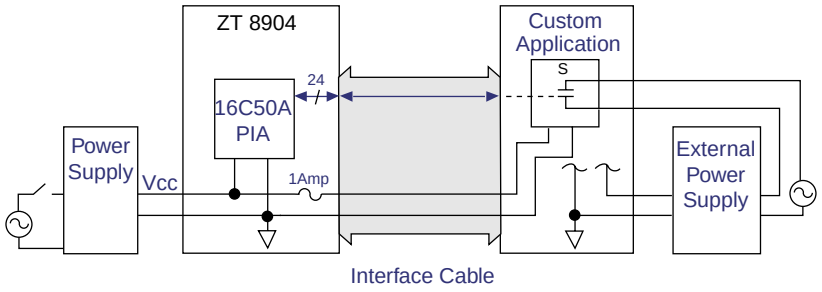


Figure 3. Computer-Switched External Power Supply

Correct Power Supply Sequence, Potential Signal Level Mismatch

A simpler solution is to power the relay controlling the external power supply directly from Vcc and ground supplied by the interface cable.

Another solution is to utilize the same switch to control the computer's power supply and the external signals' power supply, as illustrated in Figure 4. This is an acceptable solution for power supply sequence mismatches as long as the computer supply ramps up faster than the external power supply. This ensures the PIA input circuitry is powered before the external signal circuitry.

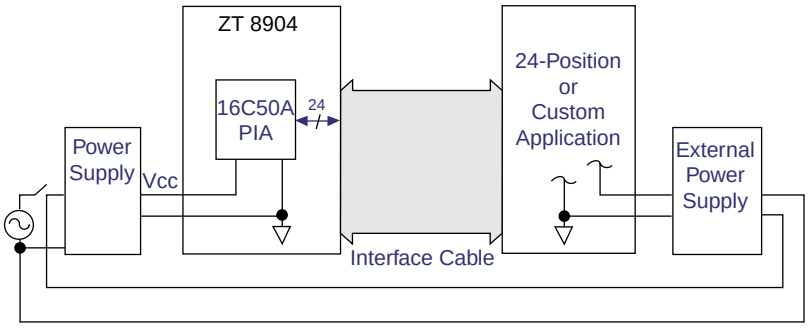


Figure 4. Computer and External Power Supply with Common Switch

Correct Power Supply Sequence, Potential Signal Level Mismatch

Signal Level Mismatch

Power supplying the external signal in Figure 1 is always relative to the PIA input circuitry power because power is provided over the interface cable. Signal level mismatches will not occur and proper system operation will result. However, if separate power supplies are used, there are two predominant causes of signal level mismatches.

The first (assuming no sequencing problems) occurs when the two supplies are not referenced to each other, as illustrated in Figures 2, 3, and 4 above. This results in signals that may be higher than Vcc or lower than ground, potentially causing SCR latchup. All that is generally needed is to reference one supply to the other, typically by connecting a common ground. The most convenient way of connecting a common ground is to use the interface cable. Figures 5, 6, and 7 below illustrate correct ground connections.

The second cause of mismatch occurs when the two power supplies are referenced to each other but the Vcc difference between the two power supplies exceeds .5 V. This results in signals that could be greater than Vcc, causing SCR latchup. This is easily remedied by adjusting the external power supply voltage to be within .5 V of the computer power supply voltage.

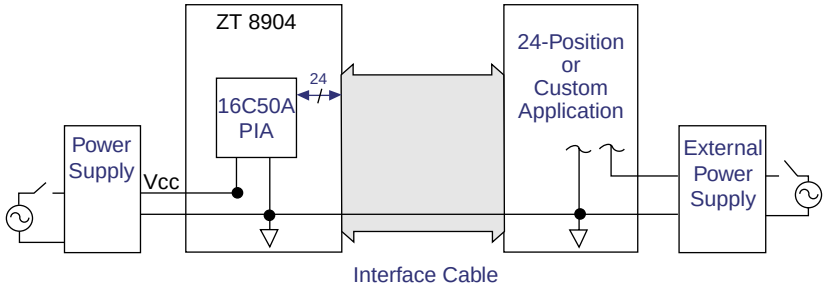


Figure 5. I/O Rack Vcc Supplied Externally, Common Ground

Potential Power Supply Seq. Mismatch, Correct Signal Level Match

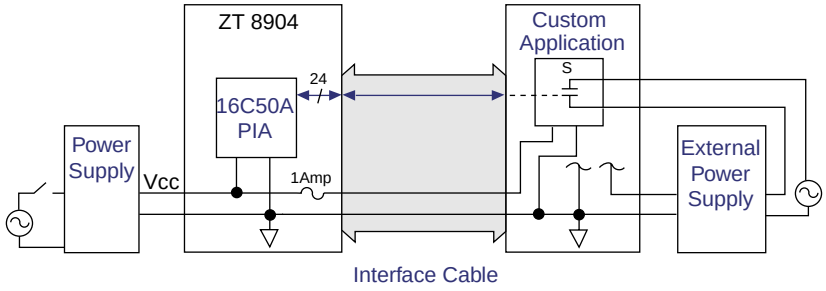


Figure 6. Computer-Switched External Power Supply, Common Ground

Correct Power Supply Sequence, Correct Signal Level Match

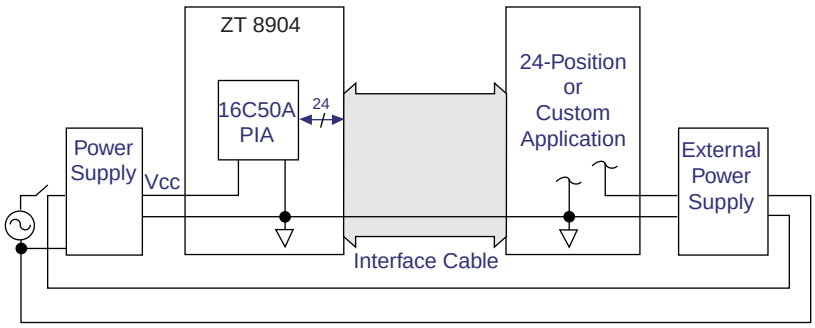


Figure 7. Computer and External Power Supply with Common Switch and Ground

Correct Power Supply Sequence, Correct Signal Level Match

PROTECTING CMOS INPUTS

The most common causes of damaged inputs are:

- Slow rise times, resulting in a ground bounce within the chip
- Inductive coupling on I/O lines causing noise to be coupled into the chip, resulting in intermittent operation

Each of these conditions is covered in the following topics.

Rise Times

Slow rise times on a CMOS input can easily cause the transistor to bounce between Vil and Vih. When this oscillation occurs, the operating current goes up, resulting in "ground bounce." Ground bounce can cause internal latchup or can cause other system components to malfunction. A pullup termination resistor is used to increase the rise time.

Input rise times must be kept to less than 50 ns. Given a maximum chip capacitance of 10 pF, a 5k Ω resistor is the largest that could be used without additional cabling. As cabling is added, the capacitance goes up, resulting in the use of a smaller pullup resistor until the maximum sink current of the output is achieved.

If the 16C50A PIA device is driving the output, its maximum sink current at a Vol of .4 V is 12 mA. This gives a lower limit of 420 Ω for the pullup resistor, allowing a maximum cabling capacitance of 110 pF. Note that while the input feature of the PIA may not be used by your application (PIA used as an output only), the input circuitry remains in parallel; therefore, the output rise time is still a critical parameter that the input still sees. The output rise time must not exceed 50 ns.

Be wary of using low pass filters to remove electrical noise. The resulting capacitance is typically too large to meet the 50 ns rise time requirement.

Typically, optical isolators are used to help remove electrical noise while providing for different grounds. Separate grounds are achieved through the use of an additional power supply for the optocoupler rather than using the computer's power supply. If the computer's power supply powers the optocouplers, electrical isolation is defeated. An example of one such circuit is illustrated in Figure 8 below. The circuit can be altered to allow for design considerations.

Assuming a Vil of 1 V maximum for the 16C50A PIA, the HP Dual Optocoupler must have a Vol of less than or equal to 1 V over the operating temperature. Using a TTL-compatible optocoupler gives a Vol of .6 V maximum with rise and fall times (50 ns and 10 ns, respectively) that are easily compatible with the PIA, given a 1k Ω pullup.

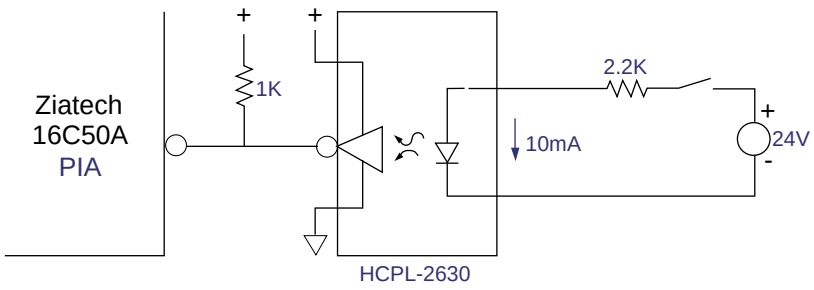


Figure 8. PIA-to-Optocoupler Interface Example

Inductive Coupling

Inductive coupling on I/O lines can cause noise to be coupled into the chip, resulting in intermittent operation. This situation occurs when the PIA I/O signals are routed with other signals within a wire bundle. One way to filter inductively coupled noise, or any noise for that matter, within a system with the same ground (not using optocouplers) is illustrated in Figure 9.

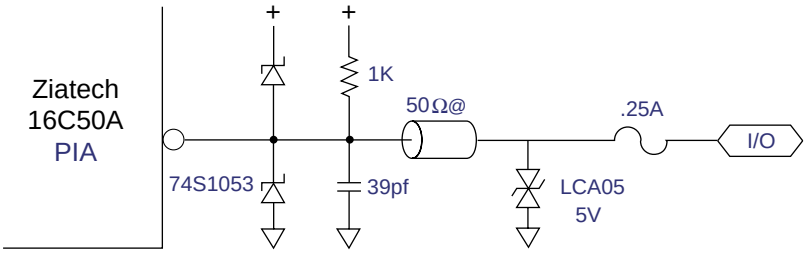


Figure 9. PIA-to-Filter Interface Example

In the above circuit, the Texas Instruments 74S1053 Schottky diode clamps limit a transient to ±1 V above +5 V or below ground. The ferrite bead has a 50 Ω impedance at the frequency of interest. As the diodes begin to clamp and current flows through them, the voltage across the LCA05 5 V bidirectional TransZorbs® increases, causing

them to conduct and allowing the majority of energy to flow through them instead of through the diode clamps. The 39 pF capacitor, in conjunction with the ferrite bead, forms an additional low pass filter, and is entirely optional. The 1k Ω pullup ensures adequate rise time on the signal. The fuse acts as additional insurance against catastrophic events that might destroy the TransZorb and diode clamps.

ADDITIONAL INFORMATION

You can find additional design information in the *Advanced CMOS Logic Designer's Handbook* published by Texas Instruments.

D. CUSTOMER SUPPORT

This appendix offers technical assistance and warranty information for this product, and also the necessary information should you need to return a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

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San Luis Obispo, CA 93401 USA

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FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.

2. Supply a purchase order number for invoicing the repair if the warranty expired.

3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

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