1553-PCI3
MIL-STD-1553 Interface

Features

- 1 to 4 dual redundant 1553 channel featuring 100% concurrent and independent operation as a:
  - Bus Controller
  - 31 Remote Terminals
  - Bus Monitor
- Bus Controller
  - Programmable Linked Lists
  - Minor/Major Framing
  - Dual Conditional Branching
  - Robust Scheduling Features
  - High/Low Priority Async
  - Built-In Monitoring
  - Full Error Injection/Detection
  - Optional Multiple DMAs/Block
- Remote Terminal
  - Programmable Linked Buffers
  - Programmable Response Time
  - Built-In Monitoring
  - Autorun/Autoload Feature
  - 1760 Busy Bit Operation
  - Full Error Injection/Detection
  - Multiple DMAs/Message Option
- Bus Monitor
  - Full Error Detection
  - Double Buffered Monitoring
  - 48-bit, 1-μsec Time Stamp
  - Definable/Filtered Monitoring
  - Multiple DMAs/Message Option
- PCI/PCI-X Architecture
  - 33/66 MHz (PCI)
    - 66 MHz (PCI-X)
  - Multiple DMA Channels
  - FPGA Processing @ > 100 MHz
  - 1 MB RAM w/parity per channel

- In-System Updates
- Variable Voltage 1553
- Support for 3.3V and 5V PCI
- Up to 40 TTL, 12 RS-422 I/Os
- Temperature Sensor
- Software Support
  - Complimentary drivers for most operating systems
  - Integrated Avionics Library, including source code

1553-PCI3 is a flexible interface providing a 1 to 4 channel, single or full function, dual redundant MIL-STD-1553 interface to the PCI backplane. The full function version provides concurrent operation as a Bus Controller (BC), 31 Remote Terminals (RT), and dual function Bus Monitoring (BM), while the single function version provides operation in one of above modes, including 31 Remote Terminals. 1553-PCI3 equips the PCI bus system wit a complete 1553 interface, including 1553A/1553B selections, pointer-driven transmit and receive buffers, extensive programmable event interrupts, and triggers. An available DMA option provides you with the flexibility of using multiple DMAs per message. Both versions include IRIG time code generator capability.

BC simulation structures consist of linked lists of 1553 command messages: BC-to-RT, RT-to-BC, RT-to-RT, mode code, broadcast and time delay block transmissions. RT simulation consists of a simple series of pointers to RT definition tables. The tables in turn point to control data buffers. Buses can be monitored in both Map and Sequential modes, providing user defined linked lists of data buffers and sequential 1553 activity. 1553 activity can be time stamped and/or double buffered. Both monitoring modes

perform broad error monitoring and provide a comprehensive error table that the host processor can read at any time.

Hardware Overview

GE bases the interface upon an advanced high speed Field Programmable Gate Array (FPGA) and dual port RAM. It delivers a highly reliable hardware platform that is feature rich and user friendly. Through the 1 MB of RAM (with parity) per channel, the host processor has access to set up, monitor, and change the 1553 interface data structures at any time. Link-list memory architecture allows you to structure interface memory usage for maximum flexibility and usefulness.

The card supports conventional PCI specs along with the newest PCI-X specification at speeds ranging from 33 to 66 MHz, with data transfer rates up to 266 MB/s. Using the optional DMA features of the data structures allows data buffers to automatically update to and from the system memory without host processor intervention. The 1553-PCI3 supports up to 40 TTL level I/O signals and 12 RS-422 Differential I/O signals. These signals can be controlled either via the user application or automatically via the data structures. The card design allows easy customization of I/O control and is available upon request.

Software Support Overview

GE distributed software includes host processor device drivers to the dual port control, along with data structures and an application layer to these structures. GE also provides low-level drivers for most operating systems, and the Integrated Avionics Library, with source code, at no additional cost.

1553-PCI3 MIL-STD-1553 Interface

Specifications

PCI3 Functionality: Bus Controller (BC)

- BC retry
- Major and minor frame timing and message scheduling
- Programmable intermessage gap
- Programmable delay gaps and null BC blocks
- Multiple BC data buffers in a linked list structure
- Programmable RT no-response time-out
- Error injection/detection
- Multiple DMAs per block
- Dual Conditional Branching per block
- High and low priority asynchronous message
- Built-In monitoring of full message, including response, time stamping and gap
- Command and Error Counters
- Extensive interrupt events

Remote Terminals (RTs)

- 31 RTs and all subaddresses supported
- Transmit/Receive buffers for each subaddress
- Multiple RT data buffers in a linked list structure
- Programmable RT response time and no response selection
- Error injection/detection
- Multiple DMAs per message
- Built-In monitoring of full message, including response, time stamping and gaps
- External RT Address via I/O pins
- 1760 Busy bit operation
- Autorun/Autoload feature allows the card to automatically start operation from user pre-loaded data structures stored in Flash memory
- Data Wrapping feature
- Message and Error Counters by RT and Buffer Counter in each buffer
- Extensive interrupt events

Map Monitoring

- Multiple linked buffers for each transmit/ receive subaddress
- Mapped buffers read by host processor as time permits
- Number of buffers per transmit/receive subaddress is programmable or user definable to account for various host speeds
- Multiple DMAs per message
- Extensive interrupt events

Sequential Monitoring

- Host driver selected messages are double buffered
- Messages time stamped with a 1 µs 48-bit clock or optional 48-bit IRIG-B clock
- Standard firmware performs broad error monitoring
- Comprehensive error table readable at any time by host processor
- Multiple DMAs per message
- Extensive interrupt events

Self Test

- Power-up test with status register report (Power-up BIT)
- Initiated Built-In-Test (IBIT)
- BIT-RAM and encoder/decoder test
- Run-time health status monitor/Continuous BIT (CBIT)
- Unit Test application for 1553 bus functionality
- Built-in internal test bus to support testing without disconnecting from the external 1553 bus. This feature also allows forinternal simulation between multiple channels.

Inputs/Outputs

- Bi-directional external triggers/discretes: Up to 40
- External TTL/RS-422: Up to 12
- IRIG clock input (optional IRIG output)
- Variable voltage 1553 outputs: 0-22 V p-p

PCI and PCI/X Functionality

- PCI-X compliant 66 MHz
- PCI compliant 33/66 MHz
- Up to 266 MB per second maximumtransfer rate
- 16-bit and 32-bit transfer modes
- Multiple Programmable DMA Controllers
- On-board firmware storage via Flash memory. User in-system upgradable.
- Support for 5 V and 3.3 V PCI bus

Interface Connections

- 80-pin SCSI type connector
- BJ77F Triax connector to 1553 bus
- Software programmable Transformer (Long) or Direct (Short) stub interfacing

Interface Card Specifications

- Mechanical-single channel:
  - 1/2 length PCI bus card
  - Length: 6.875" Height: 4.2"
- Maximum power consumption (98% bus activity) - single channel: TBD
- Standard commercial temperature: 0°C to +70°C 95% rH non-condensing

Software and Documentation Support

- Low-level drivers for most operating systems
- Integrated Avionics Library w/source code
- Borland and Microsoft® C Compiler compatible
- Hardware and Integrated Avionics Library documentation included on CD. Hard copies of the documentation are available upon request.

Customer Support

- Two-year warranty
- Extended warranties available
- Driver and library upgrades
- Many operating systems supported on various platforms

Configurations

Model Number	Configuration
1553-PCI3-(1-4)FC00	Full Function 1553 to cPCI interface, 1 to 4 Channels, IRIG
1553-PCI3-(1-4)SC00	Single Function 1553 to PCI interface, 1 to 4 Channels, IRIG, Multi RT

About GE Intelligent Platforms

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