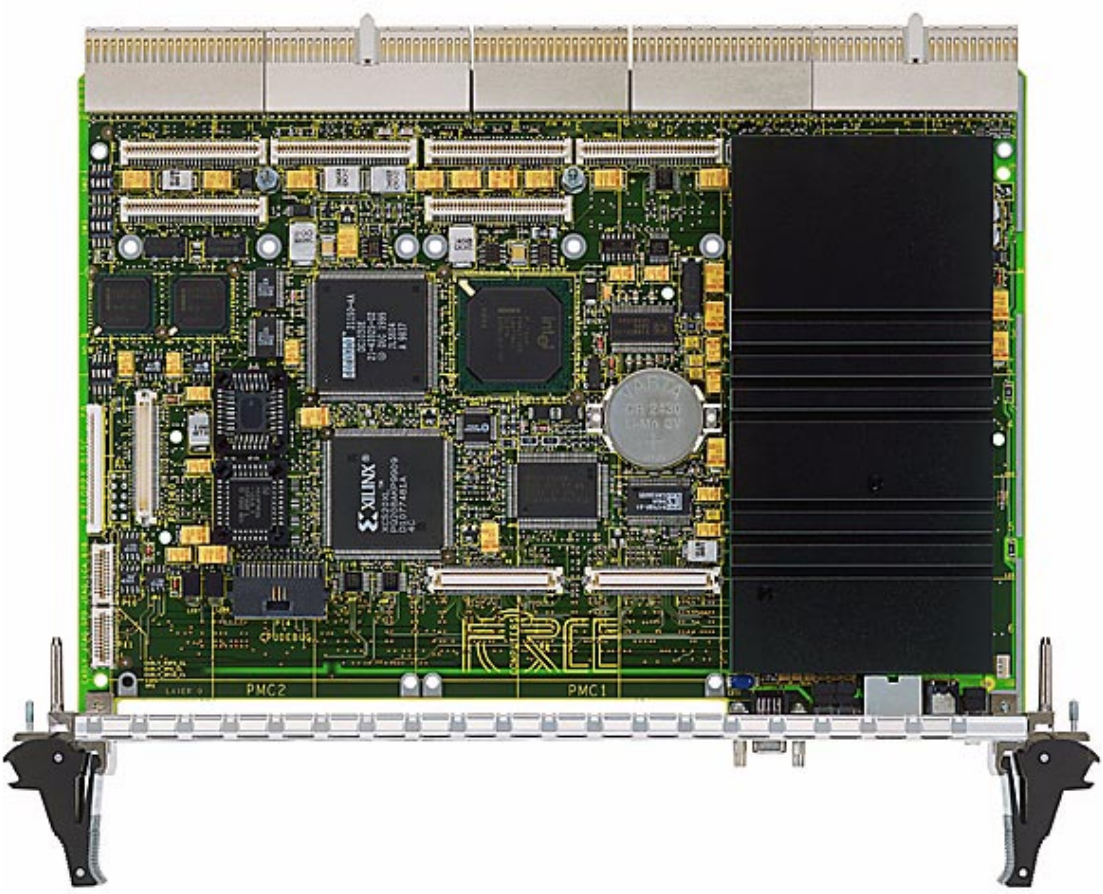
A SOLECTRON COMPANY

PENT/CPCI-731

Installation Guide

P / N 213021 Revision AD
August 2001



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Using This Manual

This Installation Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), Compact Peripheral Component Interconnect (CPCI), and telecommunications.

Conventions

Notation	Description
1234	All numbers are decimal numbers except when used with the notations described below.
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signaled
Bold	Character format used to emphasize a word
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for buttons
Note:	No danger encountered. Pay attention to important information marked using this layout.
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible
Danger 	Dangerous situation: injuries to people or severe damage to objects possible

Revision History

Order No.	Revision	Date	Description
211605	1.0	December 1999	First Print
211605	2.0	February 2000	Corrected Forced Air Flow in Table 5 “Environmental Requirements” on page 2-5
213021	AA	June 2000	Changed SW2-3 to ON in Table 6 “PENT/CPCI-731 Switch Settings” on page 2-15; Corrected the “BIOS” section on page 4-1; Merged Reference Guide with SAP No. 211605 to Installation Guide with SAP No. 213021; editorial changes
213021	AB	March 2001	Revised layout of Installation Guide; Corrected default setting of second bit in Table 18 “Reset Control Register 1” on page 6-11; Added the “Troubleshooting” section on page 7-1
213021	AC	July 2001	Corrected information on default setting of white switches in the “Switch Settings” section on page 2-15; Updated the “BIOS” section on page 4-1; Removed Troubleshooting section; Added the “Appendix” section on page A-1; Added the “Index” section on page I-1; Editorial changes;
213021	AD	August 2001	Added the “Sicherheitshinweise” section on page -xxiii

Other Sources of Information

For further information refer to the following documents:

Company	Web Address	Documents
Force Computers	www.forcecomput-ers.com	PENT / CPCI-730 Installation Guide (P / N 212399)
		PENT / CPCI-731 / HD-AccKit
		IOBP-CPCI-731
Intel	www.devel-oper.intel.com	BIOS flash: 1Mx8, 28F008S5
		CPU: Intel Pentium II
		Intel Pentium II Processore Mobile Module: Mobile module connector 2 (MMC-2)
		Intel Architecture Software Developer's Manual Volume 1: Basic Architecture Volume 2: Instruction Set Refer-ence Manual Volume 3: System Programming Guide
		EIDE, PCI-to-ISA bridge, USB: 82371AB (82371EB)
		Ethernet: 82559
		Host-to-PCI bridge: 82443BX
		PCI-to-PCI bridge: 21150
		PCI-to-PCI bridge: 21554
Hitachi / Micron / Mitsubishi	www.halsp.hitachi.com	8Mx8 (M5M4V64S30A) SRAM
National	www.national.com	Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy: PC87309 SuperI / O
Philips Semiconduc-tor	www. philips.com	The I^2C bus and how to use it (including specifications)
SanDisk	www.sandisk.com	IDE flash disk: Flash Chipset, SDFCSTB-128-366
Winbond	www.winbond.com	Hardware monitor: W83781D

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PENT/CPCI-731. For your protection, follow all warnings and instructions found in the following text.
This Installation Guide provides the necessary information to install and handle the PENT/CPCI-731. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The PENT/CPCI-731 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, uninstall or maintain the PENT/CPCI-731. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A.

These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The board generates, uses and can radiate radio frequency energy and, if not installed properly and used in accordance with this Installation Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If boards are integrated into open systems, always cover empty slots.

To ensure proper EMC shielding, always operate the PENT/CPCI-731 with the blind panels or with PMC modules installed.

Installation

Electrostatic discharge and incorrect board installation and removing can damage circuits or shorten their life. Therefore:

- **Before installing or removing the board, check the "Requirements" section on page 2-4.**
- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**

Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the CompactPCI rack and shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Hot Swap

Never install or remove the board in a system under hot-swap conditions unless the basic hot-swap, full hot-swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components).

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMI and the possibly changed functionality of the product.

IOBP

The IOBP-CPCI-731 is especially designed for the base board of the PENT/CPCI-731. Do not connect any other I/O panels with the PENT/CPCI-731.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as your PENT/CPCI-731. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meter.**

Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as a power backup. Therefore, back up affected data before exchanging the battery.**

- **Always use the same type of Lithium battery as is already installed.**
- **If the battery is covered by a PMC module on slot 1 or by a memory module, the module must be removed first.**
- **Use an appropriate tool to remove the battery from its holder to avoid possible damage to the board or the battery holder.**
- **When installing the new battery, ensure that the '+' on top of the battery stays at the top and therefore is visible when viewing the board from its component side. If necessary, reinstall the PMC or memory module in its correct position.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des PENT/CPCI-731 zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des PENT/CPCI-731. Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das PENT/CPCI-731 erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls kann es dieses ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet und entspricht den Grenzen eines Klasse-A-Produktes gemäß Abschnitt 15 der FCC-Richtlinien, insbesondere EN 55022 Klasse A.

Diese Grenzen sind dafür vorgesehen, einen vernünftigen Schutz gegen störende Einflüsse bei einem Betrieb in einer kommerziellen Umgebung zu gewährleisten.

Das Board erzeugt elektromagnetische Strahlung. Wird das System unsachgemäß installiert oder in anderer Weise als in diesem Installationshandbuch beschrieben betrieben, kann es in der Umgebung von Rundfunksendern und in Wohngegenden zu Störungen kommen. In diesem Fall ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen und die Kosten von Messungen selbst zu tragen.

Werden Boards in offene Systeme eingebaut, müssen freie Steckplätze mit einer Blende abgeschirmt werden.

Um eine ausreichende Abschirmung zu gewährleisten, darf das Board nur mit einer Blindblende oder mit einer installierten PCMCIA-Karte betrieben werden.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt “Requirements” auf Seite 2-4**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf das Front Panel, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Strom an allen Power Pins anliegt.**

Betrieb

Während des Betriebs müssen die Umgebungs- und die Stromsversorgungsbedingungen gewährleistet sein.

Wenn das Board in Gebieten mit starker elektromagnetischer Strahlung betrieben wird, stellen Sie sicher, dass das Board auf dem Compact PCI Rack verschraubt ist und mit einem Gehäuse geschützt ist.

Es ist sicherzustellen, dass Anschlüsse und Kabel des Boards während des Betriebs nicht versehentlich berührt werden können.

Hot Swap

Einbau oder Ausbau des Boards in einem System unter Hot Swap Bedingungen darf nur dann stattfinden, wenn die grundlegende Hot Swap Plattform, die vollständige Hot Swap Plattform, oder die Hochverfügbarkeits Hot Swap Plattform benutzt wird und die Systembeschreibung ausdrücklich die geeigneten Richtlinien vorgibt.

Erweiterung

Beachten Sie den Gesamtstromverbrauch aller installierter Komponenten (siehe technische Daten der entsprechenden Komponente).

Vergewissern Sie sich, daß jeder individuelle Ausgangsstrom jedes Stromverbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe technische Daten des entsprechenden Verbrauchers).

Benutzen Sie bei der Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Ansonsten sind Sie für die Auswirkungen auf EMV und die möglicherweise geänderte Funktionalität des Produktes verantwortlich.

IOBP

Das IOBP-CPCI-731 ist speziell für das Basis-Board der CPCI-731 entwickelt worden. Verwenden Sie kein anderes IOBP zusammen mit der CPCI-731.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Tauschen Sie die Batterie aus, bevor die fünf Jahre tatsächlicher Betriebsdauer vorbei sind.**
- **Beim Austausch der Batterie gibt es immer einen Datenverlust bei den Bausteinen, die die Batterie aus Notstromversorgung verwenden. Sichern Sie deshalb die betroffenen Daten vor dem Austausch der Batterie.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Falls die Batterie von einem PMC Modul auf Steckplatz 1 oder von einem Speichermodul verdeckt wird, muss erst das Modul entfernt werden.**
- **Verwenden Sie zum Entfernen der Batterie aus dem Halter geeignetes Werkzeug, um Schaden an Board oder Batteriehalter zu vermeiden.**
- **Vergewissern Sie sich beim Einbau einer neuen Batterie, dass das '+' oben auf der Batterie oben und damit sichtbar bleibt, wenn das Board von der Komponentenseite betrachtet wird. Falls nötig, installieren Sie das PMC-Modul oder das Speichermodul in der dafür vorgesehenen Position.**

Umweltschutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

1

Introduction

Features

The PENT/CPCI-731 is a 6U CompactPCI computer based on the Intel Pentium III CPU and is a CompactPCI non-host or I/O board. It requires the space of one slot. All PENT/CPCI-731 PCI buses are 32-bit wide and operate at 33 MHz PCI bus frequency.

The PENT/CPCI-731 is qualified to run with Windows NT Version 4.0. or higher, VxWorks and LynxOS. It is provided with inrush current protection and supports full hot swap.

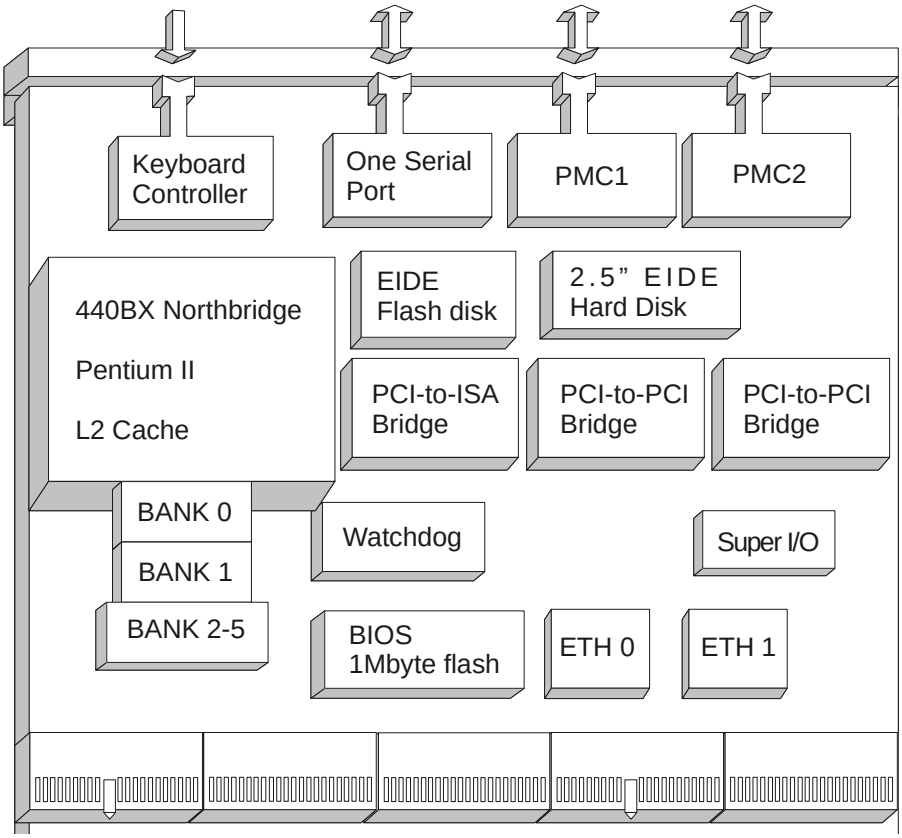


Figure 1: *Function Blocks*

CPU

The PENT/CPCI-731 offers a mobile module based on a Pentium II processor with 333 MHz speed or higher with 512 KByte L2 cache or a Pentium III processor with 500 MHz speed with 256 KByte L2 cache.

Additional features are:

- Motorola 146818 compatible real-time clock and CMOS RAM for storing factory settings, both RTC and RAM with battery backup
- Program-readable vintage registers for board information protocol (BIP)
- Software-controllable, scalable watchdog, which controls the CPU activity and causes a RESET or an NMI in case of malfunction
- Two 82C37A compatible DMA controllers on the PCI-to-ISA bridge
- Two 82C29 compatible interrupt controllers on the PCI-to-ISA bridge
- 8254 compatible 3-channel timer

Memory

Memory features include:

- One MByte flash BIOS, 8-bit wide
- Optional 16 MByte flash disk
- Synchronous DRAM with ECC support running at 66 or 100 MHz clock frequency
- Up to 768 MByte main memory with ECC, depending on selected memory option

Interfaces

The front panel and on-board interfaces of the PENT/CPCI-731 are shown in the table below.

Table 1: *Interfaces*

Interface	Description
Ethernet	Two 10/100 BaseTEthernet available via CompactPCI connector J5 (IOBP-CPCI-731)
Floppy	Floppy controller via CompactPCI connector J4
IDE	Primary IDE interface available via on-board connector Secondary IDE interface available via CompactPCI connectors J4 and J5
Keyboard/Mouse	PS2 keyboard and mouse interface available on front panel and on CompactPCI connector J5
Parallel I/O	Parallel interface IEEE 1284, compatible with ECP (Extendend Capabilities Port) and EPP (Extended Parallel Port) at CompactPCI connector J4
PMC	Two PMC interfaces, both supporting the front panel interface and the rear interface via CompactPCI connectors J3 and J5
Serial I/O	Two serial interfaces COM1 on front panel and on CompactPCI connector J3 COM2 on CompactPCI connector J3
USB	Two USB interfaces available on CompactPCI connector J3

Block Diagram

This block diagram serves as an overview of how the PENT/CPCI-731 devices operate together and which data paths they use.

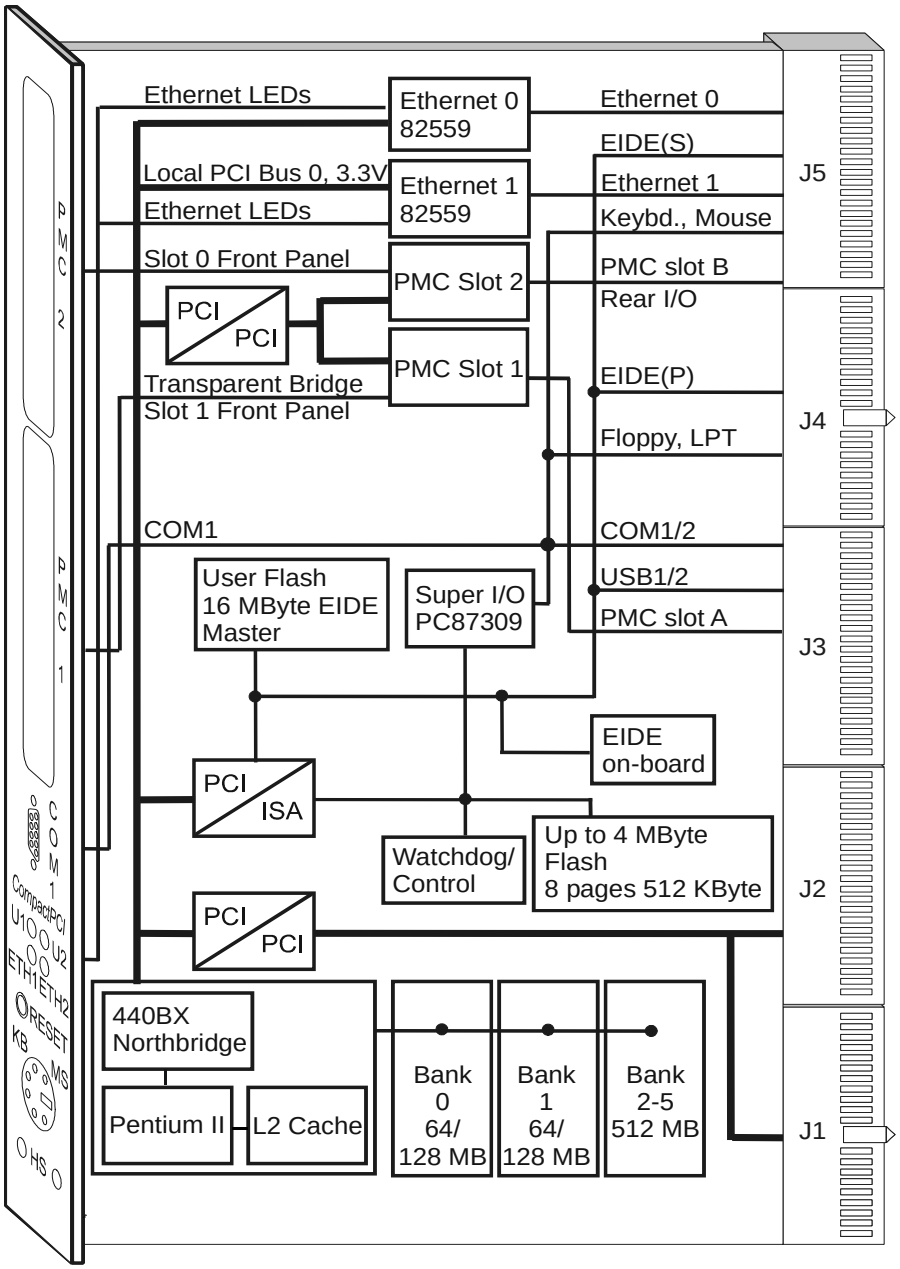


Figure 2: *Block Diagram*

Standard Compliance

The PENT/CPCI-731 complies with the following standards:

Table 2: *Standard Compliance*

Standard	Description
IEC 68-2-1/2/3/13/14	Climatic environmental requirements.The PENT/CPCI-731 can only be used in an restricted temperature range (see Table 5 “Environmental Requirements” on page 2-5 for details.)
IEC 68-2-6/27/32	Mechanical environmental requirements
EN 609 50/UL 1950 (predefined Force system); UL 94V-0/1	Legal requirements
EN 50081-1, EN 50082-2, FCC Part 15 Class A	EMC requirements on system level
ANSI/IPC-A-610 Rev.B Class 2, ANSI/IPC-R-700B, ANSI-J-001...003	Manufacturing requirements
ISO 8601	Y2K compliance

Ordering Information

When ordering PENT / CPCI-731 board variants, upgrades, and accessories, use the order numbers given below.

Product Nomenclature

The following table will provide you with the key for the product name extensions.

Table 3: *Nomenclature*

PENT/CPCI-731//dd-ppp-Lccc-u	
ddd	DRAM size in MByte
ppp	Processor clock frequency in MHz
Lccc	L2 cache capacity in KByte
u	MByte IDE flash disk

Order Numbers

The upgrades and accessories available depend on the variant of the PENT/CPCI-731 under consideration. Consult your local sales representative to confirm availability of specific combinations.

Table 4: *Ordering Information Excerpt* [1)]

Order No.	PENT/CPCI-731	Description
106759	.../128-266-L512-0	Intel Pentium II 266 MHz with 128 MByte main memory, 512 KByte L2 cache, no flash disk
106666	.../256-333-L256-16	Intel Pentium II 333 MHz with 256 MByte main memory, 256 KByte L2 cache, 16 MByte flash disk
107092	PENT/MEM-700/III	III= 512 MByte memory module
107088	PMC/VGA-4	PMC based VGA graphics card and related installation components
Accessories PENT/CPCI-731		
106810	.../HD-AccKit	Hard Disk and related installation components
106619	IOBP/CPCI-731	Rear transition board and related installation components
Software Accessories PENT/CPCI-731		
106710	.../BIOS Upgrade Kit	BIOS upgrade utilities

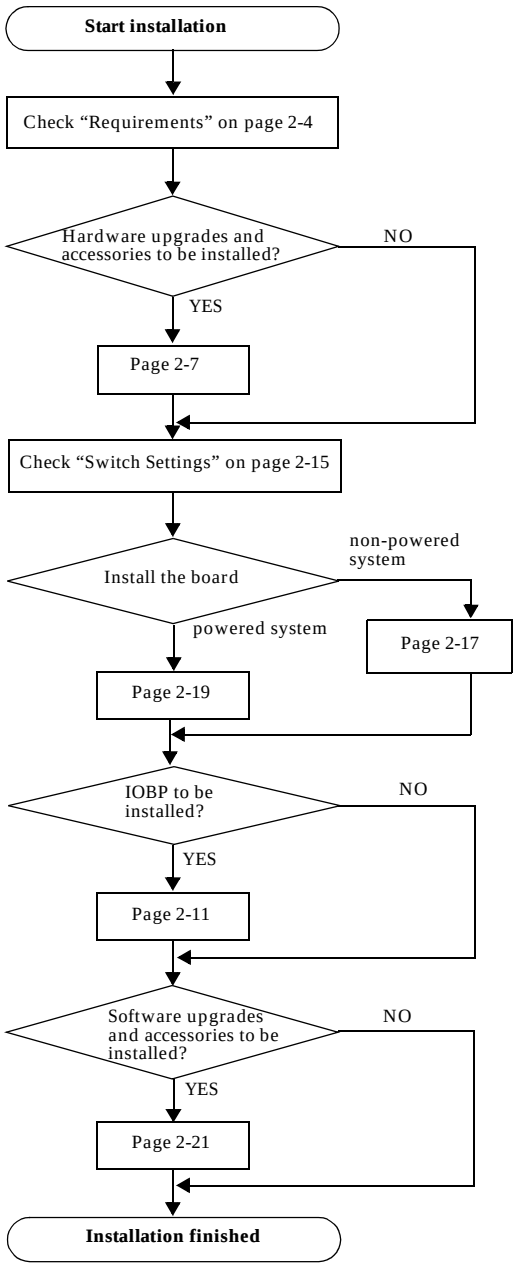
1) Status: August 2001

2

Installation

Action Plan

In order to install the board, follow the procedure listed in the flow chart below.



Requirements

The PENT/CPCI-731 fulfills the standard Force Computers reliability requirements for board products. It is a CompactPCI peripheral slot board. The PCI bus supports 32-bit data bus width with a frequency of 33 MHz.

Caution

Always install the PENT/CPCI-731 in a peripheral slot which is marked by a circle. Otherwise, irreversible damage may occur to the board or to the system into which the board has been installed.

Environmental Requirements

The environmental values must be tested and proven in the used system configuration. These conditions refer to the surroundings of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature. To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.

Table 5: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature[1)]	0°C to +55°C	–40°C to +85°C
Forced Air Flow (in LFM= Linear Feet per Minute)	300 LFM	-
Temp. Change	+ / - 0.5°C/min	+ / - 1°C/min
Rel. Humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C
Altitude	-300 m to + 3,000 m	- 300 m to + 13,000 m
Vibration 10 to 15 Hz 15 to 150 Hz	 2 mm amplitude 2 g	 5 mm amplitude 5 g
Shock[2)]	5 g / 11 ms halfsine	15g / 11 ms halfsine
Free Fall	100 mm / 3 axis	1,200 mm / all edges and corners (packed state)

1. For information on the allowed hard disk operating temperature, consult the Installation Guide of the PENT / CPCI-731 / HD-AccKit.
2. For information on shock and vibration values that are valid when using the PENT / CPCI-731 together with the PENT / CPCI-731 / HD-AccKit, refer to the Installation Guide of the PENT / CPCI-731 / HD-AccKit.

Caution

If the PENT/CPCI-731/HD-AccKit is installed on the PENT/CPCI-731, operating temperature, shock and vibration values are limited by the hard disk environmental requirements. For details, refer to the Installation Guide of PENT/CPCI-731/HD-AccKit.

Power Requirements

The power requirements of the PENT/CPCI-731 depend on the PMC modules installed. The PENT/CPCI-731 provides a limited current at the PMC supply pins. If no other boards are installed, these are the typical power requirements for 5V and 3.3V for the PENT/CPCI-731:

- Current of 1.8A at +5V
- Current of 1.7A at +3.3V

If you want to install any accessories, the load of the respective accessory has to be added to the load of the board variant. For information on the accessory's power requirements, refer to the documentation delivered together with the respective accessory or consult your local Force Computers representative.

Caution

The total maximal power consumption per PMC slot at +/-12V, 5V, and 3.3V level must not exceed 7.5W (total overall used voltages).

Hardware Upgrades and Accessories

The PENT/CPCI-731 allows for an easy and cost-efficient way to adapt the board to the application's needs by adding memory modules, PMC modules, and a hard-disk drive.

Memory Module

In addition to the local SDRAM of the PENT/CPCI-731, the memory module PENT/MEM-700 with SDRAM chips can be installed on the PENT/CPCI-731. The maximum possible memory size of the memory module is 512 MByte. This allows a maximum possible system memory of 768 MByte in total.

Note: The memory module option can only be installed on this location if no PMC is required on this slot.

For installation information, refer to the Installation Guide shipped with the memory module.

PMC Module

The PENT/CPCI-731 provides two cutouts to enable the installation of PMC modules. If the PENT/CPCI-731 is shipped without modules installed, the front panel cutouts are covered by blind panels to ensure proper EMC shielding.

Note:

- **To ensure proper EMC shielding, always operate a PENT/CPCI-731 with the blind front panel or with the modules installed.**
- **If the PENT/CPCI-731 is upgraded with PMC modules, ensure that the blind panels are stored in a safe place to be used again when removing the upgrades.**

Slots 1 and 2

The PMC slot 1 can be used to install a standard PMC module with front panel I/O and rear I/O onto the PENT/CPCI-731. The PMC slot 2 can be used to install a standard PMC module with front panel I/O and rear panel I/O onto the PENT/CPCI-731.

Note: Slot 1 is only available if no memory module is installed and Slot 2 is only available if no hard drive is assembled.

Voltage Keys

The PCI bus uses a 5V or 3.3V voltage signal level on the PMC slots (factory option). The appropriate voltage key prevents 3.3V PMC cards, or respective 5V PMC cards, from being plugged into the PMC slots.

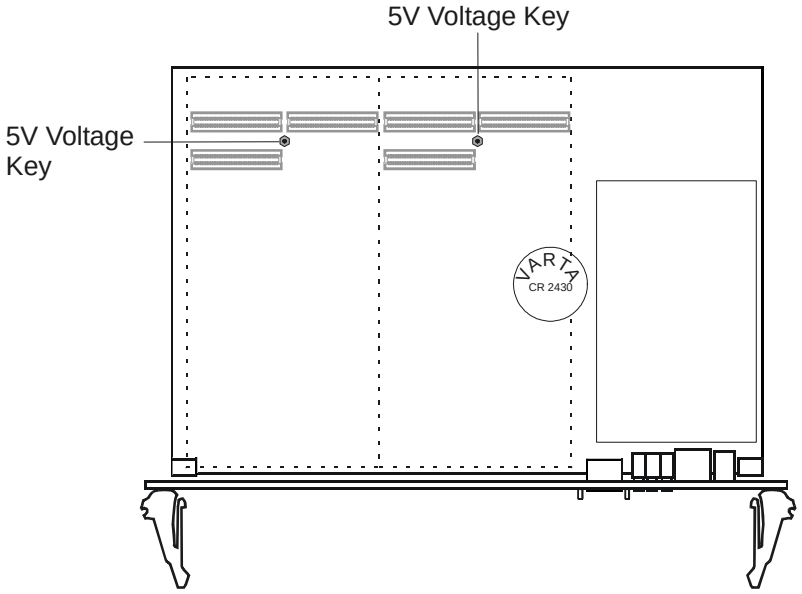


Figure 3: *Voltage Keys*

Connector Configuration

The 32-bit PCI bus requires two PMC connectors. The third PMC connector connects additional user I/O signals of PMC slots 1 and 2 with the CompactPCI J3 and J5 connector.

Installing the PMC Module

In order to install a PMC module on a PMC slot, proceed as follows:

Note: If PMC slot 1 is intended for use, the memory module option cannot be used. If the space for PMC slot 1 is occupied by a memory module, the memory module must first be removed. If PMC slot 2 is intended for use, the on-board hard drive option cannot be used. If the space of PMC slot 2 is occupied by a hard drive, the hard drive must first be removed.

---

1. Remove blind panel of respective PMC slot from front panel and store in safe place
2. Plug PMC module into connectors PN11, PN12, and PN14 for PMC slot 1 or PN21, PN22, and PN24 for PMC slot 2, so that standoffs of module fit on mounting holes PN11...PN14 or PN21...PN24

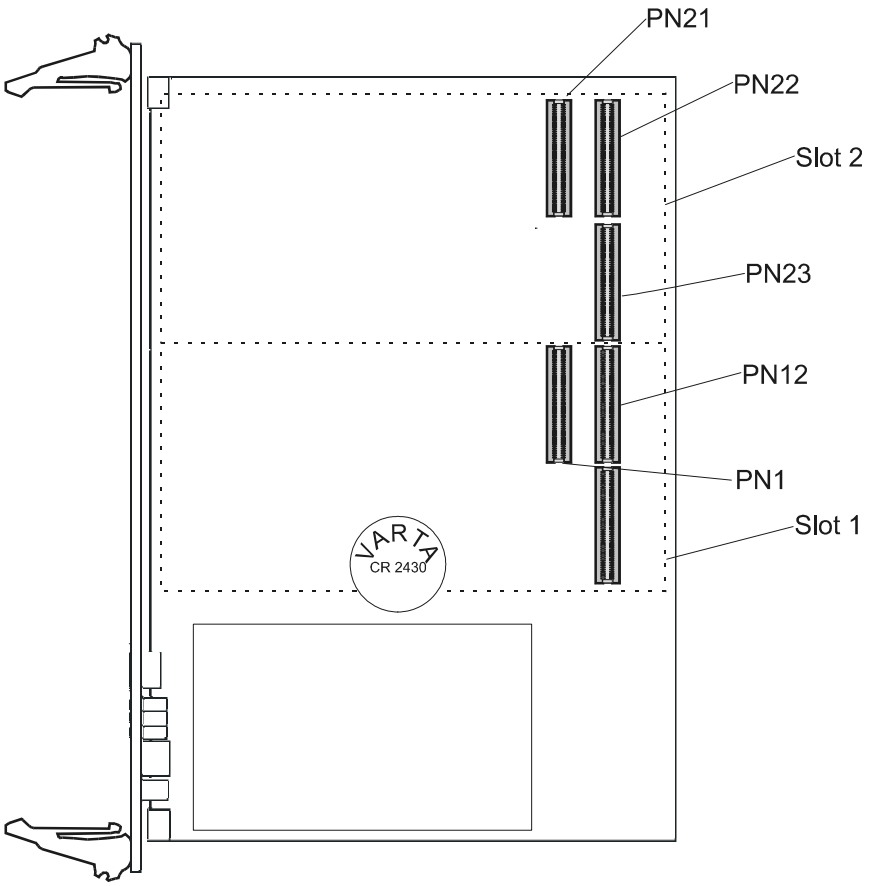


Figure 4: *PMC Connectors and Slots*

3. Check whether standoffs of module cover mounting holes of PENT/CPCI-731

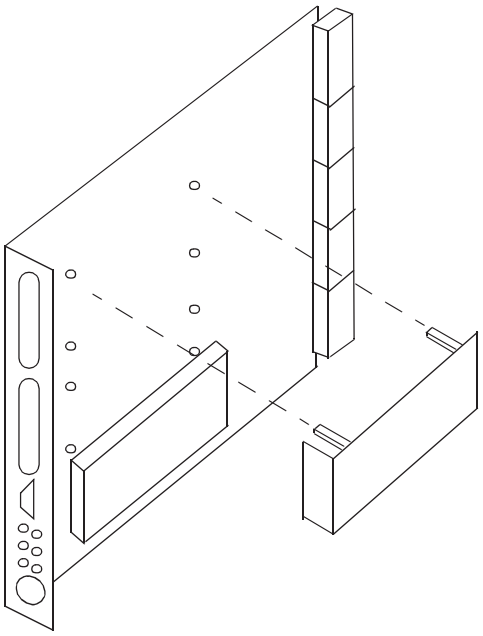


Figure 5: *Position of Mounting Holes*

4. Place screws delivered together with PMC module in mounting holes
5. Fasten screws

Removing the PMC Module

In order to remove a PMC module from PMC slots 1 or 2, proceed as follows:

1. Remove screws 1 through 4
2. Remove PMC module carefully from slot
3. Cover front panel at free slot with blind panel

VGA-Acc-Kit

The VGA accessory kit PMC/VGA is a PMC-based VGA card. It can be installed in one of the PMC slots of the PENT/CPCI-731. For installation information refer to the Installation Guide delivered together with the VGA accessory kit.

IDE Devices

It is possible to have up to two IDE devices on the PENT/CPCI-731:

- As a factory option, a 16 MByte flash disk can be installed on the board. It is connected to the primary IDE port.
- A HD-accessory kit can be installed to the primary IDE port via the on-board connector.

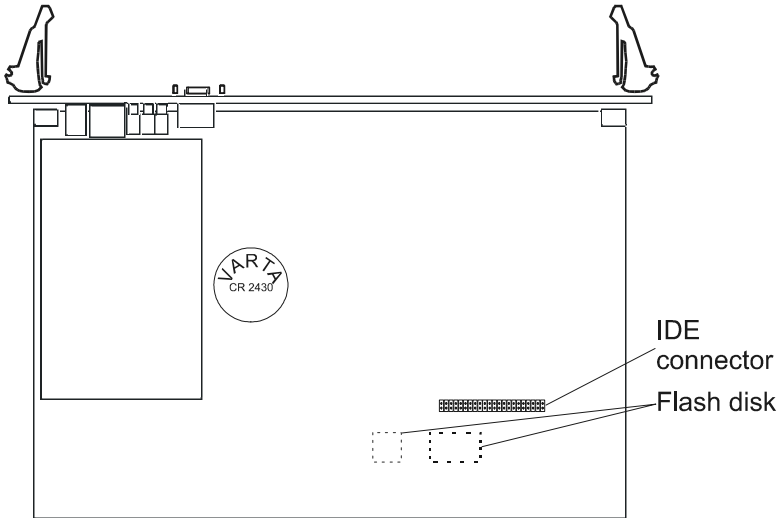


Figure 6: *Flash Disk and IDE Connector*

HD-Accessory Kit

The PENT/CPCI-731/HD-AccKit is a local mass storage device. It has to be connected to the primary IDE port via the on-board connector. The 2.5" hard drive may be installed at the location of the PMC slot 2 instead of a PMC module.

For installation information, refer to the Installation Guide delivered together with the hard disk accessory kit.

Caution

If the standard PENT/CPCI-731/HD-AccKit is installed, the operation temperature of the PENT/CPCI-731 is limited by the maximum operation temperature of the hard disk. If the maximum operation temperature of the hard disk is lower than the maximum temperature of the PENT/CPCI-731, the maximum temperature specified for the hard disk must not be exceeded.

Note: If the hard disk is installed on the PENT/CPCI-731 with a 16 MByte flash disk, either the hard disk or the flash disk has to be set to IDE master. For the configuration options, refer to the Installation Guide delivered with the hard disk accessory kit and to "Switch Settings" on page 2-15.

IOBP-CPCI-731

The IOBP-CPCI-731 is available as a separate price list item for the PENT/CPCI-731. It has to be connected to the PENT/CPCI-731 from the rear after the CPU board has been installed.

The IOBP-CPCI-731 provides access to the base board's CompactPCI user I/O interfaces via industry standard connectors. It is included in the IOBP-CPCI-731 accessory kit, containing the I/O panel itself and the cables.

Caution

The IOBP-CPCI-731 is especially designed to be used on the PENT/CPCI-731. Do not use any other I/O panels on the PENT/CPCI-731.

For additional information, refer to the IOBP-CPCI-731 Installation Guide.

Floppy Disk Connection

The floppy disk connector provides BIOS field upgrade ability of the PENT/CPCI-731 if no IOBP-CPCI-731 is available.

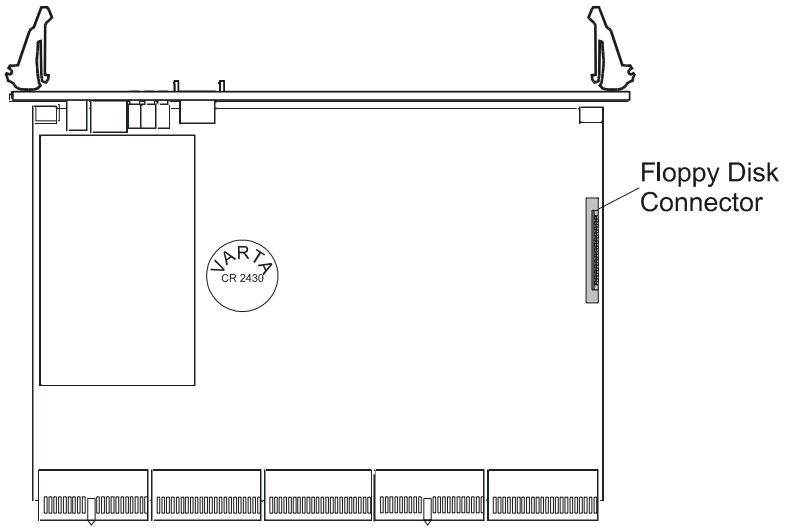


Figure 7: *Floppy Connector*

Switch Settings

The PENT/CPCI-731 is configurable via three micro switches, SW1, SW2, and SW3. The switches are located on the left-hand side of the base board seen from the front panel.

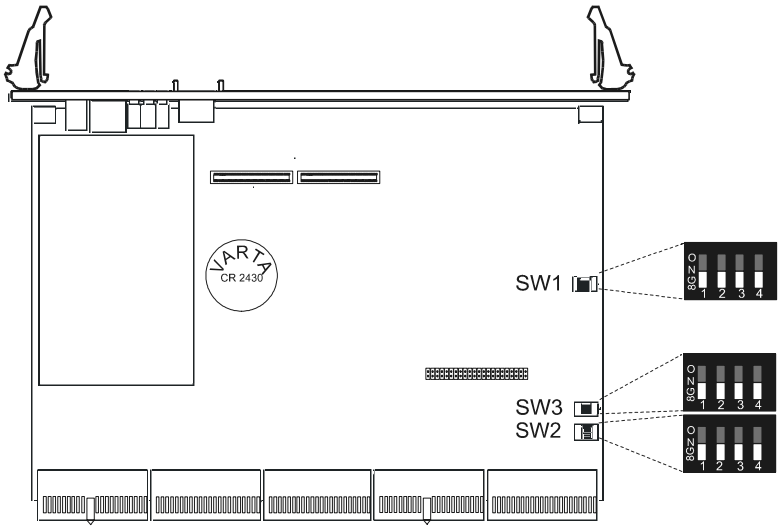


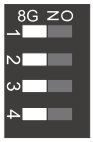
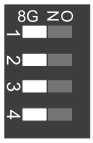
Figure 8: *Switch Sets*

As default setting, the white switches are moved to the OFF position, except for SW2-3 whose default position is set to ON.

Table 6: *PENT/CPCI-731 Switch Settings*

Name and Default Settings		Description
SW1 	1	I^2C USER EEPROM write protection OFF (default): Write-protected ON: Write enabled
	2	Boot Block write protection OFF (default): Write enabled ON: Write-protected
	3	Flash disk enable OFF (default): Flash disk disabled ON: Flash disk enabled
	4	Flash Disk Master/Slave (boot enable) OFF (default): Primary IDE slave ON: Primary IDE master

Table 6: *PENT/CPCI-731 Switch Settings (cont.)*

Name and Default Settings		Description
SW2 	1	FPGA Download source OFF (default): Via EEPROM ON: Via Download Cable
	2	FPGA Init Select OFF (default): Lower 64KB ON: Upper 64KB
	3	12V Supervising OFF: Enabled ON (default): Disabled
	4	Reset Key OFF (default): Enabled ON: Disabled
SW3 	1	FPGA Spare Switch OFF (default)
	2	FPGA Spare Switch OFF (default)
	3	FPGA Spare Switch OFF (default)
	4	FPGA Spare Switch OFF (default)

Board Installation

Since the PENT/CPCI-731 is a peripheral board, it is not allowed to install the board in a system slot. Otherwise, the board or other cards in the system may be damaged.

Caution

Always plug the PENT/CPCI-731 into a peripheral slot marked by a circle.

The PENT/CPCI-731 provides hot-swap support, i.e. it may be installed in or removed from a powered system supporting hot swap. In this section you will find the instructions for installing the board in a non-powered system and in a powered system supporting hot swap.

Signaling Level

Due to the hot-swap capability and compliance to the CompactPCI Hot Swap Specification 2.1, the PENT/CPCI-731 board can only be used in a 5V system. A 5V voltage key within the CPCI P1 connector prevents the board from being installed in a non-5V system.

Installation in a Non-Powered System

Note: Before installing the board, install the accessories, if necessary (see the "Hardware Upgrades and Accessories" section on page 2-7).

Installing the PENT/CPCI-731

1. Check installation guides of all installed boards for steps to be taken before turning off power, take those steps, and finally turn off power
2. Plug board into peripheral slot
3. Press handles towards front panel to lock board on CompactPCI rack
4. Fasten board with screws

5. Plug in interface cables in front panel connectors, if applicable

Caution **Before powering up the board, check the switch settings for consistency.**

6. Turn on power

Removing the PENT/CPCI-731

1. Check installation guides of all installed boards for steps to be taken before turning off power, take those steps, and finally, turn off power
2. Unplug interface cables from front panel connector, if applicable
3. Unfasten mounting screws
4. Release locks of board on rack by pressing them towards rack
5. Remove board

Installation in a Powered System Supporting Hot Swap

If hot swap is supported by the system, the system documentation includes at least installation guidelines on how to install or remove boards under hot-swap conditions.

Note: When installing or removing the PENT/CPCI-731, refer to the documentation of all installed boards and to the system documentation.

Caution

- **The PENT/CPCI-731 can be used in non-hot-swap platforms, hot-swap platforms, and high-availability platforms. Never install or remove the board in a system under hot-swap conditions unless a hot-swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines for these tasks.**
- **The power of the HDDs connected to the board via IOBPs must be controlled by the 5V supply voltage on the IOBP to ensure that the HDDs are powered down when the PENT/CPCI-731 is removed from or inserted into the system.**
- **The PENT/CPCI-731 as a peripheral board can support full hot swap. This covers board support in the following situation:**

The purpose of hot-swap support is to allow the board to be installed in and removed from a powered system without adversely affecting the system. This is helpful for exchanging faulty boards or reconfiguring a system.

Installing the PENT/CPCI-731

To install the board in the hot-swap system, proceed as follows:

1. Check board configuration (switch settings, additional memory modules)
2. Check use of appropriate rear transition board, if applicable
3. Insert board into powered system
4. Connect software according to system documentation

To install the board in a full hot-swap or high-availability system, proceed as follows:

1. Check board configuration (switch settings, additional memory modules)
2. Check use of appropriate rear transition board, if applicable
3. Insert board into powered system
   The hot-swap LED stays blue until the board goes healthy.

Removing the PENT/CPCI-731

To remove the board in a hot-swap system, proceed as follows:

1. Start removing board by disconnecting software using system documentation
2. Check that software disconnection process has been completed
3. Remove board from powered system

Software Upgrades and Accessories

The only software upgrade and accessory available for the PENT/CPCI-731 is the BIOS-Upgrade Kit. The PENT/CPCI-731/BIOS-UpKit contains a DOS-formatted floppy disk with a BIOS upgrade file and upgrade utilities e.g. to reflect extended hardware support.

For installation information refer to the README file contained on the floppy disk delivered with the PENT/CPCI-731/BIOS-UpKit.

Maintenance

This board is designed to be maintenance-free. The only component which might be exchanged is the Lithium battery installed on the PENT/CPCI-731. Before exchanging the battery, read the information given below.

Battery

The battery provides a data retention of five years summing up all periods of actual battery use. Therefore, Force Computers assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare-part handling.

Caution

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is installed.**

In order to exchange the battery, follow the instructions below:

1. If battery is covered by PMC module or memory module, remove module first

Caution

To avoid possible damage to the PCB or the battery holder, do not use a screwdriver to remove the battery from its holder.

2. Remove battery
3. When installing new battery, ensure that the '+' on top of battery stays at top and therefore is visible when viewing board from its component side
4. If required, reinstall PMC or memory module in its correct position

3

Controls, Indicators, and Connectors

Front Panel

The following figure displays the position of cutouts for PMC modules, connectors, and LEDs on the PENT/CPCI-731 front panel.

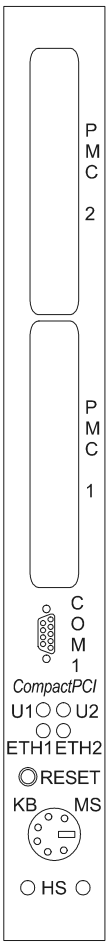


Figure 9: *PENT/CPCI-731 Front Panel*

PMC Cutouts

The PENT/CPCI-731 provides two cutouts to install PMC modules.

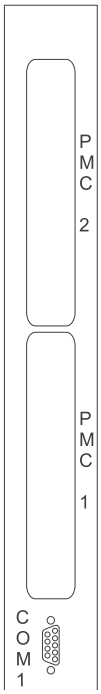


Figure 10: *Cutouts for PMC Modules*

LEDs

The PENT/CPCI-731 provides four front panel LEDs.

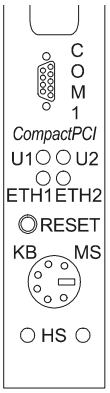
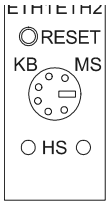


Table 7: *Description of Front Panel LEDs*

LED	Description
U1, U2	Per default U1 signals board power and U2 signals IDE activity. These LEDs are fully software-programmable by means of a register. Possible LED status: Green, red, or off
ETH 1	Ethernet 1 active, link LED: signals status of Ethernet Interface 1. Possible LED status: LED is illuminated when properly connected to an Ethernet Network. LED flashes during network access.
ETH2	Ethernet 2 active, link LED: signals status of ethernet interface 2. Possible LED status: LED is illuminated when properly connected to an Ethernet Network. LED flashes during network access.

Keys

The only front panel key used is the mechanical reset key.



When enabled and toggled, it instantaneously affects the system board by generating a main reset. The main reset generates a CompactPCI reset.

A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. Reset is held active until the key is back in the inactive position, however, at least 200 ms are guaranteed by a local timer. Power fail (below approximately 4.7V) and power up - both lasting a minimum of 200 ms to 300 ms - also force a reset to start the system board.

For information on how to disable the key, see the “Switch Settings” section on page 2-15 and the “Reset” section on page 6-9.

Connectors

The front panel of the PENT / CPCI-731 provides a Keyboard / Mouse and a COM1 connector.

If the PENT / CPCI-731 is to be incorporated into larger systems and adapted to specific needs, the following connector pinouts may be useful to give information on which signal is assigned to which pin.

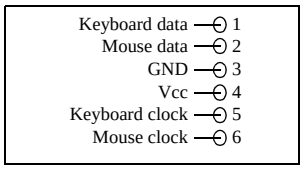


Figure 11: *KBD/MS - Keyboard and Mouse Connector Pinout*

Note: Make sure that the length of the keyboard, mouse and USB cables does not exceed three meters and that the cables are installed apart from other cables.

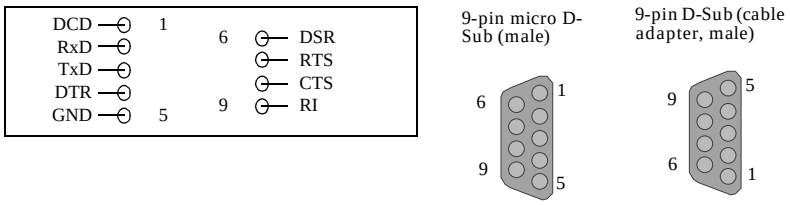


Figure 12: *COM1 Connector Pinout*

CompactPCI Connectors

The PENT/CPCI-731 provides the CompactPCI connectors J1, J2, J3, J4, and J5. The interfaces available on the CompactPCI connectors can be routed to the interface-dependent standard connectors via IOBP-CPCI-731.

The PENT/CPCI-731 provides full hot swap. This, however, does only cover the CPCI interfaces of connectors J1 and J2. If I/O devices are used at the connectors J3, J4, and J5 (e.g. via IOBP-CPCI-731), refer to the respective documentation for hot-swap capability.

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI specification. Therefore, this manual only documents the pinout of the J3, J4, and J5 connectors.

J3

The following interfaces are available via the PENT/CPCI-731 CompactPCI J3 connector (the designations used in the following pinout are given in brackets):

- USB 1 (USB1)
- USB 2 (USB2)
- COM 1 (COM1)
- COM 2 (COM2)
- PMC Slot 1 I/O signals (PMC1IO)

Note: Make sure that the length of the keyboard, mouse and USB cables does not exceed three meters and that the cables are installed apart from other cables.

	A	B	C	A B C D E	D	E	
19	USB2 P+	USB2 P-	USB1 P+		USB1 P-	reserved	19
18	COM1 DTR	COM1 R1	COM2 DTR		COM2 R1	reserved	18
17	COM1 DSR	COM1 DCD	COM2 DSR		COM2 DCD	reserved	17
16	COM1 CTS	COM1 TXD	COM2 CTS		COM2 TXD	reserved	16
15	COM1 RTS	COM1 RXD	COM2 RTS		COM2 RXD	reserved	15
14	3.3 V	3.3 V	3.3 V		5V	5V	14
13	PMC1IO-05	PMC1IO-04	PMC1IO-03		PMC1IO-02	PMC1IO-01	13
12	PMC1IO-10	PMC1IO-09	PMC1IO-08		PMC1IO-07	PMC1IO-06	12
11	PMC1IO-15	PMC1IO-14	PMC1IO-13		PMC1IO-12	PMC1IO-11	11
10	PMC1IO-20	PMC1IO-19	PMC1IO-18		PMC1IO-17	PMC1IO-16	10
9	PMC1IO-25	PMC1IO-24	PMC1IO-23		PMC1IO-22	PMC1IO-21	9
8	PMC1IO-30	PMC1IO-29	PMC1IO-28		PMC1IO-27	PMC1IO-26	8
7	PMC1IO-35	PMC1IO-34	PMC1IO-33		PMC1IO-32	PMC1IO-31	7
6	PMC1IO-40	PMC1IO-39	PMC1IO-38		PMC1IO-37	PMC1IO-36	6
5	PMC1IO-45	PMC1IO-44	PMC1IO-43		PMC1IO-42	PMC1IO-41	5
4	PMC1IO-50	PMC1IO-49	PMC1IO-48		PMC1IO-47	PMC1IO-46	4
3	PMC1IO-55	PMC1IO-54	PMC1IO-53		PMC1IO-52	PMC1IO-51	3
2	PMC1IO-60	PMC1IO-59	PMC1IO-58		PMC1IO-57	PMC1IO-56	2
1	GND	PMC1IO-64	PMC1IO-63		PMC1IO-62	PMC1IO-61	1

Figure 13: *CompactPCI J3 Connector Pinout*

J4

The following interfaces are available on the CompactPCI J4 connector (the designations used in the pinout below are given in brackets):

- Floppy Disk (FD)
- LPT (LPT)
- Primary IDE (PIDE)

	A	B	C	D	E	
25	GND	PIDE CS1#	PIDE INTRQ	PIDE RSTDR#	NC	25
24	PIDE IOW#	PIDE DREQ	PIDE IORDY	PIDE CS3#	PIDE DMACK#	24
23	PIDE D15	PIDE DA0	PIDE DA1	PIDE DIOR#	PIDE DA2	23
22	PIDE D10	PIDE D11	PIDE D12	PIDE D13	PIDE D14	22
21	PIDE D05	PIDE D06	PIDE D07	PIDE D08	PIDE D09	21
20	PIDE D00	PIDE D01	PIDE D02	PIDE D03	PIDE D04	20
19	PIDE DASP#	PIDE PDIAG#	NC	NC	NC	19
18	NC	NC	NC	NC	NC	18
17	NC	NC	NC	NC	NC	17
16	NC	NC	NC	NC	NC	16
15	NC	NC	NC	NC	NC	15
14	Key	Key	Key	Key	Key	14
13	Key	Key	Key	Key	Key	13
12	Key	Key	Key	Key	Key	12
11	NC	NC	NC	NC	NC	11
10	NC	NC	NC	NC	NC	10
9	NC	NC	NC	NC	NC	9
8	NC	NC	NC	NC	NC	8
7	NC	NC	LPT STB#	LPT AFD#	LPT PD2	7
6	LPT INIT#	LPT PD1	LPT ERR#	LPT PD0	LPT PD6	6
5	LPT PD5	LPT PD4	LPT PD3	LPT SLIN#	LPT SLCT	5
4	LPT PE	LPT BUSY#	LPT ACK#	LPT PD7	FD DENSEL	4
3	FD TRK0#	FD WP#	FD RDATA#	FD HDSEL#	FD DSKCHG#	3
2	FD MTR1#	FD DIR#	FD STEP#	FD WDATA#	FD WGATE#	2
1	FD DRATE0	FD INDEX#	FD MTR0#	FD DS1#	FD DS0#	1

Figure 14: *CompactPCI J4 Connector Pinout*

J5

The following interfaces are available via the PENT/CPCI-731 CompactPCI J5 connector (the name used in the below pinout is given in brackets):

- Ethernet 1 (ETH1)
- Ethernet 2 (ETH2)
- Keyboard (KBD), PS2 mouse (MS)

Note: Make sure that the length of the keyboard, mouse and USB cables does not exceed three meters and that the cables are installed apart from other cables.

- PMC Slot 2 I/O signals (PMC2IO)
- Secondary IDE (SIDE)

	A	B	C	A B C D E	D	E	
22	ETH1 TX+	ETH1 RX+	KBD DAT		SIDE INTR	SIDE RSTDR#	22
21	ETH1 TX-	ETH1 RX-	KBD CLK		SIDE DACK#	SIDE CS1#	21
20	GND	AUXVCC	RESET IN		SIDE IORDY	SIDE CS3#	20
19	ETH2 TX+	ETH2 RX+	MS DAT		SIDE IOW#	SIDE DREQ	19
18	ETH2 TX-	ETH2 RX-	MS CLK		SIDE IOR#	SIDE A2	18
17	GND	AUXVCC	SIDE D15		SIDE A0	SIDE A1	17
16	SIDE D10	SIDE D11	SIDE D12		SIDE D13	SIDE D14	16
15	SIDE D05	SIDE D06	SIDE D07		SIDE D08	SIDE D09	15
14	SIDE D00	SIDE D01	SIDE D02		SIDE D03	SIDE D04	14
13	PMC2IO-05	PMC2IO-04	PMC2IO-03		PMC2IO-02	PMC2IO-01	13
12	PMC2IO-10	PMC2IO-09	PMC2IO-08		PMC2IO-07	PMC2IO-06	12
11	PMC2IO-15	PMC2IO-14	PMC2IO-13		PMC2IO-12	PMC2IO-11	11
10	PMC2IO-20	PMC2IO-19	PMC2IO-18		PMC2IO-17	PMC2IO-16	10
9	PMC2IO-25	PMC2IO-24	PMC2IO-23		PMC2IO-22	PMC2IO-21	9
8	PMC2IO-30	PMC2IO-29	PMC2IO-28		PMC2IO-27	PMC2IO-26	8
7	PMC2IO-35	PMC2IO-34	PMC2IO-33		PMC2IO-32	PMC2IO-31	7
6	PMC2IO-40	PMC2IO-39	PMC2IO-38		PMC2IO-37	PMC2IO-36	6
5	PMC2IO-45	PMC2IO-44	PMC2IO-43		PMC2IO-42	PMC2IO-41	5
4	PMC2IO-50	PMC2IO-49	PMC2IO-48		PMC2IO-47	PMC2IO-46	4
3	PMC2IO-55	PMC2IO-54	PMC2IO-53		PMC2IO-52	PMC2IO-51	3
2	PMC2IO-60	PMC2IO-59	PMC2IO-58		PMC2IO-57	PMC2IO-56	2
1	TM_PRNT	PMC2IO-64	PMC2IO-63		PMC2IO-62	PMC2IO-61	1

Figure 15: *CompactPCI J5 Connector Pinout*

4

BIOS

Introduction

BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the board. It is used for the hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the board for the initial boot-up procedure. BIOS offers the following features:

- Hardware set-up utility for setting configuration data
- Multiboot for a flexible boot order
- Software upgrade utilities

The BIOS complies to the following specifications:

- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.1
- BIOS Boot Specification 1.01

The BIOS set-up program is required to configure the hardware of the board. This configuration is necessary for operating the board and connected peripherals. It is stored in the CMOS memory. A battery preserves configuration data when the board is powered off.

When you are not sure about configuration settings, restore the default values. They are provided in case that a value has been changed and one wishes to reset settings. To restore the default values, press <F9> in setup.

Note:

- **Loading the BIOS default values will affect all set-up items and will reset options previously altered.**
- **If you set the default values, the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they become effective if the BIOS setup is exited after changes have been saved.**

Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (power-on self-test). Press <F1> while the message `Press <F1> to enter SETUP` appears on the screen. The main menu appears.

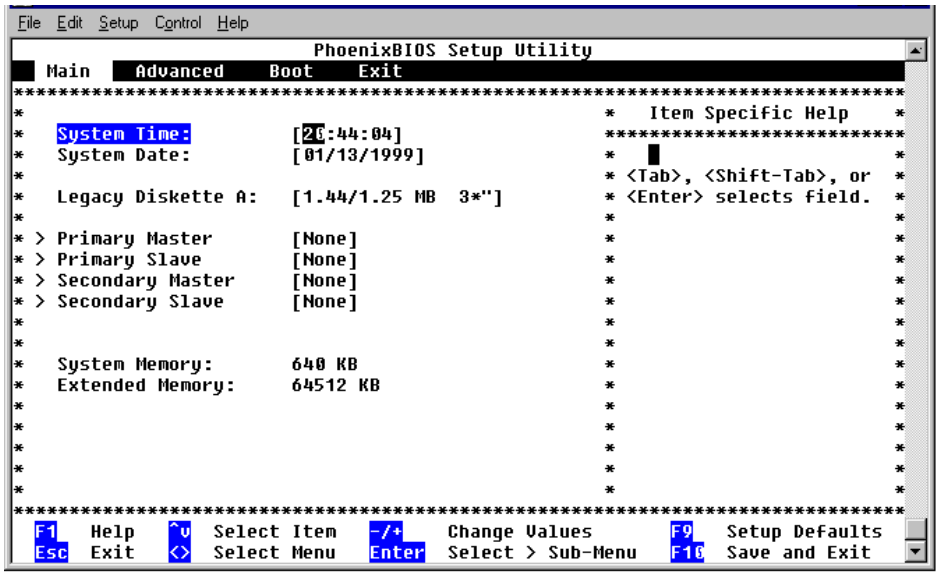


Figure 16: *Main Menu*

Note:

- **Make sure that BIOS is properly configured prior to installing the operating system and its drivers.**
- **If you save changes in setup, the next time the board boots, BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter Setup to get the default values or to change the selections that caused the failure.**

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

Selecting the Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

- Via setup to select a permanent order of boot devices
- Via boot selection menu to select any device for the next boot-up procedure only

Via Setup

To determine the order of boot devices in setup, proceed as follows:

1. In menu line, select [Boot]
2. Select order of devices from which BIOS attempts to boot operating system

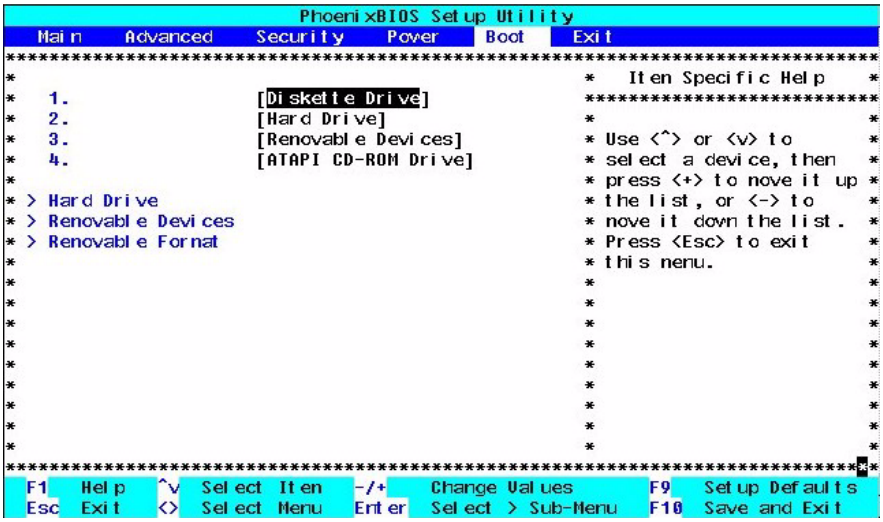


Figure 17: *Boot Device Order*

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

If there is more than one device of the same type, e.g. several hard disks, the displayed entry represents the first of these devices as specified in the boot configuration via setup.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices to which the operating system may assign drive letters A: and B:. The drives C:, D:, E: etc. are reserved for hard-disk drives.

Note: There is not always an exact correspondence between the order specified in setup and the letters assigned by the operating system. Many devices, such as legacy option ROMs, support more than one device that can be assigned to several letters. If the CD-ROM drive should have a letter coming before the one assigned to the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot compliant BIOS option ROM from which you can boot the operating system.

Via Boot Selection Menu

To enter the boot menu, press <ESC> during POST.

Figure 18: *Boot Menu*

Continue with one of the following options:

a) Override existing boot sequence by selecting another boot device from the boot order list

---

Note: If the selected device does not load the operating system, BIOS reverts to the previous boot sequence.

---

b) Select [Enter Setup] to enter setup utility

c) Press <Esc> to return to POST screen and continue with previous boot sequence

Serial Console Redirection

The firmware of the board provides a serial console redirection feature. This allows remote board configuration by connecting a terminal to the board via a serial communication link.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC input. The serial console redirection feature can be configured via setup utility.

Note: If serial console redirection is enabled the terminal represents an option and is not necessarily required for boot-up procedure.

Requirements

For serial console redirection, the following is required:

- Terminal which supports a VT100 or ANSI mode
- NULL-modem cable

Terminal emulation programs such as Hyper Terminal or TeraTermPro can be used.

Serial console redirection does not necessarily require a VGA card. If no VGA card is present, an on-board SRAM memory is used as video buffer.

Remote Configuration

The procedure to configure the board remotely for boot-up depends on the board's configuration.

Remote Configuration Set

If the board is set for remote configuration and if you are familiar with the setting, proceed as follows:

1. Configure terminal to communicate using the same parameters as in BIOS setup
2. Connect terminal to NULL-modem cable
3. Connect NULL-modem cable to COM port you have selected in setup
4. Turn on board

Remote Configuration Not Set

If the board is not set for remote configuration, proceed as follows:

1. Connect monitor and keyboard to board
2. Turn on board
3. Press <Del> when `Press <DEL> to enter SETUP` appears on screen
4. Select [Advanced]
5. Select [Console Redirection]
6. Select appropriate parameters for communication
7. Save setup
8. Reboot board
9. Configure terminal to communicate using same parameters as in BIOS setup
10. Connect NULL-modem cable to COM port you have selected in setup

Updating BIOS via Software

For the board the BIOS upgrade kit PENT/CPCI-731/BIOS-UpKit is offered. It contains a DOS-formatted floppy disk with BIOS upgrade file and upgrade utilities e.g. to reflect extended hardware support. For installation information, refer to the README file provided on the floppy disk.

BIOS Messages

The following messages may be displayed, e.g. if your system fails after you made changes in the setup menus. If it is not possible to fix a problem with the help of this section, contact your local sales representative or FAE for further support.

Message	Explanation	Corrective Action
`nnnn Cache SRAM Passed`	*nnnn* is amount of system cache in KBytes successfully tested	None
`CD-ROM Drive Identified`	Autotyping identified CD-ROM Drive	None
`Diskette drive A error` `Diskette drive B error`	Drive A: or B: fails the BIOS POST disk tests. Drive is selected via setup but either not present or defect.	Check that drive is defined with proper disk type in Setup, that disk drive is attached correctly and that controller is enabled.
`Entering SETUP ...`	Starting set-up program	None
`Extended RAM Failed at offset:nnnn`	Extended memory not working or not configured properly at offset *nnnn*	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.
`nnnn Extended RAM Passed`	*nnnn* is amount of RAM in MBytes successfully tested.	None

Message	Explanation	Corrective Action
`Failing Bits:nnnn`	*nnnn* is a map of the bits at the RAM address (in system, extended or shadow memory) which failed the memory test. Each `1` (one) in the map indicates a failed bit.	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
	Fixed disk not working or not configured properly	Check if fixed disk is attached properly. Run setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`	Autotyping identified specified fixed disk.	None
`Incorrect Drive A type - run SETUP` `Incorrect Drive B type - run SETUP`	Type of floppy drive not correctly identified in setup	Check for correct floppy drive in setup.
`Keyboard controller error`	Keyboard controller failed test	Replace keyboard
`Keyboard error`	Keyboard not working	Check for correct keyboard connection.
`Keyboard error nnn`	BIOS discovered a stuck key and displays scan code *nn* for stuck key.	Replace keyboard, check for stuck keys.
`Operating system not found`	Operating system cannot be located on either drive A:or drive C:.	Enter setup and check if fixed disk and drive A: are properly identified.
`Parity Check 1 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.
`Parity Check 2 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.

Message	Explanation	Corrective Action
`Press <F1> to resume, <F2> to set up`	Displayed after any recoverable error message	Press <F1> to start boot process or <F2> to enter setup and change any settings.
`Previous boot incomplete - Default configuration used`	Previous POST did not complete successfully. POST loads default values and offers to run setup. If failure was caused by incorrect values and they are not corrected, the next boot will likely fail.	Run setup to restore original configuration. This error is cleared the next time the system is booted.
`Real time clock error`	Real-time clock fails BIOS test.	May require board repair
`Resource allocation conflict on motherboard - Run Configuration Utility`	Possible interrupt or interface resource conflict.	Run ISA or EISA Configuration Utility to resolve resource conflict.
`Shadow RAM Failed at offset:nnnn`	Shadow RAM failed at offset *nnnn* of the 64k block at which error was detected.	Contact your local sales representative or FAE for further support.
`nnnn Shadow RAM Passed`	*nnnn* is amount of shadow RAM in KBytes successfully tested.	None
`System battery is dead - Replace and run SETUP`	The NVRAM (CMOS) clock battery indicator shows the battery is dead.	Replace battery and run setup to reconfigure system.
`System BIOS shadowed`	System BIOS copied to shadow RAM	None
`System cache error - Cache disabled`	RAM cache failed BIOS test. BIOS disabled cache.	Contact your local sales representative or FAE for further support.
`System CMOS checksum bad - run SETUP`	System NVRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS).	Run setup and reconfigure system either by getting default values and / or making your own selections.

Message	Explanation	Corrective Action
`System RAM Failed at offset:nnnn`	System RAM failed at offset *nnnn* in the 64k block at which the error was detected.	Check for correct memory modules. Otherwise contact your local sales representative or FAE for further support.
`nnnn System RAM Passed`	*nnnn* is amount of system RAM in KBytes successfully tested.	None
`System timer error`	Timer test failed.	Requires repair of system board.
`UMB upper limit segment address:nnnn`	Address *nnnn* of the upper limit of upper memory blocks indicates released segments of BIOS which may be reclaimed by a virtual memory manager.	None
`Video BIOS shadowed`	Video BIOS successfully copied to shadow RAM.	None
`Invalid System Configuration Data – run configuration utility`		Enter setup and use advanced configuration option to reset configuration data (due to corrupted ESCD data).

5

Buses

Board Information I²C Bus

This serial bus uses the I²C serial protocol and contains a serial EEPROM free for application. The EEPROM has a size of 256 Bytes.

Table 8: *Devices on Module Information I²C Bus*

Device Name	Device Type	Function	Location	Address
BIB	24C04	Contains board information	Base board	$1010000X_2$
	24C02		Memory module	$1010011X_2$
MEEPROM3	24C02	Free for applications	Base board	$101001X0_2$

Note: In order to avoid malfunction, do not write any data to the BIB I2C EEPROM which contains board-specific information.

System Management Bus

This serial bus is used for the PC compatible serial devices which comply with the SMBus specification from Intel. Via the temperature sensores, the bus provides the CPU with status information on the following devices:

- Pentium II Mobile Module
- Hardware monitor chip W83781D
- One SPD serial EEPROM for the first and second memory bank

If the memory module is installed, two SPD serial EEPROMs on the module are visible on this bus as well. They contain information for memory banks two to five. The SPD serial EEPROMs are built with the 24C02 version.

Table 9: *Devices on System Management I^2C Bus*

Device Name	Device Type	Function	Location	Address
SPDEEPROM1	24C02	Memory bank 0, 1 information	Base board	$1010000X_2$
SPDEEPROM2	24C02	Memory bank 2, 3 information	Memory module	$1010001X_2$
SPDEEPROM3	24C02	Memory bank 4, 5 information	Memory module	$1010010X_2$
TEMPSENSE1	MAX1617	Temperature sensor	Pentium II mobile module	$1001110X_2$
HWMON	W83781D	Hardware monitor chip	Base board	$0101101X_2$ [1)]

1)Power-on default value, can be altered via software

6

Maps and Registers

Overview

Following the block diagram for the PENT/CPCI-731, this section gives an overview of the I/O and memory maps and describes all PENT/CPCI-731 specific registers.

Table 10: *Register Overview*

Register	Description
Flag Register	page 6-25
Flash Control Register	page 6-8
General Purpose I/O Registers in Intel21150	page 6-28
Geographical Address Register	page 6-22
Hot Swap ENUM Register	page 6-23
I^2C Register	page 6-9
LED Control Register	page 6-24
Lock and Page Register	page 6-25
NMI Control Register	page 6-14
PCI Control Register	page 6-20
PCI Interrupt Control Register	page 6-21
Register on Page 1 overview	page 6-6
Register on Page 2 overview	page 6-6
Reset Control Register 1	page 6-11
Reset Control Register 2	page 6-12
Reset/NMI Status Register	page 6-15
Software NMI/Reset Register	page 6-16
Version Register	page 6-26
Watchdog Timer Register	page 6-18

I/O and Memory Maps

Table 11: *I/O Map*

I/O Address	Device		
	EIDE, PCI-to-ISA bridge		
		Keyboard, PS2 Mouse, COM1, COM2, LPT1, floppy	
0000_{16}…$001F_{16}$	x		DMA controller 1
0020_{16}...$003F_{16}$	x		Interrupt controller 1
0040_{16}...$005F_{16}$	x		Counter and timer
0060_{16}		x	Keyboard controller
0061_{16}	x		NMI status and control
0064_{16}		x	Keyboard controller
0070_{16}...0071_{16}	x		RTC and NMI mask
0080_{16}...$009F_{16}$	x		DMA page register
0100_{16}...$010F_{16}$		(x)	PENT/CPCI-731 specific register (partially implemented in separate FPGA)
$00A0_{16}$...$00BF_{16}$	x		Interrupt controller 2
$00C0_{16}$...$00DF_{16}$	x		DMA controller 2
$00E0_{16}$...$00FF_{16}$	n.a.	n.a.	Coprocessor
0170_{16}...0177_{16}	x		Secondary EIDE / ATAPI
$01F0_{16}$...$01F7_{16}$	x		Primary EIDE / ATAPI
0295_{16}...0296_{16}	n.a.	n.a.	Hardware monitor
$02F8_{16}$...$02FF_{16}$		x	COM2
$03BC_{16}$...$03BF_{16}$		x	LPT1
$03C0_{16}$...$03DA_{16}$	n.a.	n.a.	Graphic controller
$03F2_{16}$…$03F7_{16}$		x	Floppy EIDE / ATAPI
$03F8_{16}$…$03FF_{16}$		x	COM1

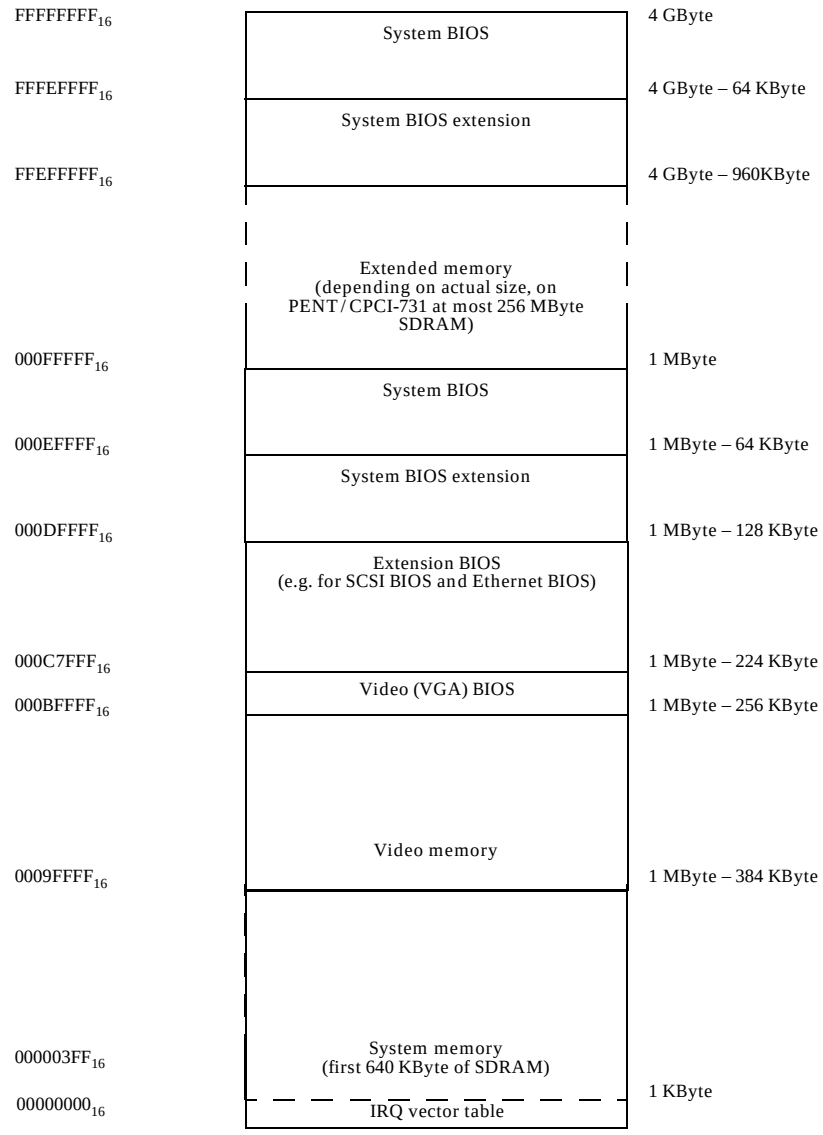


Figure 19: *Memory Map*

PENT/CPCI-731 Registers

Table 12: *Register on Page 1 Overview*

ISA-Bus Address	Register on Page 1	Comments
100_{16}	LED control register	1)
101_{16}	Reserved	1)
102_{16}	Reserved	1)
103_{16}	Flash control register	1)
104_{16}	Watchdog timer register	1)
105_{16}	Watchdog retrigger address	1)
106_{16}	Hot Swap ENUM register	1)
107_{16}	Geographical address register	1)
108_{16}	I^2C bus register	1)
109_{16}	Reset control register 1	1)
$10A_{16}$	Reset control register 2	1)
$10B_{16}$	NMI control register	1)
$10C_{16}$	Software NMI / Reset register	1)
$10D_{16}$h	Reset / NMI status register	1)
$10F_{16}$	FLAG register	1)

1)Register controlled by lock feature and locked after power-up

Table 13: *Register on Page 2 Overview*

ISA-BUS ADDRESS	Register on Page 2	Comment
103_{16}	PCI control register	1)
104_{16}	PCI interrupt control register	1)
$10F_{16}$	Version register	1)
$10E_{16}$	Lock and page register	2)

1)Register controlled by lock feature and locked after power up
2)Register not controlled by lock feature

ISA-Bus Decoding

The PCI-to-ISA bridge provides a 512 KByte or a 1 MByte address window to access the BIOS on the ISA-Bus. The FPGA allows the mapping of eight pages with a size of 512 KByte or four pages with a size of 1 MByte in the BIOS address range. Four 1 MByte flash devices are provided. The flash device selection is performed via register bits in the flash control register (see Table 14 “Flash Control Register” page 6-8). The address range is determined with the register bit RANGE.

The following figure gives an overview on the address mapping.

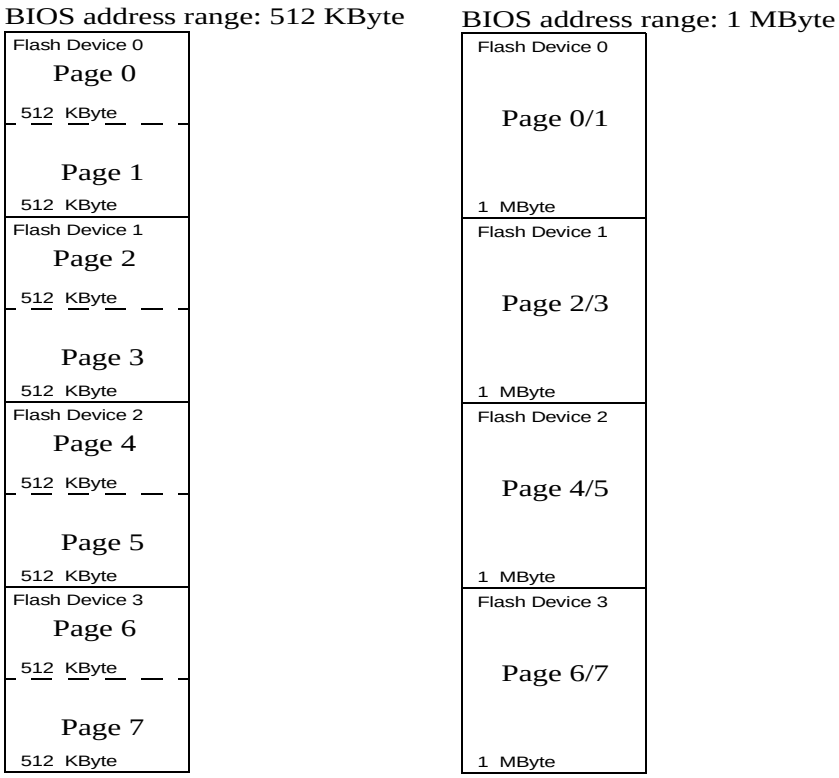


Figure 20: *Flash Device Address Mapping*

Flash Control Register

The flash device 0 programmed with the standard PC BIOS contains a write protected boot block area. The write protection can be enabled / disabled via switch SW1-2 (see “Switch Settings” page 2-15).

Table 14: *Flash Control Register*

Address: **0103 PAGE 1**

Bit	Value	Description	Access
2-0	FLASH_SEL_0, FLASH_SEL_1, FLASH_SEL_2	Selects flash device which is accessible in BIOS address range. 000_2 (default): Flash device 0 is selected 001_2: Flash device 1 is selected 010_2: Flash device 2 is selected 011_2: Flash device 3 selected 100_2: FPGA Initialization Flash is selected 101_2: reserved 110_2: reserved 111_2: reserved	r / w
3	RANGE	Selects flash address range between 512 Kbyte and 1 Mbyte. 0 (default): Address range is 512 Kbyte. 1: Address range is 1 MByte.	r / w
4	A19	Drives address line FLASH_A19 of selected flash devices directly. 0: Flash address line FLASH_A19 low. 1 (default): Flash address line FLASH_A19 high.	r / w
5	A20	Drives address line FLASH_A20 of flash devices directly. 0: Flash address line FLASH_A20 low 1 (default): Flash address line FLASH_A20 high	r / w
6	WE	Selects between write protect and write enable mode of flash memory devices. 0: Flash memory device write-protected 1 (default): Enabled for write access	r / w
7	INIT_REQ	Allows software caused reinitialization of FPGA. 0 (default): Reinitialization disabled 1: Starts reinitialization directly after write access	r / w

I^2C Register

The I^2C register is used for data transfer settings on the I^2C bus and provides access to the program-readable vintage registers for the base board and the memory modules.

Table 15: *I^2C Register*

Address: 0108_{16} PAGE 1			
Bit	**Value**	**Description**	**Access**
0	DIR	Specifies direction of data transfer. 0: Data is written to data line. 1(default): Data is read from data line.	r / w
1	SCLK	Serial Clock line of I^2C bus 0: Signal is driven low. 1 (default): Signal is driven high.	r / w
2	DATA_IN	Stores current value of data line.	r
7-3	Reserved		r / w

Reset

The reset logic supports a destructive / non-destructive board reset for every reset source. Non-destructive reset means that the contents of the main memory remains unchanged during the reset phase. The FPGA supports the following two different reset types:

a) Non-destructive reset

b) Destructive reset
Independent of all register settings, the signal BRG_S_RST_N causes in all cases a destructive reset if it is asserted via writing the reset register of the DEC 21554. This function is necessary to cause a destructive reset on a peripheral board in a system which does not allow an FPGA register access anymore or to reset a single slave board without resetting the whole CompactPCI bus. The PWR_FAIL_DET_N and WATCHDOG2 signals will also cause a destructive reset independent of all register settings.

NMI/Reset Sources

The following NMI/Reset sources and functions are implemented.

Table 16: *NMI/Reset Sources*

Signal Name	Function	Reset Maskable	Reset Type		NMI Maskable	Comments
			Destructive	Non Destructive		
CPCI_RST_N	CompactPCI bus reset	x	x	x	x	External source, bidirectional
CPCI_PBRST_N	CompactPCI bus push button reset	x	x	x	x	External source
RESET_IN_P5	Reset input from P5	x	x	x	x	
SWITCH_RESET_N	Front panel reset key	x	x	x	x	
BRG_S_RST_N	This signal is controlled by the RESET register of the PCI-to-PCI-bridge	-	x	-	-	External source, causes in any case a destructive reset
PWR_FAIL_DET_N	Power fail detection form power up CPLD	-	x	-	-	
WDOG_1_N	Watchdog 1	x	x	x	x	Internal source
WDOG_2_N	Watchdog 2	x	x	-	-	
SOFT	Software	x	x	x	x	
SB	PCI-to-ISA bridge	NA	NA	NA	NA	External source, causes only an NMI
RST_HW_MON_N	System control chip	NA	NA	NA	NA	External source, causes only an NMI

Reset Control Register

In the reset control register 1, the NMI / reset sources can be enabled / disabled to cause a reset. The Reset control register 2 determines the reset type (destructive / non-destructive). In the NMI control register, the NMI / Reset source can be enabled / disabled to cause an NMI.

Table 17: *Possible NMI/Reset Configurations*

Reset Mask Bit (Reset Configuration Register 1)	Reset Type Bit (Reset Configuration Register 2)	NMI Mask Bit (NMI Configuration Register)	NMI/Reset Source
1	-	1	Disabled
0	0	1	Causes destructive reset (default)
0	1	1	Causes non-destructive reset
1	-	0	Causes NMI
0	0	0	Causes NMI and after 1s destructive reset
0	1	0	Causes NMI and after 1 s non-destructive reset

Table 18: *Reset Control Register 1*

Address: 0109_{16} PAGE 1

Bit	Value	Description	Access
0	SWITCH_RST_MASK	Reset mask bit for front panel reset key. 0(default): Reset source enabled 1: Reset source disabled	r / w
1	RST_IN_P5_MASK	Reset mask bit for reset input from P5 connector. 0 (default): Reset source enabled 1: Reset source disabled	r / w
2	CPCI_PRBST_MASK	Reset mask bit for CompactPCI bus push-button reset. 0: Reset source enabled 1 (default): Reset source disabled	r / w
3	CPCI_RST_MASK	Reset mask bit for CompactPCI bus reset. 0 (default): Reset source enabled 1: Reset source disabled	r / w

Table 18: *Reset Control Register 1 (cont.)*

Address: 0109_{16} PAGE 1

Bit	Value	Description	Access
4	WDOG1_RST_MASK	Reset mask bit for watchdog 1 reset. 0: Reset source enabled 1 (default): Reset source disabled	r/w
5	SOFT_RST_MASK	Reset mask bit for software reset. 0 (default): Reset source enabled 1: Reset source disabled	r/w
6	WDOG2_RST_MASK	Reset mask bit for watchdog 2 reset. 0: Reset source enabled 1 (default): Reset source disabled	r/w
7	Reserved		

Note: Invalid configuration if WDOG2_RST_MASK is enabled and WDOG1_RST_MASK is disabled.

Table 19: *Reset Control Register 2*

Address: $010A_{16}$ PAGE 1

Bit	Value	Description	Access
0	SWITCH_RST_TYPE	Specifies reset type. 0 (default): Reset source causes destructive reset. 1: Reset source causes non-destructive reset.	r/w
1	RST_IN_P5_TYPE	Specifies reset type of reset input from P5 connector. 0 (default): Reset source causes destructive reset. 1: Reset source causes non-destructive reset.	r/w
2	CPCI_PBRST_TYPE	Specifies reset type of CompactPCI bus push button reset. 0 (default): Reset source causes destructive reset. 1: Reset source causes non-destructive reset.	r/w
3	CPCI_RST_TYPE	Specifies reset type of CompactPCI bus reset. 0 (default): Reset source causes destructive reset. 1: Reset source causes non-destructive reset.	r/w

Table 19: *Reset Control Register 2 (cont.)*

Address: $010A_{16}$ PAGE 1			
Bit	**Value**	**Description**	**Access**
5-4	WDOG1_RST_TYPE_0, WDOG1_RST_TYPE_1	Specifies reset type of watchdog reset. 00_2 (default): Reset source causes destructive reset 01_2: Reset source causes non-destructive reset. $=10_2$: Reset source causes NMI $=11_{2:}$ reserved.	r / w
6	SOFT_RST_TYPE	Specifies reset type of software reset. 0 (default): Reset source causes destructive reset. 1: Reset source causes non-destructive reset.	r / w
7	Reserved		

NMI Control Register

Every reset source is configured via the NMI control register to cause an NMI before asserting the reset signals. In addition to the described reset sources, the PCI-to-ISA bridge and the hardware monitor chip may also cause an NMI. The PCI-to-ISA bridge NMI source is not maskable in the NMI control register. The time between the assertion of the CPU_NMI signal and the reset signals is fixed to 1 s.

Table 20: *NMI Control Register*

Address: $010B_{16}$ PAGE 1

Bit	Value	Description	Access
0	SWITCH_NMI_MASK	NMI mask bit for reset key 0: NMI enabled 1(default): NMI disabled	r / w
1	RST_IN_P5_NMI_ MASK	NMI mask bit for reset input of P5 connector 0: NMI enabled 1 (default): NMI disabled	r / w
2	CPCI_PB_NMI_MASK	NMI mask bit for CompactPCI bus push-button reset 0: NMI enabled 1 (default): NMI disabled	r / w
3	CPCI_NMI_MASK	NMI mask bit for CompactPCI bus reset 0: NMI enabled 1 (default): NMI disabled	r / w
4	WDOG_NMI_MASK	NMI mask bit for watchdog 0: NMI enabled 1 (default): NMI disabled	r / w
5	SOFT_NMI_MASK	NMI mask bit for software reset 0: NMI enabled 1 (default): NMI disabled	r / w
6	HW_MON_NMI_ MASK	NMI mask bit for Hardware Monitor Chip reset 0: NMI enabled 1 (default): NMI disabled	r / w
7		Reserved	

Reset/NMI Status Register

The Reset / NMI status register allows the software to find out which reset source has caused an NMI and / or a non-destructive reset and enables clearing all of its status bits via a write access to this register.

Table 21: *Reset/NMI Status Register*

Address:$010D_{16}$PAGE 1

Bit	Value	Description	Access
0	SWITCH_RST_STAT	Reset key has caused NMI and / or reset 0 (default): No NMI / reset 1: NMI / reset	r / w
1	RST_IN_P5_RST_ STAT	Reset input of P5 connector has caused NMI / reset 0 (default): No NMI / reset 1: NMI / reset	r / w
2	CPCI_PBRST_STAT	Indicates whether CompactPCI bus push-button reset caused NMI / reset 0 (default): No NMI / reset 1: NMI / reset	r / w
3	CPCI_RST_STAT	Indicates whether CompactPCI bus reset caused non-destructive reset 0 (default): No NMI / reset 1: NMI / reset	r / w
4	WDOG_RST_STAT	Indicates whether watchdog caused non-destructive reset 0 (default): No NMI / reset 1: NMI / reset	r / w
5	SOFT_RST_STAT	Indicates whether software caused non-destructive reset 0 (default): No NMI / reset 1: NMI / reset	r / w
6	SB_NMI_STAT	Indicates whether South Bridge caused NMI 0 (default): No NMI 1: NMI	r / w
7	HW_MON_NMI_ STAT	Indicates whether the hardware monitor chip caused an NMI 0 (default): No NMI 1: NMI	r / w

Software NMI/Reset Register

The software NMI/Reset can be caused by writing a magic byte to the Software NMI/Reset register.

Table 22: *Software NMI/Reset Register*

Address: $010C_{16}$ PAGE 1

Bit	Value	Description	Access
7-0	SWRST[7…0]	Write access can cause NMI/reset. 01010101_2: Reset source can cause an NMI/reset. $\neq 01010101_2$: No NMI/reset will be generated.	w

Watchdog Retrigger and Watchdog Timer

The watchdog can be configured according to "Possible NMI/Reset Configurations" page 6-11. The watchdog timer starts running if the WDG_RST_MASK bit in the reset control register 1 is set to 0. If not masked by the reset control register 1 watchdog 2 will assert a destructive reset one second after watchdog 1 has set an NMI. A write access to the I/O address 0105_{16} retriggers the watchdog timer when the watchdog is enabled. This must be done at least once in every period specified in the watchdog timer register to prevent a watchdog time out. The FPGA input clock signal FPGA_CLK33 with f=33.33MHz is used to implement the watchdog timer.

Table 23: *Watchdog Timer*

DIV [3..0] Bit (Watchdog Control Register	FPGA_CLK33 33.33 MHz == 30.00 ns	Watchdog Timer
0000_2	2^{13} = 8192	245.760 µs
0001_2	2^{14} = 16384	491.520 µs
0010_2	2^{15} = 32768	983.040 µs
0011_2	2^{16} = 65536	1.966 µs
0100_2	2^{17} = 131072	3.932 ms
0101_2	2^{18} = 262144	7.864 ms
0110_2	2^{19} = 524288	15.729 ms
0111_2	2^{20} = 1048576	31.457 ms
1000	2^{21} = 2097152	62.915 ms
1001_2	2^{22} = 4194304	0.126 s
1010_2	2^{23} = 8388608	0.252 s
1011_2	2^{24} = 16777216	0.503 s
1100_2	2^{25} = 33554432	1.007 s
1101_2	2^{26} = 67108864	2.013 s
1110_2	2^{27} = 134217728	4.027 s
1111_2	2^{28} = 268435465	8.053 s

Table 24: *Watchdog Timer Register*

Address:0104_{16}PAGE 1

Bit	Value	Description	Access
3-0	DIV[0...3]	Controls retrigger period of watchdog. Retrigger period is programmable from 245.760 us to 8.053 s in 16 steps. $= 0000_2$ == 245.760 us $= 0001_2$ == 491.520 us $= 0010_2$ == 983.040 us $= 0011_2$ == 1.966 ms $= 0100_2$ == 3.932 ms $= 0101_2$ == 7.864 ms $= 0110_2$ == 15.729 ms $= 0111_2$ == 31.457 ms $= 1000_2$ == 62.915 ms $= 1001_2$ == 0.126 s $= 1010_2$ == 0.252 s $= 1011_2$ == 0.503 s $= 1100_2$ == 1.007 s $= 1101_2$ == 2.013 s $= 1110_2$ == 4.027 s = 1111 == 8.053 s	r / w
7-4		Reserved	

PCI Configuration and Interrupt, Operating Modus

The PENT/CPCI-731 is configurable to operate in a normal peripheral board or in a special mode, the Interrupt and ENUM service mode.

Interrupt and ENUM Service Mode

In this mode, CompactPCI interrupts and ENUM signals are serviced and the CompactPCI reset signal is driven. The interrupt routing is configurable independent of the currently active mode.

Signal Direction

Via the PCI_DIR bit of the PCI control register, the PENT/CPCI-731 can be configured to cause or to receive CompactPCI interrupts, CompactPCI reset and Hot Swap CompactPCI ENUM. The inverted state of this bit is mirrored to the INT_LVT_DIR signal to control the direction of the CompactPCI signal buffer on the PENT/CPCI-731.

After power up, the CPCI_SYSEN_N signal is sampled and the state is written in the PCI_DIR register bit. A low signal state configures the board to provide the interrupt and ENUM service mode. A high signal state configures the board to operate as a normal peripheral board. The PCI_DIR bit can be overwritten by software after power up.

Table 25: *Signal Direction*

CompactPCI Signal	Interrupt and ENUM Service Mode	Configuration as Peripheral
Interrupts CPCI_INT[D...A]_N	Input	Output
Reset CPCI_RST_N	Output	Input
ENUM CPCI_ENUM_N	Input	Output

Interrupt Mask

Every CompactPCI interrupt is maskable via the INTx_MASK bit in the PCI Control register, x= A, B, C, D.

PCI Control Register

Table 26: *PCI Control Register*

Address: 0103_{16}PAGE 2

Bit	Value	Description	Access
0	INTD_MASK	0: CompactPCI bus interrupt is not masked (enable). 1 (default): CompactPCI bus interrupt is masked (disabled).	r/w
1	INTC_MASK	0: CompactPCI bus interrupt is not masked (enable). 1 (default): CompactPCI bus interrupt is masked (disabled).	r/w
2	INTB_MASK	0: CompactPCI bus interrupt is not masked (enable). 1 (default): CompactPCI bus interrupt is masked (disabled).	r/w
3	INTA_MASK	0: CompactPCI bus interrupt is not masked (enable). 1 (default): CompactPCI bus interrupt is masked (disabled).	r/w
4	PCI_DIR	Selects direction of CompactPCI bus interrupt, reset and ENUM signals. 0: Drives signal INT_LVT_DIR low. 1 (default): Drives signal INT_LVT_DIR high.	r/w
5	PCIDIR_MASK	Selects whether PCI_DIR bit is programmable via software or determined by CPCI_SYSEN_N signal. 0: PCI_DIR bit is determined by CPCI_SYSEN_N pin. 1 (default): User can write 0 or 1 to PCI_DIR bit to force Interrupt and ENUM service mode or normal non-host functionality.	r/w
7-6		Reserved	

PCI Interrupt Control Register

The interrupt routing from the CompactPCI to the local PCI bus, from the primary side of the PCI-to-PCI bridge to the CompactPCI and from the secondary side of the PCI-to-PCI bridge to the local PCI bus can be selected in the PCI interrupt control register.

Table 27: *PCI Interrupt Control Register*

Address: 0104_{16}PAGE 2

Bit	Value	Description	Access
1-0	PCI_INT [1...0]	Selects interrupt routing between CompactPCI bus and local bus. 002 (default): L_PCI_INTA_N is routed to CPCI_INTA_N. L_PCI_INTB_N is routed to CPCI_INTB_N. L_PCI_INTC_N is routed to CPCI_INTC_N. L_PCI_INTD_N is routed to CPCI_INTD_N. 012: L_PCI_INTA_N is routed to CPCI_INTB_N. L_PCI_INTB_N is routed to CPCI_INTC_N. L_PCI_INTC_N is routed to CPCI_INTD_N. L_PCI_INTD_N is routed to CPCI_INTA_N. 10_2: L_PCI_INTA_N is routed to CPCI_INTC_N. L_PCI_INTB_N is routed to CPCI_INTD_N. L_PCI_INTC_N is routed to CPCI_INTA_N. L_PCI_INTD_N is routed to CPCI_INTB_N. 11_2: L_PCI_INTA_N is routed to CPCI_INTD_N. L_PCI_INTB_N is routed to CPCI_INTA_N. L_PCI_INTC_N is routed to CPCI_INTB_N. L_PCI_INTD_N is routed to CPCI_INTC_N.	r / w
3-2	SEC_INT [1...0]	Selects interrupt routing between secondary interrupt of PCI-to-PCI bridge and local PCI-Bus. 00_2: BRG_S_INT_N is routed to L_PCI_INTA_N. 01_2: BRG_S_INT_N is routed to L_PCI_INTB_N. 10_2 (default): BRG_S_INT_N is routed to L_PCI_INTC_N. 11_2: BRG_S_INT_N is routed to L_PCI_INTD_N.	r / w
5-4	PRIM_INT [1…0]	Selects interrupt routing between secondary interrupt of PCI-to-PCI bridge and local PCI-Bus. 00_2 (default): BRG_P_INT_N is routed to CPCI_INTA_N. 01_2: BRG_P_INT_N is routed to CPCI_INTB_N. 10_2: BRG_P_INT_N is routed to CPCI_INTC_N. 11_2: BRG_P_INT_N is routed to CPCI_INTD_N.	r / w
7-6		Reserved	

Geographical Addressing and Rear Transition Module

The state of the CompactPCI Geographical Address signals CPCI_GA[4...0] and the Rear Transition Module Present signal TM_RPNT are readable via the geographical address register bits.

Geographical Address

The state of the geographical address lines CPCI_GA[4...0] is directly readable via the register bits GA[4...0] of the geographical address register.

Table 28: *Geographical Address Register*

Address: 0107_{16} PAGE 1

Bit	Value	Description	Access
4-0	GA[4…0]	Mirrors signal state of geographical address lines.	r
5	TM_PRNT	Mirrors signal state of Rear Transition Module Present signal TM_PRNT.	r
7-6		Reserved Set to 0	

Rear Transition Module Detection

The TM_PRNT signal indicates if a rear transition module is assembled or not behind the corresponding CompactPCI slot.

Table 29: *TM_PRNT Signal*

TM_PRNT	Status of the Rear Transition Module
Low	Present
High	Not present

Hot-Swap ENUM Register

The hot-swap ENUM register is used to detect the assertion of the hot-swap ENUM signal. The ENUM signal can either be polled via the register or the enumeration can cause an interrupt on level 11.

Table 30: *Hot-Swap ENUM Register*

Address: 0106_{16}PAGE 1

Bit	Value	Description	Access
0	ENUM	Shows logic level of CPCI_ENUM_R_N signal at CompactPCI backplane. 0: CPCI_ENUM_R_N signal is asserted. 1: CPCI_ENUM_R_N is not asserted.	r
1	MASK	Masks ENUM interrupt. 0 (default): ENUM interrupt masked 1: ENUM interrupt unmasked	r / w
2	IRQ	Reflects status of interrupt line. 0 (default): ISA-Bus IRQ is not asserted. 1: ISA-Bus IRQ level 11 is asserted	r / w
7-3		Reserved Set to 0	

LED Control Register

The FPGA controls two bicolor (red / green) LEDs. The LEDs are configurable as user LEDs and to show the primary and secondary IDE device access. LED 2 can be programmed as IDE-LED. User LED 2 has no effect in that case. The LED control register specifies the status of the LEDs. The BIOS activates the IDE-LED after booting.

Table 31: *LED Control Register*

Address: 0100_{16} Page 1

Bit	Value	Description	Access
1-0	1_LEDSTAT [1…0]	Specifies status of user LED on front panel. 00_2 (default): off 01_2: red 10_2: green 11_2: off	r / w
3-2	2_LEDSTAT [1…0]	Specifies status of user LED on front panel. Function of 2_LEDSTAT depends on configuration of IDE_LEDSTAT. 00_2 (default): off 01_2: red 10_2: green 11_2: off	r / w
5-4	IDE_LEDSTAT [1…0]	Specifies color and function of IDE access LED on front panel. 00_2 (default): off 01_2: Signals IDE activity red. 10_2: Signals IDE activity green. 11_2: reserved.	r / w
7-6		Reserved Set to 0	

Register Lock and Page Function

The Lock and Page register enables or disables read and write access to the registers which can be protected. The affected registers are listed in “PENT/CPCI-731 Registers” page 6-6.

The read-back value of a protected register is always FF_{16}, even the Lock/Unlock register is read as FF_{16}, but is write accessible.

Table 32: *Lock and Page Register*

Address: $010E_{16}$ Page Independent			
Bit	**Value**	**Description**	**Access**
2-0	B[2…0]	Specifies whether protectable registers are unlocked or locked. 010_2: Unlocks specific registers. $\neq 010_2$ (default): Locks specific registers.	r/w
3		Reserved	
4	PAGE	Sets access to registers located in Page 1 or Page 2. 0: Registers located in Page 1 are accessible. 1: Registers located in Page 2 are accessible.	r/w
7		Reserved	

Flag Register

Table 33: *Flag Register*

Address: $010F_{16}$ Page 1			
Bit	**Value**	**Description**	**Access**
0	FLAG	BIOS determines execution of full POST or whether to jump directly to external boot loader located in user flash. 0: Normal BIOS is carried out. 1: BIOS jumps to an external bootloader.	r/w
7-1		Reserved Set to 0	

Version Register

The version Register provides the version of the FPGA software in BCD code.

Table 34: *Version Register*

Address: $010F_{16}$ Page 2

Bit	Value	Description	Access
3-0	x[3…0]	The most significant four bits specify the first number of the version.	r / w
7-4	y [3…0]	The least significant four bits specify the second number of the version. The version can therefore be max. 99_d.	r / w

Spare Configuration Switches

Four additional configuration switches are connected to the FPGA. These switches are currently unused and are reserved for features in the future.

Table 35: *Configuration Switches*

Switch	Position	CONF_SW_x_N Signal State
SW3-x	Off	High
SW3-x	On	Low

PMC Slot Identification

The PMC slot identification mechanism is used to detect if a PCI bus compliant module (i.e. PMC) is plugged on one of the PMC module sockets. For the detect mechanism four signals (BUSMODE4-BUSMODE1) are used.

BUSMODE2, 3, and 4 is a signal group generated by the PMC host. Each PMC socket has one BUSMODE1 signal which is pulled high on the host side. BUSMODE2, 3, and 4 are fixed to a certain logic level (001_2) to indicate that the host board is capable of driving the PCI bus protocol. A module using the PCI bus protocol should drive the BUSMODE1 pin low to indicate the host that it is capable of driving the PCI bus protocol.

Note: The PENT/CPCI-731 accepts PMC modules which do not drive the BUSMODE1 pin low. Application software may use the described detect mechanism to verify if a PMC card is installed.

The BUSMODE1 signals of PMC slot 1 and 2 are connected to general purpose I/O pins of the PCI-to-PCI bridge. This bridge is used to connect the PMC slots to the local PCI bus of the PENT/CPCI-731. The general purpose I/O pins used to read the logic level of the BUSMODE1 signals must be configured as inputs (default setting). The general purpose registers are accessible via the PCI configuration space of the Intel21150 PCI-to-PCI chip.

Table 36: *Busmode/GPIO Routing*

General Purpose I/O Pin	GPIO0	GPEI1
PMC slots	2	1

Table 37: *General Purpose I/O Registers in Intel21150*

Base Address	I/O Offset	Function
Via PCI configuration space, Intel21150	0x65	GPIO Output Data register
	0x66	GPIO Output Enable Control register
	0x67	GPIO Input Data register

Hardware Monitor

The PENT/CPCI-731 contains a hardware monitor chip which monitors the local board temperatures and voltages. Temperatures are monitored via three temperature sensors located on top of the board.

The following voltages are monitored:

- +5V
- +3.3V
- +12V
- -12V
- +2.5V (the two voltages from the mobile module which are used for the clock reference)

Note: The maximum input voltage at the hardware monitor is 4.095V except the 5V input. To measure the +/-12 voltages, the respective inputs are scaled with resistors. Software which sets up the hardware monitor must consider this scale.

Table 38: *Monitored Board Voltages versus Hardware Monitor Voltage Inputs*

Board Voltage	Voltage Input	Scale
+5V	+5VIN	1.0
Short to GND	-5VIN	None
+3.3V	+3.3VIN	1.0
+12V	+12VIN	0.26
-12V	-12VIN	-0.28
VCPUIO, 2.5V	VCOREA	1.0
VCLK, 2.5V	VCOREB	1.0

You can program thresholds for voltages and temperatures. If any voltage is out of the predefined range or the threshold temperature is reached, the chip generates an alarm (external system management interrupt, EXTSMI). The hardware monitor can be addressed either by using the system management bus (SMB) via the PCI-to-ISA bridge or directly via CPU I/O cycles at the ISA bus. The fan inputs (FANx) are disabled on the PENT/CPCI-731.

A software (Winbond Hardware Doctor) is available on the delivery CD-ROM. It initializes the hardware monitor chip and provides a user interface under WinNT. The thresholds can be set and events can be masked or enabled for generating alarm. For further information on the use of this software refer to the README file on the CD-ROM.

Table 39: *Hardware Monitor Base Address*

Base Address	PCI-to-ISA Chip select	Used Bus
295_{16},296_{16}	1	ISA
0101101_{2}	None	SMB

A

Appendix

Troubleshooting

A typical CompactPCI system is highly sophisticated. This chapter can be taken as a hint list for detecting erroneous system configurations and strange behaviors.It cannot replace a serious and sophisticated pre- and post- sales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or FAE for further support.

Problem	Possible Reason	Solution
Application software does not work	Memory ranges of system and peripheral boards do not match	Change application software so that memory ranges match I/O cards and host.
	Not enough disk capacity on mass storage device	Add disk capacity
	Not enough system memory	Add system memory
	Used I/O ranges do not match	Change application software so that I/O ranges match I/O cards and host.
Board does not boot	Boot device is not partitioned according to used operating system	Check partition according to the operating system's needs.
	Boot sequence not correct	Correct the boot sequence
	Interrupts are not set correctly	Set interrupts correctly
	Memory's timing parameters in firmware are outside specified ranges of used memory type	Set timing parameters correctly if configurable
	Wrong configuration of boot devices	Configure boot devices correctly
Board does not work	Backplane defect	1. Check CompactPCI slot position to be used for bent or broken pins 2. Replace damaged backplane.
	Backplane voltages wrong or missing	1. Check that all backplane voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads

Problem	Possible Reason	Solution
	Board connected to wrong slot	Connect system boards to system slots only. System slots are marked with a triangle around the slot number. Connect peripheral boards to I/O slots only. I/O slots are marked with a circle around the slot number.
	Board defect	Replace board
	Cables not connected	Connect all cables
	Cables connected to wrong connector	Check if plug fits into connector. Reconnect all cables to right connectors.
	Damaged plugs, bent or broken pins	Replace board
Board functions do not work	Functions are disabled	Configure board correctly
Board runs unstable	Disregard of environmental requirements	1. Check that temperature inside system stays within specified ranges for all system devices 2. Check for hot-spots within system. Improve cooling system if necessary. 3. Check that other environmental values like moisture or altitude are kept within specified ranges
Connected devices do not work	Backplane voltages for device not within the specified range	1. Check that all backplane voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads
	Device defect	Replace device
	Device not connected to power supply	Connect device to power supply
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective device
Devices collide with each other	Devices might have been moved to wrong address location	Configure board / devices correctly
Low system performance	Caches are disabled	Enable caches
Memory / PMC Module does not work	Module defect	Replace module

Problem	Possible Reason	Solution
	Module not defined for the used board	1. Check if module specification match with interface specification of board. 2. Replace module if specifications do not match
	Module not installed correctly	Check if module fits perfectly in socket.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective module
Operating system runs unstable	Drivers are missing, faulty or do not match hardware	1. Check that all used hardware parts have a driver matching the hardware 2. Reinstall hardware drivers
RTB does not work	RTB defect	Replace RTB
	RTB installed on wrong slot position	Install RTB on adjacent slot position of the used board.
	RTB not defined for the used peripheral or system board	Install RTB defined for the used peripheral or system board.

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Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

☞ Send this report to the nearest Force Computers headquarter listed on the address page.