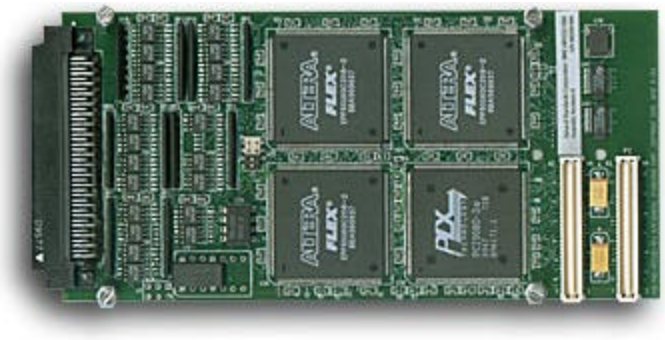
General Standards Corporation

High Performance Bus Interface Solutions

PMC-HPDI32A-ASYNC

High-speed Parallel Digital I/O PCI Board

100 to 200 Mbytes/s Cable I/O with PCI-DMA engine



Features Include:

- 100 Mbytes per second (max) input transfer rate via the front panel connector (RS422/485 differential I/O transceivers)
- Data rate of 5.0 megabits per second
- 8 Bits transmitter. LSB First.
- Software Selectable Even / Odd Parity.
- Software Selectable No Parity Bit Option.
- Software Selectable 1 or 2 stop bits.
- Software Selectable Big / Little Endian.
- Software Selectable 8 bit Tx / Rx FIFO size.
- Software Programmable gap between bytes transmitted.
- Software Programmable Message Length counters.
- Separate Transmit Data and Receive Data Lines.
- Software Selectable ability to Swap Transmit Data and Receive Data.
- Software Selectable ability to connect Transmit Data to Receive Data, for self-test loop back without requiring an external loop back cable.
- Typical 128K byte Transmit FIFO.
- Typical 128K byte Receive FIFO.
- 32 General Purpose I/O Lines

Applications Include:

- ✓ High speed data acquisition and control
- ✓ Point-to-Point PCI-to-PCI bus communication
- ✓ High-speed video data capture
- ✓ General Purpose Parallel DMA interface
- ✓ Development and research

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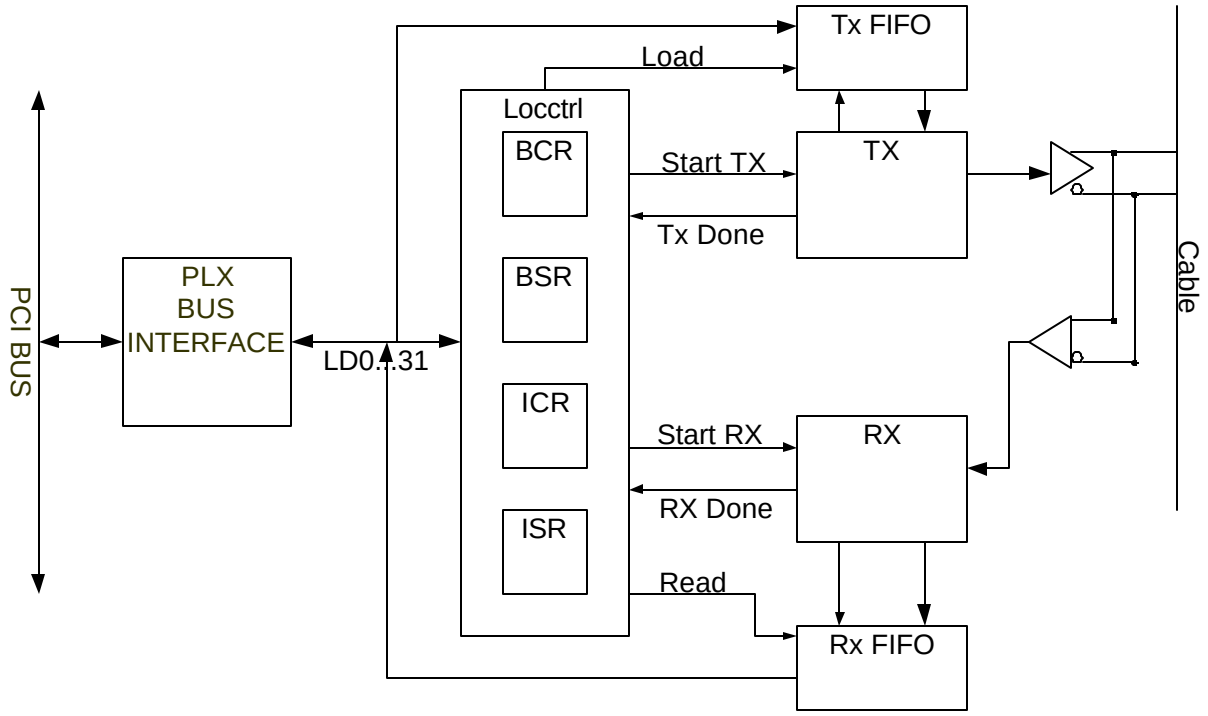
Functional Description:

The PMC-HPDI32A-ASYNC Board includes a DMA Controller, 64/128/256/512 Kbytes of FIFO buffering, a cable Transmit controller, a cable Receive controller, and cable transceivers (RS-422/485 or differential pseudo ECL). The DMA on this board is intended for reading and writing the FIFOs. After the DMA is initialized and started, the host CPU will be free to proceed with other duties and need to respond only to interrupts. The DMA controller is capable of transferring data to host memory using D32 transfers; whereas the FIFO memory provides a means for continuous transmission of data without interrupting the DMA or requiring intervention from the host CPU. The board also provides for DMA chaining, interrupt generation for various states of the board, including End-Of-Transfer, TX FIFO Almost Empty, RX FIFO Almost Full, and more. The Transmitter and Receiver are in FPGAs that provide a configurable interface that is highly flexible in data width and transfer protocol.



High Performance Architecture:

The board is designed for the highest performance level using conventional (and moderately priced) components. The PCI-DMA engine is designed to require minimal intervention from the host; it provides for high-speed transfers between the FIFO and PCI memory using DMA instructions stored in RAM. Data is transferred from the cable to the FIFO using a high-speed dedicated I/O controller.

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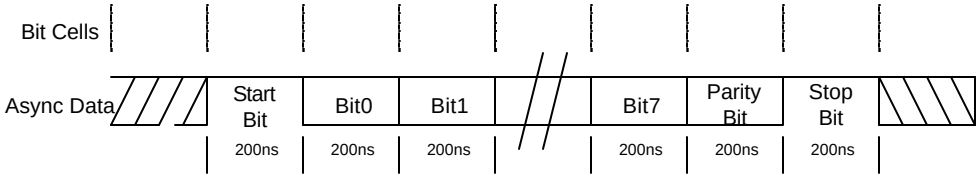
A Basic Serial Transfer:

Figure -1 Basic Serial Transfer



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SPECIFICATIONS

DMA Transfer Rates

- Transfer Rate over cable (RS-422/485 Transceivers):
  100 Mbytes/sec at 25 MHz clock rate and 32-bit cable interface.
- Transfer Rate over cable (Differential Pseudo ECL Transceivers):
  200 Mbytes/sec (max)
- PCI transfer rate from on-board FIFO to PCI:
  132 Mbytes/sec max (100 Mbytes/sec typ)
- Data transfers over the cable do not interrupt data transfers over PCI since data is decoupled using FIFO buffering.

DMA Start Latency (when started by cable input or by CPU)

Initialization and DMA start: less than 1 microsecond typ.

FIFO Memory

The FIFOs on the PMC-HPDI32A are used for buffering the transmit or receive data. There is a total of eight FIFOs on the board; 1 set of 4 for transmit, and 1 set of 4 for receive. Each set consists of 32 bits of data and 4 status flags. The receive FIFOs are loaded by the cable receive control logic and read by either the CPU or the DMA.

The transmit FIFOs are loaded by either the CPU or the DMA and read by the cable transmit control logic. The 4 status flags that accompany the FIFOs are all active low ('0' being TRUE) and are as follows: Empty, Almost Empty, Almost Full, Full. The Almost Empty and the Almost Full status flags can be programmed by the software to become true at most desired levels.

Cable Interface Transceivers

RS-422/485 levels (contact factory for availability of TTL levels)

RS-422/485 transceivers provide +- 7.5 Volts of noise immunity and can withstand +- 25 Volt transients without damage.
Optional on-board parallel termination. The parallel terminators provide the usual transmission line termination. In either case unused inputs can be left open; however, the logic level of unconnected inputs is indeterminate.

Pseudo ECL levels (option) is realized using Lucent BTK1A16NB differential pseudo ECL to/from TTL transceivers. The transceiver has a high output driver for up to 50 ohm loads. The driver outputs are

terminated internally at 220 ohms and the inputs are terminated at 110 ohms eliminating the need for external resistors. For more information refer to www.lucent.com and search on the above part number.

PCI INTERFACE

❑ **Compatibility:** Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Single multifunction interrupt.
Supports DMA transfers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ **Power Requirements**

+5.0 VDC ±0.20 VDC at 4.5 Amps, maximum

❑ **Physical Dimensions (Excluding panel bracket)**

Height:	98 mm
Length:	175 mm
Width:	6.1 mm

❑ **Environmental Specifications**

Ambient Temperature Range:	Operating: 0 to +55 degrees Celsius Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.

❑ **Cooling Requirements**

200 LFPM minimum air flow across component side of board;

ORDERING INFORMATION

Specify the basic product model number (PMC-HPDI32A-XXXK), where "X" is an option code as indicated below. For example, model number PMC-HPDI32A-256K describes a board with a total of 256Kbytes of FIFO buffering.

Other Examples Follow:

PMC-HPDI32A-ASYNC-64K with 8K x 32-bit FIFOs on each channel (both Tx & Rx, 64K byte total);
PMC-HPDI32A- ASYNC 256K with 32K x 32-bit FIFOs on each channel (both Tx & Rx, 256K byte total);
PMC-HPDI32A- ASYNC 512K with 64K x 32-bit FIFOs on each channel (both Tx & Rx, 512K byte total);
PMC-HPDI32A- ASYNC 1M with 128K x 32-bit FIFOs on each channel (both Tx & Rx, 1M byte total);

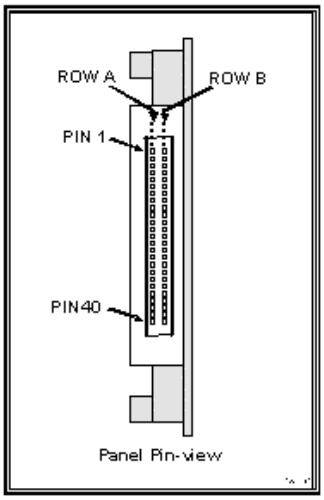
Differential ECL cable transceiver version:

PMC-HPDI32A- ASYNC 64K-ECL with 8Kx32-bit FIFOs on each channel, (both Tx & Rx,64K bytes total);
PMC-HPDI32A- ASYNC 256K-ECL with 32Kx32-bit FIFOs on each channel, (both Tx & Rx,256K byte total);
PMC-HPDI32A- ASYNC 512K-ECL with 64Kx32-bit FIFOs on each channel, (both Tx & Rx,512K byte total);
PMC-HPDI32A- ASYNC 1M-ECL with 128Kx32-bit FIFOs on each channel (both Tx & Rx, 1M byte total);

SYSTEM I/O CONNECTIONS

System Connector Pin Functions

Pin No.	Cable Signal Name	Pin No.	Cable Signal Name
1	CABLE CLK +	41	CABLE D12 +
2	CABLE CLK -	42	CABLE D12 -
3	CABLE COMMAND D0 +	43	CABLE D13 +
4	CABLE COMMAND D0 -	44	CABLE D13 -
5	CABLE COMMAND D1 +	45	CABLE D14 +
6	CABLE COMMAND D1 -	46	CABLE D14 -
7	CABLE COMMAND D2 +	47	CABLE D15 +
8	CABLE COMMAND D2 -	48	CABLE D15 -
9	CABLE COMMAND D3 +	49	CABLE D16 +
10	CABLE COMMAND D3 -	50	CABLE D16 -
11	CABLE COMMAND D4 +	51	CABLE D17 +
12	CABLE COMMAND D4 -	52	CABLE D17 -
13	CABLE COMMAND D5 +	53	CABLE D18 +
14	CABLE COMMAND D5 -	54	CABLE D18 -
15	CABLE COMMAND D6 +	55	CABLE D19 +
16	CABLE COMMAND D6 -	56	CABLE D19 -
17	CABLE D0 +	57	CABLE D20 +
18	CABLE D0 -	58	CABLE D20 -
19	CABLE D1 +	59	CABLE D21 +
20	CABLE D1 -	60	CABLE D21 -
21	CABLE D2 +	61	CABLE D22 +
22	CABLE D2 -	62	CABLE D22 +
23	CABLE D3 +	63	CABLE D23+
24	CABLE D3 -	64	CABLE D23 -
25	CABLE D4 +	65	CABLE D24 +
26	CABLE D4 -	66	CABLE D24 -
27	CABLE D5 +	67	CABLE D25 +
28	CABLE D5 -	68	CABLE D25 -
29	CABLE D6 +	69	CABLE D26 +
30	CABLE D6 -	70	CABLE D26 -
31	CABLE D7 +	71	CABLE D27 +
32	CABLE D7 -	72	CABLE D27 -
33	CABLE D8 +	73	CABLE D28 +
34	CABLE D8 -	74	CABLE D28 -
35	CABLE D9 +	75	CABLE D29 +
36	CABLE D9 -	76	CABLE D29 -
37	CABLE D10 +	77	CABLE D30 +
38	CABLE D10 -	78	CABLE D30 -
39	CABLE D11 +	79	CABLE D31 +
40	CABLE D11 -	80	CABLE D31 -



System Mating Connector:
Robinson Nugent # P50E-080-S-TG

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