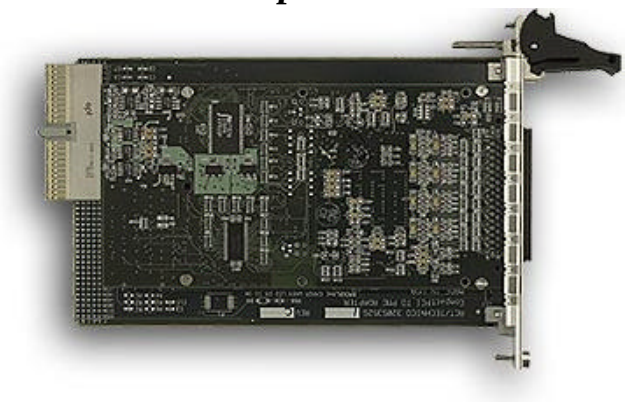
General Standards Corporation

High Performance Bus Interface Solutions

CPCI-12AIO

12-Bit Analog Input/Output CPCI Board

With 32 Input Channels, 4 Output Channels, a 16-Bit Digital I/O Port and 1.5 MSPS Input Conversion Rate



Features:

- 32 Single-Ended or 16 Differential 12-Bit Scanned Analog Input Channels
- 4 Analog Output Channels, 12-Bit D/A Converter per Channel
- 16-Bit Bi-directional Digital Port with Two Auxiliary I/O Lines
- Software-Selectable Analog Input/Output Ranges of ±10V, ±5V or ±2.5V
- Independent 32K-Sample Analog Input and Output FIFO Buffers?
- 1.5 MSPS Conversion Rate in Single-Channel Mode; 1.0 MSPS in Multichannel Scan Mode
- Low Crosstalk, Noise and Input Bias Current; Buffer Amplifiers on all Analog Input Lines
- 1.2 MSPS (Mega samples per Second) Aggregate Analog Output Clocking Rate (0.3 MSPS/Chan)
- Supports Waveform and Arbitrary Function Generation; Continuous and One-shot Modes
- Internal Rate Generator Controls Input Sampling, Output Sampling, or Both Simultaneously
- Supports Multiboard Synchronization of Analog Inputs and Outputs
- Internal Auto calibration of Analog Input and Output Channels
- Continuous and Burst (One-Shot) Input and Output Modes
- DMA Engine Minimizes Host I/O Overhead

Applications Include:

- ✓ Data Acquisition Systems
- ✓ Industrial Robotics
- ✓ Software Controlled Voltage Sources
- ✓ Automatic Test Equipment
- ✓ Function and Waveform Generation
- ✓ Research Instrumentation

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Overview:

The CPCI-12AIO board provides cost effective high-speed 12-bit analog input/output resources on a standard single-width CPCI module. Four analog output channels can be updated either synchronously or asynchronously, and support waveform generation. The analog inputs are configurable as either 32 single-ended channels or as 16 differential channels, and can be scanned continuously or in bursts. Inputs and outputs have a common software-selected range of ±10V, ±5V, or ±2.5V, and are accessed through independent FIFO buffers. Internal autocalibration networks permit calibration to be performed without removing the board from the system. Software-controlled test configurations include a loopback mode for monitoring all analog output channels. A digital I/O port provides 16 bidirectional data lines and two auxiliary I/O lines.

Functional Description:

The CPCI-12AIO board contains four 12-Bit D/A converters, a 12-bit scanning A/D converter, and a 16-Bit bi-directional port with two auxiliary I/O lines. A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller (Figure 1). Gain and offset correction of the analog input and output channels is performed by calibration DAC's that are loaded with channel correction values during auto calibration

The analog inputs are software-configurable either as 32 single-ended channels or as 16 differential signal pairs. Buffer amplifiers on all input lines eliminate multiplexer input switching noise, and minimize crosstalk and input bias currents. A selftest switching network routes a precision reference to the A/D converter during auto calibration, and also provides loopback monitoring of all analog output channels. Analog input data accumulates in a 32K-sample buffer until retrieved by the PCI bus.

Each of the four analog output channels contains a dedicated 12-bit D/A converter, offset and gain calibration DAC's, and an output range control network. The board receives analog output data from the PCI bus through a 32K-sample FIFO buffer.

Analog input scanning can be synchronized to the analog output sample clock, or the inputs and outputs can be operated independently. Both the analog inputs and outputs can be synchronized externally, and a hardware output permits multiple boards to be synchronized together. An interrupt request can be generated in response to selected conditions, including the status of the analog input and output data buffers.

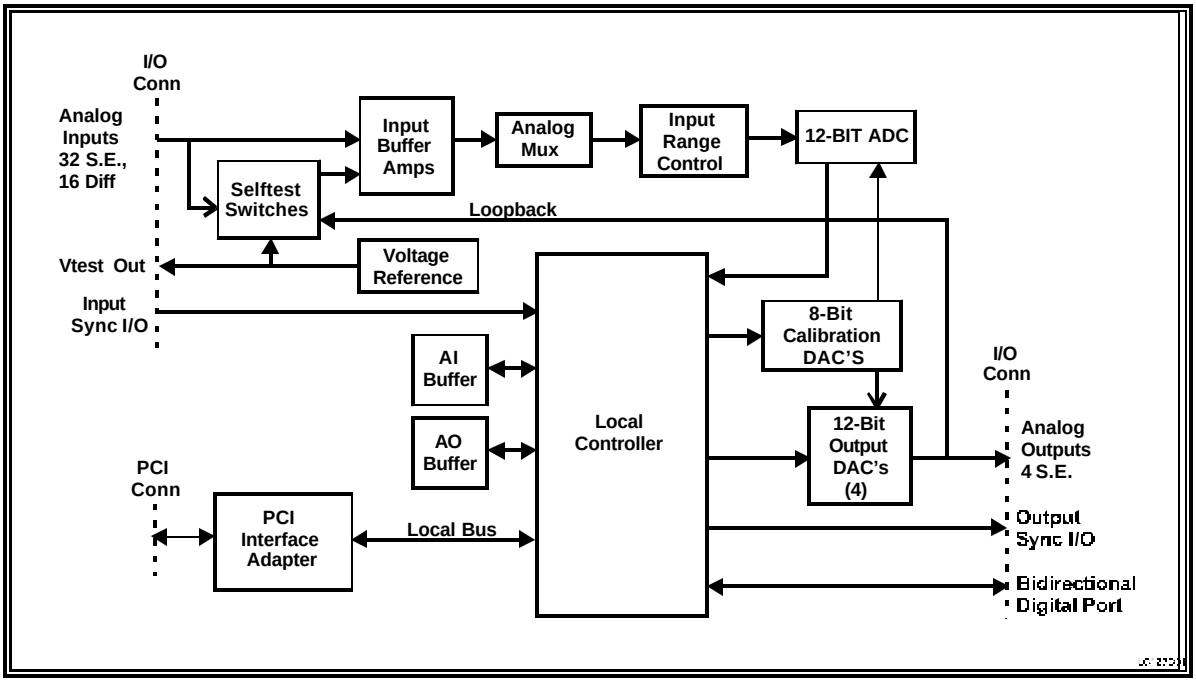

Figure 1. CPCI-12AIO; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and supports the "plug-n-play" initialization concept. System input/output connections are made at the panel bracket through a high-density 68-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

ANALOG INPUT CHANNELS

❑ Input Characteristics:

Configuration:	32 input lines, configurable as 32 single-ended or 16 differential channels
Voltage Ranges:	Software configurable as ±10, ±5 or ±2.5 Volts
Input Impedance:	1.0 Megohms line-to-ground, 2.0 Megohms line-to-line, in parallel with 100Pfd. Independent of scan rate.
Bias Current:	80 nanoamps maximum
Noise:	0.7 LSB-RMS typical
Common Mode Rejection:	60 dB typical, DC-60 Hz, differential input mode
Common Mode Range:	±10 Volts; differential input configuration
Overvoltage Protection:	Standard: ±30 Volts with power applied; ±15 Volts with power removed

❑ Transfer Characteristics:

Resolution:	12 Bits; 0.0244 percent of FSR
Maximum Conversion Rate:	1500K conversions per second, minimum in single-channel mode, 1000K in multichannel modes.
Channels per scan:	2, 4, 8, 16, or 32 Channels per scan (32 channels available only in single-ended mode)
Maximum Scan Rate:	250K scans per second in multiple-channel mode; 500 KSPS in 2Channel mode; 1500 KSPS in single-channel mode. Scan rate equals the conversion rate divided by the number of channels per scan.
Minimum Scan Rate:	400 scans per second, using a single internal rate generator; 0.006SPS using both generators. Zero, using a software sync flag or an externally supplied sync input.

DC Accuracy:
(Maximum composite error, referred to inputs)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±4.2mV	±8.4mV
±5V	±3.5mV	±5.2mV
±2.5V	±2.5mV	±4.0mV

Crosstalk Rejection:	75dB, DC-10kHz
Integral Nonlinearity:	±0.024 percent of FSR, maximum
Differential Nonlinearity:	±0.024 percent of FSR, maximum

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❑ **Analog Input Operating Modes and Controls**

Analog Input Modes:	Single Scan:	A software or hardware sync initiates a single scan of all active channels at the maximum conversion rate. As many as three target boards can be synchronized to a single initiator board.
	Continuous Scan:	Inputs are scanned continuously at the selected scan rate.
	Selftest:	Reference and loopback tests; autocalibration
	Multiple-Channel:	4, 8, 16 or 32 channels per scan
	Single-Channel:	Any single-channel can be selected for digitizing at the maximum conversion rate.
	Two-Channel:	2-Channel scan size.
Input Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported	

ANALOG OUTPUT CHANNELS

❑ Output Characteristics:

Configuration:	Four single-ended output channels. (Ordering option)
Voltage Ranges:	Same as selected for analog inputs; ±10, ±5 or ±2.5 Volts
Output Resistance:	1.0 Ohm, maximum
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to ±3ma per individual channel
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Noise:	2.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	5 nV-Sec typical, ±2.5V range

❑ **Transfer Characteristics:**

Resolution:	12 Bits (0.0244 percent of FSR)		
Output Sample Rate:	Software adjustable from 400SPS to 300KSPS per channel; 0.006SPS to 300KSPS using both internal rate generators. DC to 300KSPS with hardware or software sync.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±4.0mV	±7.5mV
	±5V	±3.1mV	±4.7mV
	±2.5V	±2.0mV	±3.5mV
Settling Time:	8us to 1LSB, typical with 50-percent fullscale step		
Crosstalk Rejection:	65 dB minimum, DC-1000Hz		
Integral Nonlinearity:	±0.025 percent of FSR, maximum		
Differential Nonlinearity:	±0.015 percent of FSR, maximum		

❑ Analog Output Operating Modes and Controls

Clocking Modes:	Simultaneous Continuous Mode: Channel values in a designated channel group are stored in an intermediate buffer, and then are transferred to the output DAC's when an output clock occurs. The clock can be generated either by the internal rate generator, by a software flag, or by an external hardware trigger. As many as three target boards can be clock-synchronized to a single initiator board. Simultaneous Burst Mode: A single function (i.e.: burst) is initiated by a software or hardware sync. During a burst, channel values in a designated channel group are stored in a transfer buffer, and then are transferred to the output DAC's each time a clock pulse is generated by the internal rate generator. The burst terminates when a Burst End flag is encountered Channel-Sequential Modes: Same as simultaneous modes, except each value in the data buffer is written immediately to the associated output DAC. The group-end flag is ignored in this mode.
Channel Assignment:	A 2-bit field in the output buffer assigns the associated data field to a specific output channel.
Group End:	A single bit in the output buffer indicates the last value in a channel group.
Burst End:	A single bit in the output buffer indicates the last value in an output burst sequence.
Output Data Buffer:	32K-sample FIFO with 0000h-7FFEh adjustable threshold flag; DMA is supported

RATE GENERATORS

Analog outputs and inputs can be clocked from either of two independent rate generators, or both inputs and outputs can be synchronized to a single generator. Each rate generator uses a 16-bit adjustable frequency divider, and the two generators can be operated in series to provide very low clocking rates.

DIGITAL I/O PORT

The digital I/O port consists of 16 bidirectional data lines, one auxiliary input line and one auxiliary output line. An interrupt request can be generated in response to the auxiliary input. The data lines are organized as two data bytes, each of which can be configured independently as either an input or output byte. Standard TTL logic levels apply, with 20 ma current-sink capability per output line.

AUTOCALIBRATION

A single control bit initiates Autocalibration. During autocalibration, analog input and output channels are calibrated to a single precision internal voltage reference. Analog output channels are active during autocalibration, which has a typical duration of two seconds.

PCI INTERFACE

❑ **Compatibility:**

Conforms to PCI Specification 2.2, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers as bus master.

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MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5VDC ±0.2 VDC at 1.3 Amps, maximum

Maximum Power Dissipation: 5.5 Watts, Side 1; 1.0 Watt, Side 2

❑ Physical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Optional EMI shield available for Side 1.

❑ Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +55 degrees Celsius Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-AB", as indicated below. For example, model number CPCI-12AIO-41 describes a board with 4 output channels, and with a bezel and EMI shield installed.

Optional Parameter	Value	Specify Option As:
Number of Analog Outputs	No Output Channels	A = 0
	4 Output Channels	A = 4
EMI Shield (Recommended in high-noise environments)	No bezel or shield	B = 0
	Bezel & shield installed	B = 1

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SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

P5 ROW-A		P5 ROW-B	
PIN	SIGNAL	PIN	SIGNAL
34	ANA INP00 HI	34	ANA OUT00
33	ANA INP00 LO *	33	OUTPUT RTN
32	ANA INP02 HI	32	ANA OUT01
31	ANA INP02 LO	31	OUTPUT RTN
30	ANA INP04 HI	30	ANA OUT02
29	ANA INP04 LO	29	OUTPUT RTN
28	ANA INP06 HI	28	ANA OUT03
27	ANA INP06 LO	27	OUTPUT RTN
26	ANA INP08 HI	26	VTEST
25	ANA INP08 LO	25	VTEST RTN
24	ANA INP10 HI	24	DIGITAL RTN
23	ANA INP10 LO	23	AUX DIGITAL IN
22	ANA INP12 HI	22	AUX DIGITAL OUT
21	ANA INP12 LO	21	DIG IO 00
20	ANA INP14 HI	20	DIG IO 01
19	ANA INP14 LO	19	DIG IO 02
18	INPUT RTN	18	DIG IO 03
17	INPUT RTN	17	DIG IO 04
16	ANA INP16 HI	16	DIG IO 05
15	ANA INP16 LO	15	DIG IO 06
14	ANA INP18 HI	14	DIG IO 07
13	ANA INP18 LO	13	DIG IO 08
12	ANA INP20 HI	12	DIG IO 09
11	ANA INP20 LO	11	DIG IO 10
10	ANA INP22 HI	10	DIG IO 11
9	ANA INP22 LO	9	DIG IO 12
8	ANA INP24 HI	8	DIG IO 13
7	ANA INP24 LO	7	DIG IO 14
6	ANA INP26 HI	6	DIG IO 15
5	ANA INP26 LO	5	DIGITAL RTN
4	ANA INP28 HI	4	SYNC OUTPUT
3	ANA INP28 LO	3	DIGITAL RTN
2	ANA INP30 HI	2	SYNC INPUT
1	ANA INP30 LO	1	DIGITAL RTN

* Analog inputs are shown for the differential input mode. In single-ended mode, LO inputs become consecutive odd-numbered channels, beginning with ANA INP 01 replacing ANA INP 00 LO.

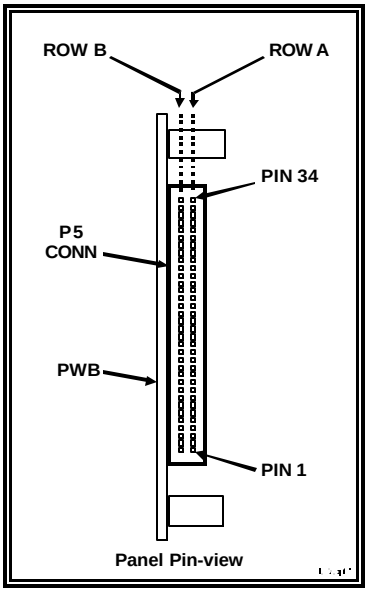

Figure 2. System Input/Output Connector

System Mating Connector:

68-Pin 2-row 0.050" dual-ribbon cable socket connector: Robinson Nugent #P50E-068-S-TG, or equivalent.

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