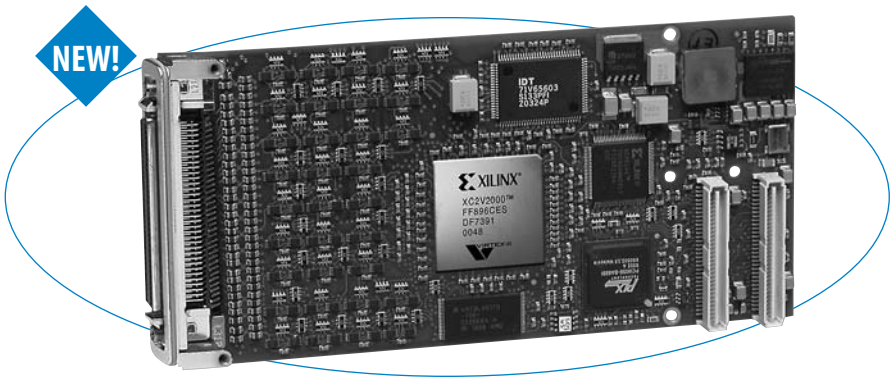
PMC-DX504/DX2004 Reconfigurable FPGA with LVDS I/O



Download your own logic programs and algorithms into the on-board user-configured FPGA to quickly create a custom digital I/O module.

- PMC-DX504: 32 LVDS I/O, 500K system gates
- PMC-DX2004: 32 LVDS I/O, 2M system gates

PMC-DX504 and PMC-DX2004 modules provide users with the capability to implement complex, customized digital I/O board solutions. Application-specific logic routines and algorithms can be downloaded into the on-board reconfigurable FPGA to control operation of the I/O channels.

These modules are ideal for advanced LVDS I/O functions. They support data rates of up to 200Mbps and clock rates up to 100MHz. Typical uses include hardware simulation, in-circuit diagnostics, and communication processing. Modules are able to generate recipe-based responses to input stimulus and to translate communication protocols.

Powerful and versatile, these PMC modules are designed around a reconfigurable FPGA, the Xilinx® Virtex®-II. The PMC-DX504 has the 500K-gate package, while the PMC-DX2004 uses the 2M-gate version. Both DSP-capable FPGAs feature versatile logic resources, large on-chip memories, and a high-speed interface.

The PCI bus interface is handled by a PLX® PCI 9056 device which provides 32-bit 66MHz bus mastering with dual-channel DMA support.

Features

- 32 bi-directional LVDS I/O channels
- Customizable FPGA with 500,000 or 2,000,000 gates (Xilinx Virtex-II XC2V500 or XC2V2000)
- FPGA code loads from PCI bus or flash memory
- Data rates of up to 200Mbps and clock rates up to 100MHz.
- 256K x 36-bit SRAM memory
- Supports dual DMA channel data transfer to CPU
- Supports both 5V and 3.3V signalling
- Extended temperature option (-40 to 85°C)

Specifications

FPGA

FPGA: Xilinx Virtex-II FPGA
PMC-DX504: XC2V500 FPGA with 500K system gates
PMC-DX2004: XC2V2000 FPGA with 2M system gates

FPGA configuration: Downloadable via PCI bus or from flash memory.

Input/output signals: 32 LVDS lines.

Example FPGA program: VHDL provided implements interface to PCI bus IC, interface to SRAM, PLL control, and digital I/O control. Program requires user proficiency with Xilinx software tools. See Engineering Design Kit.

LVDS I/O

I/O channel configuration: 32 LVDS I/O channels.

Differential input voltage (Q - $\overline{Q}$): 100mV minimum.

Output signal threshold with 100 ohms across Q & $\overline{Q}$:

High voltage for Q & $\overline{Q}$: 1.575V maximum.

Low voltage for Q & $\overline{Q}$: 0.925V minimum.

Differential voltage: 250mV minimum, 400mV maximum.

Maximum data rate: 200Mbps

Maximum clock rate: 100MHz

Meets or exceeds the TIA/EIA-644 Standard Compliant LVDS

Meets or exceeds the M-LVDS Standard TIA/EIA-899 for multipoint data exchange.

Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a PMC-DX module. See Page 54 for details.

PMC Compliance

Conforms to PCI Local Bus Specification, Revision 2.2 and CMC/PMC Specification, P1386.1.

Electrical/Mechanical Interface: Single-Width Module.

PCI bus clock frequency: 66MHz.

32-bit PCI Master: Implemented by PLX PCI 9056 device.

Signaling: 5V and 3.3V compliant.

Interrupts (INTA#): Interrupt A is used to request an interrupt.

Environmental

Operating temperature: 0 to 70°C or -40 to 85°C (E versions)

Storage temperature: -55 to 105°C.

Relative humidity: 5 to 95% non-condensing.

Power: Consult factory. Operates from 3.3V supply.

MTBF: Consult factory.

Ordering Information

PMC Modules

PMC-DX504: LVDS I/O module with 500K-gate FPGA

PMC-DX504E: PMC-DX504 with extended temp. range

PMC-DX2004: LVDS I/O module with 2M-gate FPGA

PMC-DX2004E: PMC-DX2004 with extended temp. range

PMC-DX-EDK: Engineering Design Kit (one kit required)

Software *(see Page 81)*

PMCSW-API-VXW: VxWorks® software support package

PCISW-API-QNX: QNX® software support package

PCISW-API-WIN: Windows® DLL software support

Accessories *(see Page 87)*

5028-432: Cable, shielded, SCSI-3 connector both ends