Third edition

68000 SINGLE BOARD SYSTEM

The GESSBS-6A 68000 Single Board System offers unique features available for the first time on single Euroboard format. Built around the 68000 16/32 bit CPU running at 8 MHz or 16 MHz, the module has 256 Kbytes of zero wait-state CMOS static RAM. A power fail logic with the addition of an external battery, protect the integrity of the data stored in CMOS static Ram. Four 32-pin JEDEC sockets allow up to 512 Kbytes of EPROM or 256 Kbytes of EPROM plus 256 Kbytes of static RAM. 8 Mbytes of external memory can be addressed by the GESSBS-6A allowing system RAM extension.

Two RS 232-C serial ports are available with an 8530 Serial Communications Controller chip. One channel supports asynchronous and synchronous protocols like monosync, IBM bisync, SDLC and HDLC. The second channel supports only asynchronous protocols.

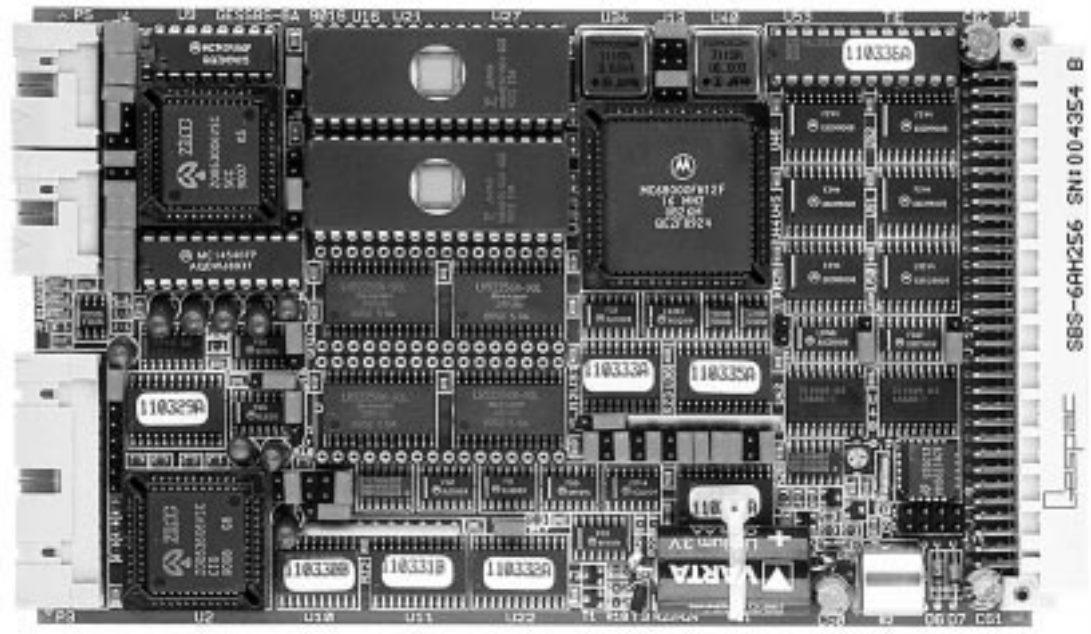
The GESSBS-6A includes two independent 8-bit bidirectional I/O ports and three independent 16-bit counter/timers (8536 CIO chip). A Real-Time-Clock Calendar (NS58274) with an on-board battery backup and Watch Dog circuit are implemented on the module.

The GESSBS-6A is fully compatible with the standard G-64 and G-96 Bus.

Technical features

- 16/32 bit architecture with 8/16 MHz 68000/68010 microprocessor
- 512 Kbytes of SRAM and 256 Kbytes of EPROM or 256 Kbytes of SRAM and 512 Kbytes of EPROM
- 1 Mbytes of EPROM optional
- 8 Mbytes of external memory addressing capability
- 256 Kbytes of CMOS static RAM are protected against the power fail
- Real-Time-Clock Calendar with on-board battery backup
- Two independent RS 232-C full-duplex serial channels
- One channel supports asynchronous and synchronous protocols and provides all signals necessary for a modem
- Programmable baud rates from 0 to 38400 Bauds (async) and from 0 to 800 Kbits/s (sync)
- Two 8-bit double buffered bidirectional I/O ports with four handshake lines.

  These ports can be linked to form a single 16-bit I/O port
- Three independent 16-bit counter/timers
- Two timers can be linked to form a 32-bit timer/counter
- Watch Dog circuit for program security
- Fully compatible G-64 and G-96 Bus
- Standard power supply : + 5 V (± 12 V optional)



Reference

GESSBS-6A: 68000 Single Board System

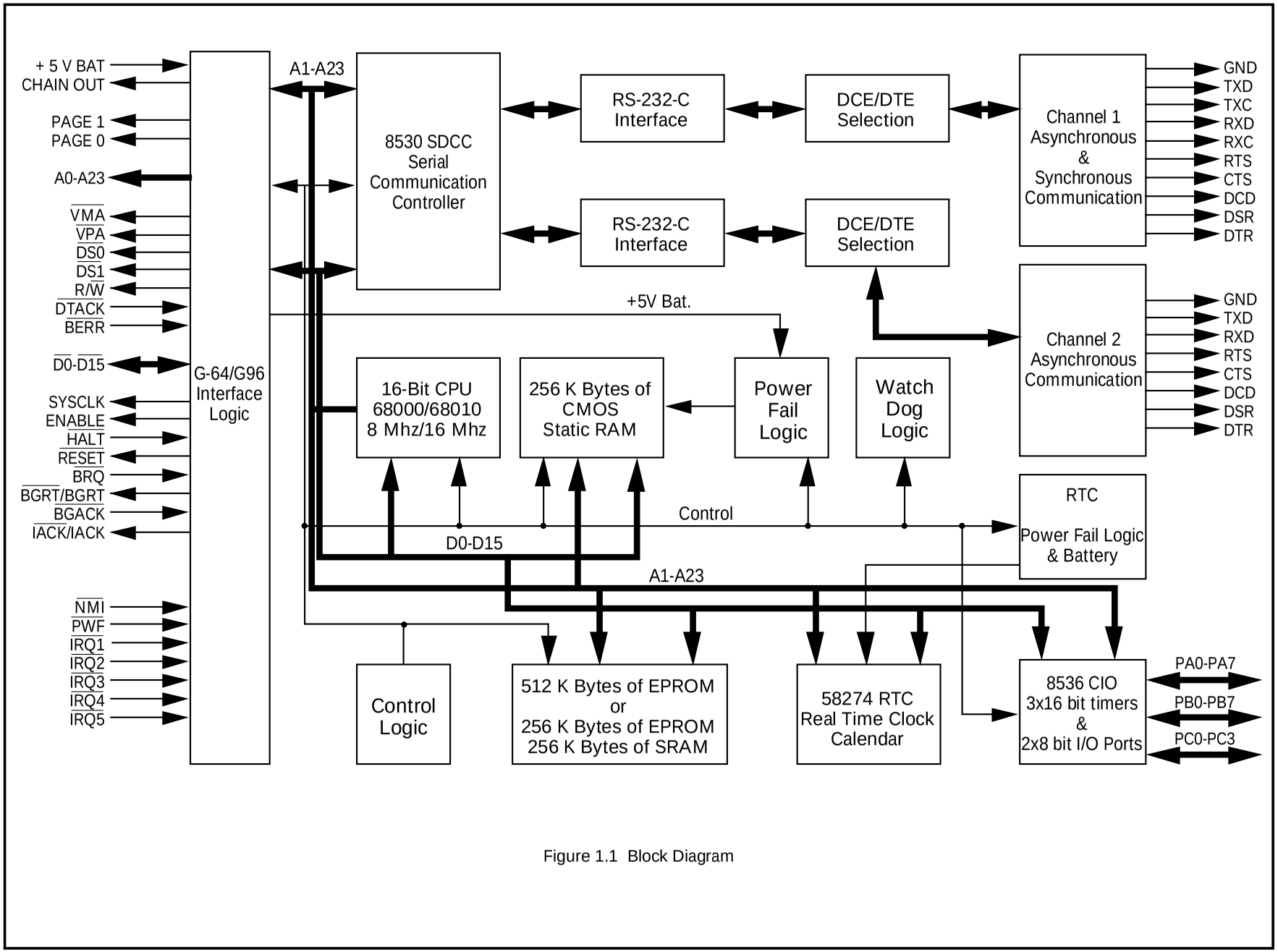


Figure 1.1 Block Diagram

1. GENERAL INFORMATION

1.1 DESCRIPTION

Using Surface Mounting Device and very high PCB technology, it has been possible to offer a complete 68000 system on a single Euroboard format.

The GESSBS-6A is built around the 68000 16/32 bit CPU running at 8 MHz or 16 MHz and has 256 Kbytes of zero wait-state CMOS static RAM. A power fail logic with the addition of an on-board battery, protect the integrity of data stored in the CMOS static RAM. Four 32-pin JEDEC sockets allow up to 512 Kbytes of EPROM or 256 Kbytes of EPROM plus 256 Kbytes of static RAM. The EPROM can operate at zero wait-sate (120 ns EPROM time access). 8 Mbytes of external asynchronous memory can be addressed by the GESSBS-6A allowing important system RAM extension.

Two RS 232-C serial channels are available with an 8530 SCC chip. One channel supports asynchronous and synchronous protocols like monosync, IBM bisync, SDLC and HDLC. This channel provides all the signals necessary for modem connection. The second channel supports only asynchronous protocols and allows terminal connection. The speed of transmission is independently programmable for each channels from 0 to 38400 Bauds for asynchronous protocols.

The module includes two independant 8-bit, double-buffered bidirectional I/O ports plus a 4-bit special-purpose I/O port (8536 CIO). The 8536 CIO features flexible pattern-recognition logic, four handshake modes (including 3-Wire like the IEEE-488). The two 8-bit I/O ports can be linked to form a single 16-bit I/O port.

The 8536 CIO provides three independant 16-bit counter/timers with up to four external command/control lines per counter/timer (count input, output, gate and trigger) and three output duty cycles (pulsed, one-shot and square wave), programmable as retriggerable or nonretriggerable. Two 16-bit counter/timers can be linked to form a 32-bit counter/timer.

A Real-Time-Clock Calendar (NS58274), with an on-board battery backup indicates time and date and can generate a programmable interrupt.

The module implements a "Watch Dog" function which can generate a reset or a level 7 interrupt.

Five interrupt bus lines (level 1 - level 5) are selectable to be vectored or autovectored. All the internal interrupts are on the level 6. Four interrupt sources can activate the level 7 : NMI bus line, PWF bus line, ABORT external switch and Watch Dog Fail signal. A status register contains the source of level 7 interrupt.

A control register permits selection of one of four possible memory maps.

Control lines for direct memory access operations (DMA) are accessible on the bus. Note that DMA operations can not be realized on the on-board local RAM. A timeout logic controls asynchronous operations when the transfer execution is not possible.

The GESSBS-6A is fully compatible with the standard G-64 and G-96 Bus. The block diagram of figure 1.1 illustrates the different parts of the module and their interconnections.

1.2 SPECIFICATIONS

Microprocessors :	68000
CPU clock :	8 MHz or 16 MHz
Data transfer :	8/16-bit, syn/asynchronous
Synchronous transfer :	1 MHz or 2 MHz Enable frequency clock
Timeout delay :	8 µs or 16 µs
Wait-states :	SRAM : 0 or 1 EPROM : 0, 1, 2 or 4
Addressing capability :	
Internal memory :	- 256 Kbytes of CMOS low power SRAM - 512 Kbytes of EPROM or 256 Kbytes of EPROM plus 256 Kbytes of SRAM or 1 Mbyte of EPROM
External memory :	8 Mbytes
External peripheral :	2 Kbytes (1 K x 16)
8530 clock input :	3.6864 MHz
Serial channel 1 :	8530 SCC channel A
Available protocols :	Asynchronous, monosync, IBM bisync, SDLC and HDLC
Interface :	RS 232-C compatible
Signals for modem :	Yes
Progr. data rates :	0-38400 Bauds (async) 0-800 Kbits/s (sync)
Channel configuration :	DCE or DTE
Serial channel 2 :	8530 SCC channel B
Available protocols :	Asynchronous
Interface :	RS 232-C compatible
Signals for modem :	No
Progr. data rates :	0-38400 Bauds (async)
Channel configuration :	DCE or DTE
Parallel communication :	Two 8-bit bouble-buffered bidirectional ports plus a 4-bit special purpose I/O port
Progr. timer features :	3 independent 16-bit timer/counters cascadable to form a 32-bit timer/counter Interrupt capability for each timer
Timer clock origin :	External or internal 2 MHz

RTC interrupt time intervals :	0.1, 0.5, 1, 5, 10, 30 and 60 sec
RTC functions :	Hours, minutes, seconds, day, month, year
Battery life time approx. :	15000 hours
Bus interface :	- Address bus : 3 states TTL compatible - Data bus : 3 states TTL compatible - Other signals : TTL compatible
Bus drivers :	48 mA device type
Power requirements :	+ 5 Vdc : 1.75 A typ*
Operating temperature :	+ 5° to + 55 C°
PCB dimensions :	100 x 160 mm

* Without U13 / U14 / U15 / U16 devices

Table 1.1 Specifications

1.3 MEMORY MAP

The GESSBS-6A module has been designed to work either on the G-64 or on the G-96 Bus. With the G-64 Bus, the external memory which can be added to the module is limited at 128 K x 16 (256 Kbytes). Nevertheless with the G-96 Bus, this limitation is fixed at 8 Mbytes allowing important system memory extension.

Addresses on the bus are considered as word addresses. The upper and lower bytes are selected by DS0 and DS1 bus lines. Therefore the address line A1 of the 68000 drives the A0 line on the bus.

The four possible memory maps generated by the GESSBS-6A module are shown in table 1.2.

CPU Byte address (hexadecimal)	BUS Word address (hexadecimal)	Field size	Physical address space
FFFFFF FC0000	Do not care	256 Kbytes[5]	Internals EPROM / SRAM U13, U14
FBFFFF F80000	Do not care	256 Kbytes[5]	Internals EPROM U15, U16
F7FFFF F40000	Do not care	256 Kbytes	Internal Low Power SRAM
			Not used
8207FF 820000	4103FF 410000	2 Kbytes[1]	Asynchronous External I/O[2]
			Reserved
81007F 810000	Do not care	64 Kbytes	Internal I/O[3]
			Reserved
8007FF 800000	4003FF 400000	2 Kbytes[1]	Synchronous External I/O[2]
7FFFFF 080000	3FFFFF 040000	7680 Kbytes	External Memory G-96 only
07FFFF 040000	03FFFF 020000	256 Kbytes	External Memory G-64 & G-96
03FFFF 000000	01FFFF 000000	256 Kbytes	Mapping 3[4] : MAP1 = 1, MAP0 = 1 External Memory G-64 & G-96
03FFFF 000000	Do not care	256 Kbytes	Mapping 2[4] : MAP1 = 1, MAP0 = 0 U13, U14 EPROM/ SRAM
03FFFF 000000	Do not care	256 Kbytes	Mapping 1[4] : MAP1 = 0, MAP0 = 1 Internal Low Power SRAM
03FFFF 000000	Do not care	256 Kbytes	Mapping 0[4] : MAP1 = 0, MAP0 = 0 Internal EPROM/ U15, U16

Table 1.2 Memory map

Notes: [1] External field is characterized on the bus by the VPA signal and A0-A9 address line.

[2] External I/O module allow access by word. If the I/O module is an 8-bit module, the high byte on D8-D15 bus lines is unused.

[3] Internal I/O are redundant, refer to § 1.3.1

[4] After power on or restart operation, this area is relocated in the internal EPROM field (mapping 0). Refer to § 1.4.

[5] 1 Mbyte EPROM version refer to § 2.18.

1.3.1 INTERNAL I/O MAP

The asynchronous address field allows the access of the internal peripheral devices: 8530 SCC, 8536 CIO, 58274 RTC and the control/status register.

The internal I/O field is redundant. Therefore, it is recommended to use the addresses that are shown in table 1.3 for software compatibility and running.

CPU Physical address	Access type	DEVICES
		Reserved
$810071	Byte	Level 7 interrupt control status register
$810069	Byte	Watchdog trigger register
		Reserved
$810061	Byte	Mapping control Register
		Reserved
$81005F $810041	Byte	58274 RTC
		Reserved
$810027 $810021	Byte	8530 SCC
		Reserved
$810007 $810001	Byte	8536 CIO

Table 1.3 Internal I/O map

1.4 MAPPING CONTROL REGISTER

After power on or restart operations, the area $000000 - $03FFFF is redundant with the internal EPROM field located at the addresses $F80000 - $FBFFFF.

The attribution of the address field $000000 - $03FFFF (256 Kbytes) is controlled by two bits (MAP1, MAP0) of the control register located at the address $810061 as shown in the figure 1.2. The table 1.4 shows how to select one of the four possible module mapping.

Address : $810061 (write only)

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	*	MAP1	MAP0

*Unused bits

Figure 1.2 Mapping control register

MAP1	MAP0	CPU Byte address	Redundant CPU byte address	Physical address space
0	0	$03FFFF $000000	$FBFFFF $F80000	Internal EPROM U15, U16
0	1	$03FFFF $000000	$F7FFFF $F40000	Internal Low Power SRAM
1	0	$03FFFF $000000	$FFFFFF $FC0000	Internal EPROM/ SRAM U13, U14
1	1	$03FFFF $000000	- - -	External memory

Notes: After power on or restart operations, MAP1 and MAP0 control bits are cleared

Table 1.4 Mapping selection

1.5 LEVEL 7 INTERRUPT CONTROL/STATUS REGISTER

Four interrupt sources are wired on the interrupt level 7 of the CPU : NMI bus line, PWF bus line, ABORT external switch signal and Watch Dog Fail signal. A Control/Status register located at address $810071 allows to know the source of this interrupt and after to clear it as described in figure 1.3.

Address : $810071 (read/write)

D7	D6	D5	D4	D3	D2	D1	D0
PWF	*	*	*	*	WDF	NMI	ABORT

*Unused bits

ABORT When set, this bit indicates that the external ABORT switch has been depressed. While this bit is a one, a non-maskable interrupt (level 7) is generated to the CPU

SET ABORT external switch depressed
CLEARED CPU writes a one

NMI When set, this bit indicates that a Non-Maskable Interrupt (NMI) request has occured on the G-64/G-96 Bus. While this bit is a one, a non-maskable interrupt (level 7) is generated to the CPU.

SET NMI bus line asserted low
CLEARED CPU writes a one

WDF When set, this bit indicates that the Watch Dog logic has generated an interrupt. While this bit is a one, a non-maskable interrupt (level 7) is generated to the CPU.

SET Watch Dog Fail signal asserted low
CLEARED CPU writes a one

PWF Power Failure Detected. This bit reflects the condition of the PWF bus line. This state is the logical complement of this line. While this bit is a one, a non-maskable interrupt (level 7) is generated to the CPU.

SET The power supply is defective
CLEARED CPU writes a one and the power supply is correct

Important notes :

- All these interrupts sources are latched on their falling edge.
- After power on or restart operation, before unmasking the interrupts, the interrupt control/status register must be initialized with the pattern 1XXXX111 by the CPU.

Figure 1.3 Interrupt Control/Status register

1.6 RESTART OPERATION

The RESET is an output signal generated by the GESSBS-6A module during power on, the software instruction «RESET» or by depressing the external Reset-switch.

The reset circuitry is made with the TI 7702 device which generates automatically a RESET signal during either the power-on sequence or when the power supply drops under the nominal voltage of 4.75 V typ. Thus, it is very important to ensure a correct + 5 V power supply.

1.7 8536 COUNTER/TIMER AND PARALLEL I/O UNIT

1.7.1 GENERAL DESCRIPTION

The 8536 CIO is a general-purpose peripheral circuit, satisfying most counter/timer and parallel I/O needs encountered in system designs. This versatile device contains three I/O ports and three counter/timers.

The features of the 8536 CIO are listed below :

- Two independent 8-bit, double-buffered, bidirectional I/O ports plus a 4-bit special-purpose I/O port. I/O ports feature programmable polarity, programmable direction (Bit mode), «pulse catchers» and programmable open-drain output.
- Four handshake modes, including 3-Wire (like the IEEE-488).
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers with up to four external access lines per counter/timer.

1.7.2 8536 REGISTERS

The 8536 CIO contains 45 registers which are not directly accessible by the CPU. Only four registers are directly accessible as shown in table 1.5.

Physical Address	Access	Register name
$810001	R/W	Port C's Data Register
$810003	R/W	Port B's Data Register
$810005	R/W	Port A's Data Register
$810007	R/W	Control Register

Table 1.5 8536 CIO directly accessible register map

The internal registers are accessed by the folowing two-step sequence :

First, write the address of the target register into the Control Register ; then read from or write to the target register by accessing the Control Register for the second time. Note that the data registers can be accessed by the same way but it is most useful to make a direct access of these registers.

Table 1.6 gives the target addresses of the 8536 CIO's registers.

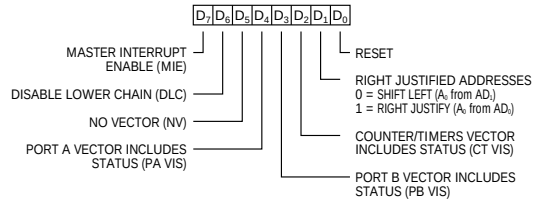
Target register address	Target register name
$00	Master Interrupt Control
$01	Master Configuration Control
$02	Port A's Interrupt Vector
$03	Port B's Interrupt Vector
$04	Counter/Timer's Interrupt Vector
$05	Port C's Data Path Polarity
$06	Port C's Data Direction
$07	Port C's Special I/O Control
$08	Port A's Command and Status
$09	Port B's Command and Status
$0A	Counter/Timer 1's Command and Status
$0B	Counter/Timer 2's Command and Status
$0C	Counter/Timer 3's Command and Status
$0D	Port A's Data*
$0E	Port B's Data*
$0F	Port C's Data*
$10	Counter/Timer 1's Current Count-MSB
$11	Counter/Timer 1's Current Count-LSB
$12	Counter/Timer 2's Current Count-MSB
$13	Counter/Timer 2's Current Count-LSB
$14	Counter/Timer 3's Current Count-MSB
$15	Counter/Timer 3's Current Count-LSB
$16	Counter/Timer 1's Time Constant MSB
$17	Counter/Timer 1's Time Constant LSB
$18	Counter/Timer 2's Time Constant MSB
$19	Counter/Timer 2's Time Constant LSB
$1A	Counter/Timer 3's Time Constant MSB
$1B	Counter/Timer 3's Time Constant LSB
$1C	Counter/Timer 1's Mode Specification
$1D	Counter/Timer 2's Mode Specification
$1E	Counter/Timer 3's Mode Specification
$1F	Current Vector
$20	Port A's Mode Specification
$21	Port A's Handshake Specification
$22	Port A's Data Path Polarity
$23	Port A's Data Direction
$24	Port A's Special I/O Control
$25	Port A's Pattern Polarity
$26	Port A's Pattern Transition
$27	Port A's Pattern Mask
$28	Port B's Mode Specification
$29	Port B's Handshake Specification
$2A	Port B's Data Path Polarity
$2B	Port B's Data Direction
$2C	Port B's Special I/O Control
$2D	Port B's Pattern Polarity
$2E	Port B's Pattern Transition
$2F	Port B's Pattern Mask

*Can be accessed directly

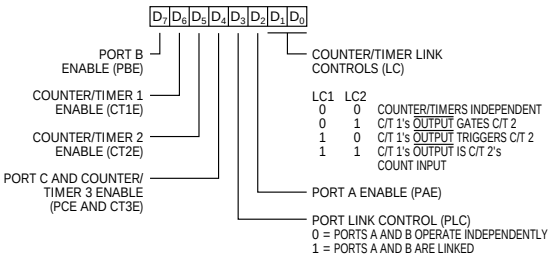
Table 1.6 8536 CIO indirectly accessible register map

The figure 1.4 describes the contents of the 8536 CIO registers. *For more information regarding 8536 register promming, please refer to the "Z8036/Z8536 CIO Counter/Timer and Parallel I/O Unit tecchnical manual" from Zilog.*

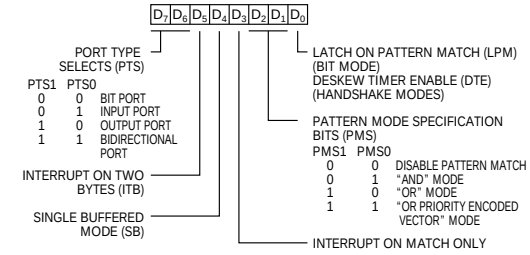
Master Interrupt Control Register
Address : 000000
(Read/Write)



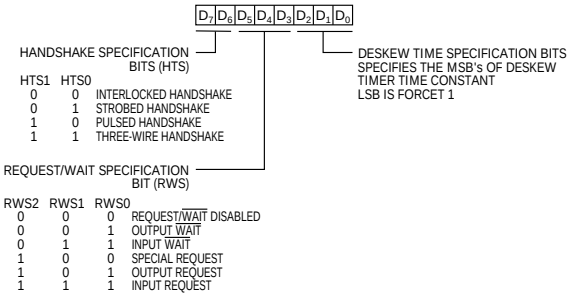
Master Configuration Control Register
Address : 000001
(Read/Write)



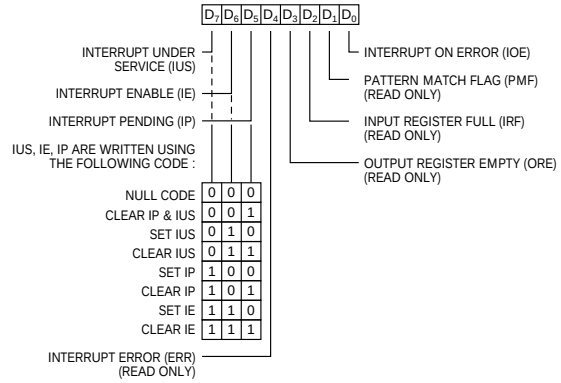
Port Mode Specification Registers
Address : 100000 Port A
101000 Port B
(Read/Write)



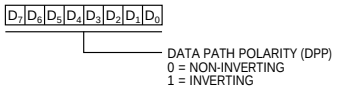
Port Handshake Specification Registers
Address : 100001 Port A
101001 Port B
(Read/Write)



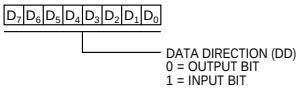
Port Command and Status Registers
Address : 001000 Port A
001001 Port B
(Read/Partial Write)



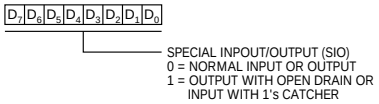
Data Path Polarity Registers
Address : 100010 Port A
101010 Port B
000101 Port C (4 LSBs only)
(Read/Write)



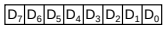
Data Direction Registers
Address : 100011 Port A
101011 Port B
000110 Port C (4 LSBs only)
(Read/Write)



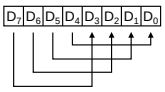
Special I/O Control Registers
Address : 100100 Port A
101100 Port B
000111 Port C (4 LSBs only)
(Read/Write)



Port Data Registers
Address : 001101 Port A (this register can be accessed directly)
001110 Port B (this register can be accessed directly)
(Read/Write)



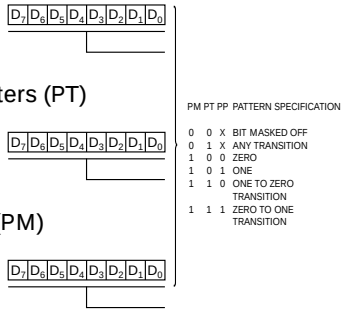
Port C Data Register
Address : 001111 (this register can be accessed directly)
(Read/Write)



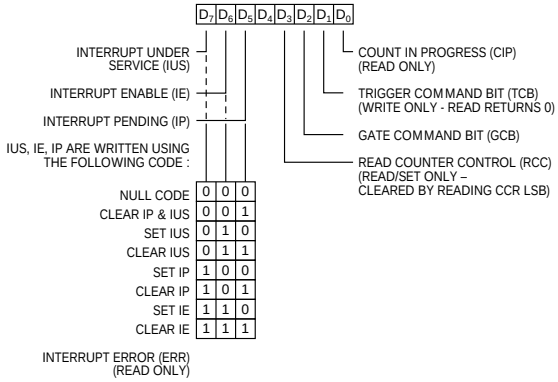
Pattern Polarity Registers (PP)
Address : 100101 Port A
101101 Port B
(Read/Write)

Pattern Transition Registers (PT)
Address : 100110 Port A
101110 Port B
(Read/Write)

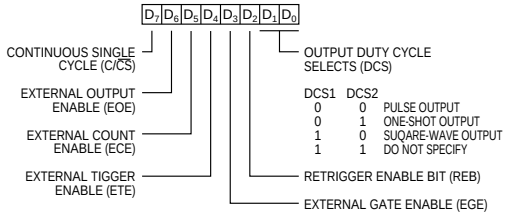
Pattern Mask Registers (PM)
Address : 100111 Port A
101111 Port B
(Read/Write)



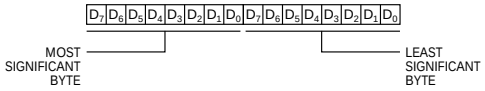
Counter/Timer Command and Status Registers
Address : 001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3
(Read/Partial Write)



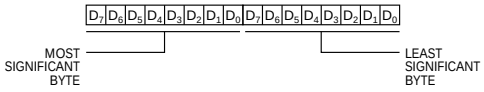
Counter/Timer Mode Specification Registers
Address : 011100 Counter/Timer 1
011101 Counter/Timer 2
011110 Counter/Timer 3
(Read/Write)



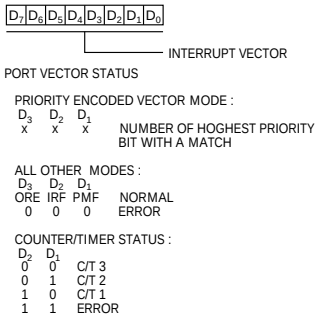
Counter/Timer Current Count Registers
Address : 010000 Counter/Timer 1's MSB
010001 Counter/Timer 1's LSB
010010 Counter/Timer 2's MSB
010011 Counter/Timer 2's LSB
010100 Counter/Timer 3's MSB
010101 Counter/Timer 3's LSB
(Read Only)



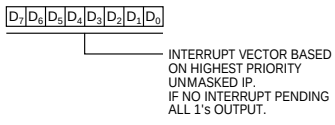
Counter/Timer Constant Registers
Address : 010110 Counter/Timer 1's MSB
010111 Counter/Timer 1's LSB
011000 Counter/Timer 2's MSB
011001 Counter/Timer 2's LSB
011010 Counter/Timer 3's MSB
011011 Counter/Timer 3's LSB
(Read/Write)



Interrupt Vector Registers
Address : 000010 Port A
000011 Port B
000100 Counter/Timers
(Read/Write)



Current Vector Register
Address : 011111
(Read only)



Notes : Write a "1" will select the register bit's function.
Write a "0" will deselect the register bit's function.

Figure 1.4 8536 CIO registers

1.7.3 8536 INTERRUPTS

The 8536 CIO can generate a vectored interrupt when one of the following conditions has occured :

a) A pattern match occuring in a bit port

b) Another byte becoming available in an input port with handshake

c) A counter/timer reaching its terminal count

Five potential sources of interrupts are available. The priorities of these sources are fixed in the following order (highest to lowest) :

1) Counter/Timer 3 HIGHEST
2) Port A
3) Counter/Timer 2
4) Port B
5) Counter/Timer 1 LOWEST

All internal interrupts of the GESSBS-6A are on the level 6. The CIO interrupt priority, relative to other components (8530 SCC and 58274 RTC), is fixed as described below :

1) 8536 CIO HIGHEST
2) 8530 SCC
3) 58274 RTC LOWEST

WARNING : The 8536 needs a recovery time of 650 ns min. between each access. With a 16 MHz CPU, this value is not respected when using instructions like BTST and BCLR.

1.8 8530 SERIAL COMMUNICATIONS CONTROLLER

1.8.1 GENERAL DESCRIPTION

The 8530 SCC Serial Communication Controller is designed for multifunction support for handling the large variety of serial communication protocols available. The 8530 can be programmed to satisfy special serial communications requirements as well as to follow standard formats such as byte-oriented synchronous and asynchronous.

The features of the 8530 SCC are listed below :

- Two independent full-duplex channels,
  Receiver data registers quadruply buffered,
  Transmitter data registers double buffered,
  Baud rate generator in each channel,
  Digital Phase-Locked Loop for clock recovery,
  NRZ, NRZI, and FM encoding/decoding.

- Asynchronous capabilities :
  5, 6, 7 or 8 bits per character,
  1, 1 $^1/_2$ or 2 stop bits,
  Odd or even parity,
  Times 1, 16, 32 or 64 clock modes,
  Break generation and detection,
  Parity, overrun and framing error detection.
- Byte-oriented synchronous capabilities :
  Internal character synchronization,
  1 or 2 sync characters in separate registers,
  Automatic sync character insertion and deletion,
  Cyclic redundancy check (CRC) generation/detection,
  6 or 8-bit sync character.
- SDLC / HDLC capabilities :
  Abort sequence generation and checking,
  Automatic zero insertion and deletion,
  Automatic flag insertion between messages,
  Address field recognition,
  I-field residue handling,
  CRC generation/deletion,
  SDLC loop mode with EOP recognition,
  loop entry and exit.

1.8.2 8530 REGISTERS

The 8530 SCC contains 13 registers in each channel that allow the configuration of the functional characteristic of the channels. Only six registers are directly accessible by the CPU, as shown in table 1.7, allowing access to the other 8530 registers.

Physical Address	Access	Register name
$810021	W	Channel B Control Register
$810021	R	Channel B Status Register
$810023	R/W	Channel B Data Register
$810025	W	Channel A Control Register
$810025	R	Channel A Status Register
$810027	R/W	Channel A Data Register

Table 1.7 8530 SCC directly accessible register map

Notes :
The Control Register is the WRO 8530 register
The Status Register is the RRO 8530 register
The Data Register, in write access, is the WR8 8530 register
The Data Register, in read access, is the RR8 8530 register

The 8530 SCC uses the same two-step sequence as the 8536 CIO, to access the internal registers. First, write the address of the target register into the Control Register of the concerned channel; then read or write to the target register by accessing the Control Register for the second time. Note that the Data registers can be accessed in the same way but it is most useful to make a direct access of these registers.

The table 1.8 gives the target addresses of the 8530 SCC's registers.

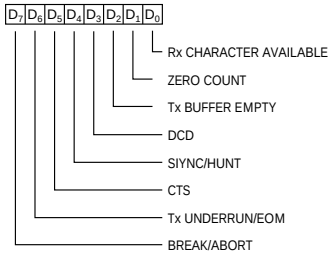
Target register Address	Name	Access	Target register functions
$0	WR0	Write	CRC initialize, registers pointers*
$0	RR0	Read	Transmit/receive buffer and external status*
$1	WR1	Write	Transmit/receive interrupt mode
$1	RR1	Read	Special receive condition status
$2	WR2	Write	Interrupt vector
$2	RR2	Read	Interrupt vector
$3	WR3	Write	Receive parameters and controls
$3	RR3	Read	Interrupt pending bits
$4	WR4	Write	Transmit/receive miscellaneous parameters/modes
$5	WR5	Write	Transmit parameters and controls
$6	WR6	Write	Sync character or SSDLC address field
$7	WR7	Write	Sync character or SDLC flag
$8	WR8	Write	Transmit buffer*
$8	RR8	Read	Receive buffer*
$9	WR9	Write	Master interrupt control and reset
$A	WR10	Write	Miscellaneous transmitter/ reveiver control bits
$A	RR10	Read	Miscellaneous status
$B	WR11	Write	Clock mode control
$C	WR12	Write	Lower byte of baud rate generator time constant
$C	RR12	Read	Lower byte of baud rate generator time constant
$D	WR13	Write	Upper byte of baud rate generator time constant
$D	RR13	Read	Upper byte of baud rate generator time constant
$E	WR14	Write	Miscellaneous control bits
$F	WR15	Write	External/status interrupt control
$F	RR15	Read	External/status interrupt information

* Can be accessed directly

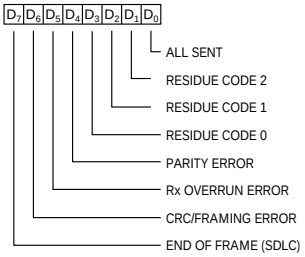
Table 1.8 8530 SCC indirectly accessible register map.

The figure 1.5 describes the contents of the 8530 SCC registers. *For more information regarding 8530 registers programming, please refer to "Z8030/Z8530 SCC Serial Communication Controller technical manual" from Zilog.*

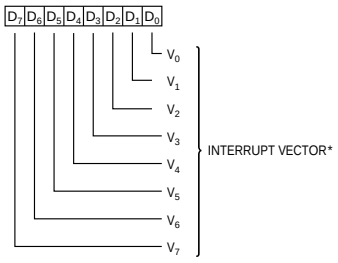
Read Register 0



Read Register 1

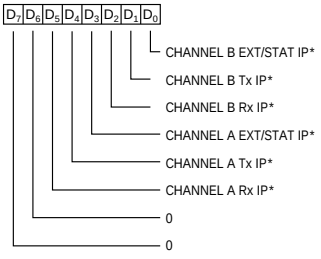


Read Register 2



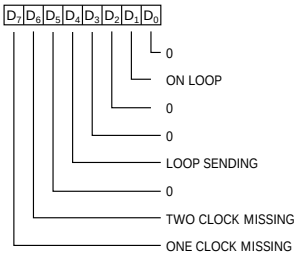
* MODIFIED IN B CHANNEL

Read Register 3

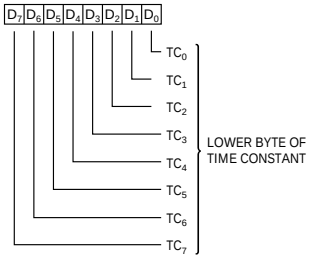


* ALWAYS 0 IN B CHANNEL

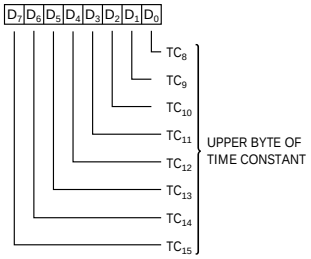
Read Register 10



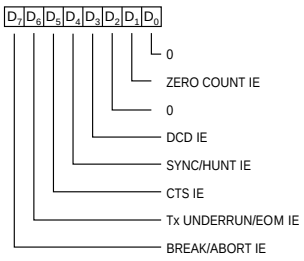
Read Register 12



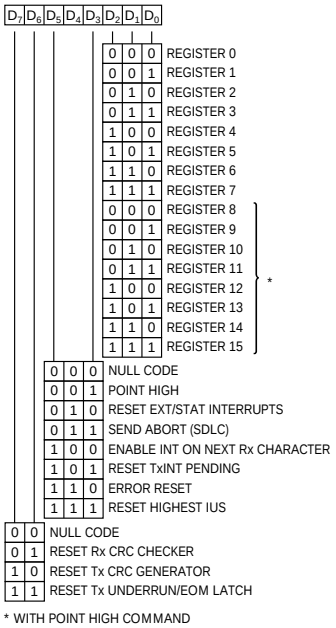
Read Register 13



Read Register 15

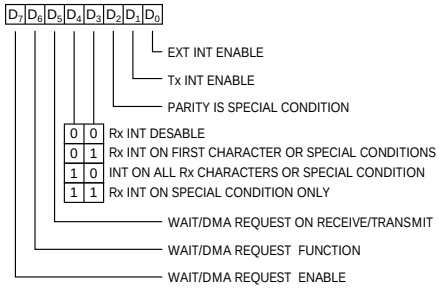


Write Register 0

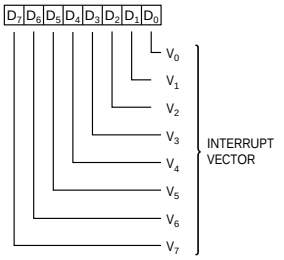


* WITH POINT HIGH COMMAND

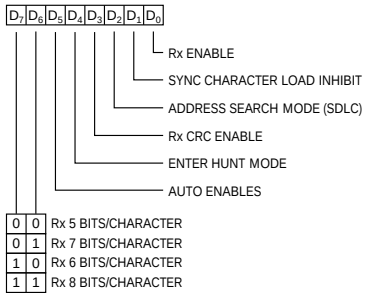
Write Register 1



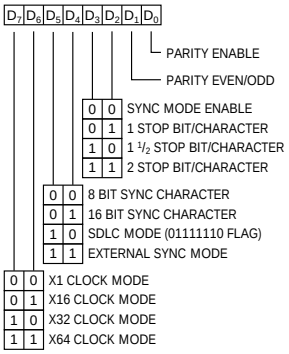
Write Register 2



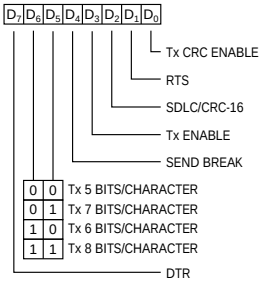
Write Register 3



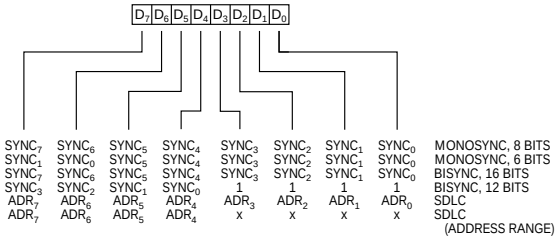
Write Register 4



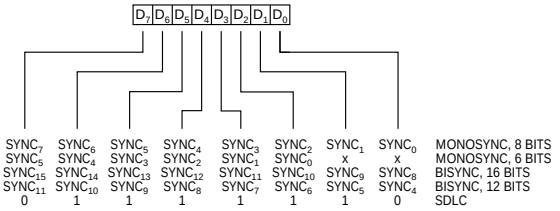
Write Register 5



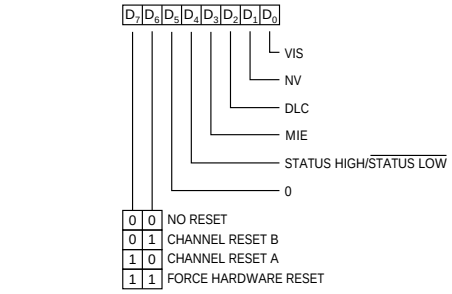
Write Register 6



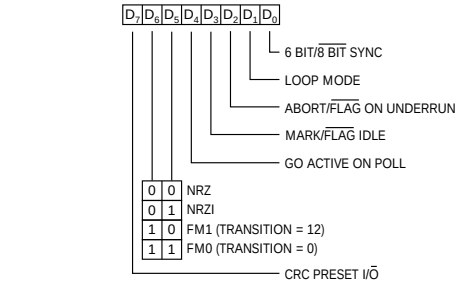
Write Register 7



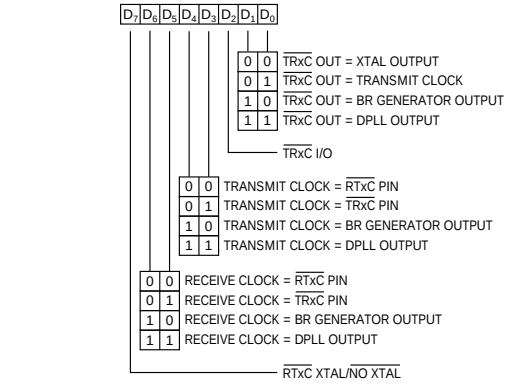
Write Register 9



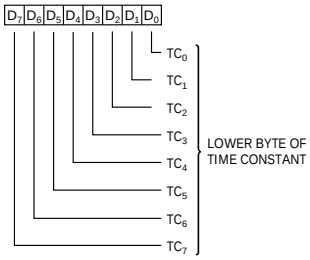
Write Register 10



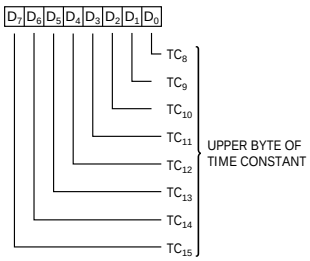
Write Register 11



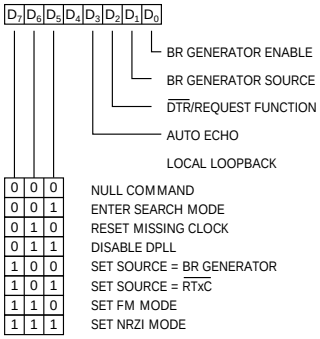
Write Register 12



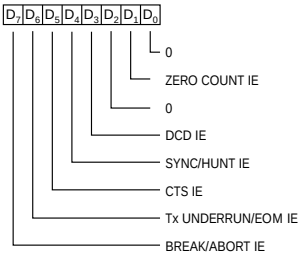
Write Register 13



Write Register 14



Write Register 15



Notes : Write a "1" will select the register bit's function.
Write a "0" will deselect the register bit's function.

Figure 1.5 8530 CIO registers

1.8.3 8530 INTERRUPTS

The 8530 SCC can generate a vectored interrupt when one of the following condition has occured :

a) Channel A transmitter empty
b) Channel A receiver full
c) Channel A external/status conditions
d) Channel B transmitter empty
e) Channel B receiver full
f) Channel B external/status conditions

Channel A interrupts are higher-priority than Channel B interrupts, with the receiver, transmitter and external/status interrupts prioritized in that order within each channel.

All internal interrupts of the GESSBS-6A are on the level 6. The SCC interrupt priority, relative to other components (8536 CIO and 58274 RTC), is fixed as described below :

1) 8536 CIO HIGHEST
2) 8530 SCC
3) 58274 RTC LOWEST

WARNING :

1) In the 8530's interrupt routine, after the interrupt source has been cleared, a delay of 3 µs must be inserted prior to exit from this routine.
2) The 8530 needs a recovery time of 1,8 µs min. between each access. With a 16 MHz CPU, this value is not respected when the 8530 is consecutively accessed. It is recommended to insert NOP instructions to reach this specified delay.

1.9 58274 REAL TIME CLOCK CALENDAR

1.9.1 58274 REGISTERS

The 58274 chip adds to the GESSBS-6A board a real-time clock and calendar function. A battery will maintain timekeeping, when the power supply is turned off. The register map is shown in table 1.9.

Physical Address	Access	Register name
$810041	R	Status register
$810041	W	Control register
$810043	R	Tenths of seconds
$810045	R/W	Unit seconds
$810047	R/W	Tens seconds
$810049	R/W	Units minutes
$81004B	R/W	Tens minutes
$81004D	R/W	Unit hours
$81004F	R/W	Tens hours
$810051	R/W	Unit days
$810053	R/W	Tens days
$810055	R/W	Unit months
$810057	R/W	Tens months
$810059	R/W	Unit years
$81005B	R/W	Tens years
$81005D	R/W	Day of week
$81005F	R/W	Clock setting/Interrupt registers

Table 1.9 RTC 58274 register map

The organisation of the registers is shown in the figures 1.7 through 1.8.
For more information on the device, refer to the manufacturer's data sheet.

a) Status Register (read only)

Address : 810041 (Hexadecimal)

7	6	5	4	3	2	1	0
*	*	*	*	DCF	0	0	IF

*Unused bits

DCF Data-Changed Flag. This flag is set by the clock setting pulse which also clocks the time registers. Testing this bit can tell the processor whether or not the time has change during a read operation

SET	The time data has changed while being read out of the clock by the processor
CLEARED	Status register read

IF Interrupt Flag. When this bit is one, it indicates that an interrupt is pending.

SET	The interrupt timer times out
CLEARED	Status register read

b) Control Register (write only)

Address : 810041 (Hexadecimal)

7	6	5	4	3	2	1	0
*	*	*	*	TST	CSS	RS	ISS

*Unused bits

TST Test. A one written into the test bit puts the device into test mode. This allows setting of the oscillator frequency. For normal operation the test bit is loaded with zero

CSS Clock Sart/Stop. A one stops the timekeeping of the clock and resets to zero the tenths of seconds counter. Timing is restarted when the start/stop bit is written with a zero.

RS Register Select. The register select bit determines which of the two registers mapped onto address 81005F will be accessed when this address is selected.

RS	Register selected
0	Clock setting register
1	Interrupt register

ISS Interrupt Start/Stop. The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit, a one to halt the interrupt and reset the timer, a zero to start interrupt timing.

SET	MPU writes a one
CLEARED	MPU writes a zero

Figure 1.7 Status/Control Register

a) Clock Setting Register (RS bit = 0))

Address : 81005F (Hexadecimal)

7	6	5	4	3	2	1	0
*	*	*	*	LY1	LY0	AM/PM	12/24

*Unused bits

LY1-LY0 The leap year counter is a 2-stage binary counter which should be loaded with the number of years since the last leap year.

AM/PM AM/PM indicator. The AM/PM indicator returns a zero for AM and a one for PM in the 12-hour mode. This bit is forced to zero in 24-hour mode.

AM/PM indicator	
0	AM
1	PM

12/24 12/24-hour mode. The 12/24-hour mode bit determines whether the hours counter counts from 1 to 12 or from 0 to 23.

12/24-hour bit	
0	12-hour mode
1	24-hour mode

SET	MPU writes a one
CLEARED	MPU writes a zero

b) Interrupt Control Register (RS bit = 1)

Address : 81005F (Hexadecimal)

7	6	5	4	3	2	1	0
*	*	*	*	S/R	LP2	LP1	LP0

*Unused bits

SR This bit determines the interrupt mode.

SR	Mode
0	Single interrupt
1	Repeated interrupt

LP2-LP0 These bits determine the time delay period that will occur between interrupts.

LP2	LP1	LP0	Time Delay
0	0	0	No interrupt
0	0	1	0.1 second
0	1	0	0.5 second
0	1	1	1 second
1	0	0	5 seconds
1	0	1	10 seconds
1	1	0	30 seconds
1	1	1	60 seconds

Figure 1.8 Clock Setting/Interrupt Control Register

1.9.2 58274 INTERRUPTS

The interrupt generated by the 58274 RTC are wired on the level 6 of the CPU. These interrupts are autovectored.

The RTC interrupt priority, relative to other components (8536 CIO and 8530 SCC), is fixed as described below :

1) 8536 CIO HIGHEST
2) 8530 SCC
3) 58274 RTC LOWEST

1.10 COMPLEMENTARY INFORMATION

For complementary information about the programming procedure of the devices used on the GESSBS-6A, please refer to the manufacturer's data sheet.

- 8536 CIO *"Z8536 Counter/Timer and Parallel I/O Unit technical manual"* from ZILOG.
- 8530 SCC *"Z8530 Serial Communications Controller technical manual"* from ZILOG.
- 58274 RTC *"MM58274 Microprocessor Compatible Real Time Clock"* from NATIONAL

2. PREPARATION FOR USE, INTERCONNECTIONS

2.1 CONNECTOR AND JUMPERS IDENTIFICATION

Table 2.1 identifies the jumpers and connectors of the GESSBS-6A module. Figure 2.1 shows their locations on the printed circuit.

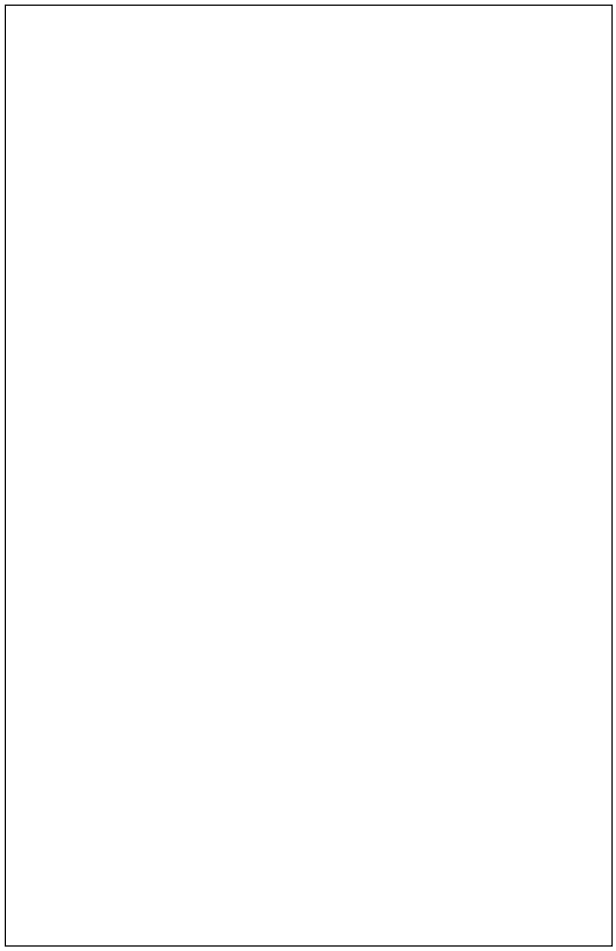


Figure 2.1 Implementation

Designation	Function
P1	G-64/G-96 Bus interface connector
P2	External Reset and Abort switch connector
P3	Parallel I/O and Timers connector
P4	Serial channel B connector
P5	Serial channel A connector
J1	Watch Dog Fail Off/Reset/Interrupt selector
J2	Serial Channel B DCE/DTE configuration selector
J3	Serial channel A Transmit/Receive clock selector
J4	Serial channel A DCE/DTE configuration selector
J5	– EPROM wait-states selector – U13/U14 EPROM/RAM selector
J6	SRAM wait-states selector
J7	U13/U14 devices selector
J8	U13/U14 devices selector
J9	U15/U16 EPROM type selector
J10	– 8/16 MHz running frequency selector
J11	– 8/16 µs bus timeout selector – Autovectored/vectored interrupt mode selector – 1/2 MHz Enable clock selector – 8/16 MHz running frequency selector – IACK/IACK signal selector – BGRT/BGRT signal selector
J12	8/16 MHz CPU clock selector
J13	U13/U14/U15/U16 devices selector
J14	$\overline{PWF}$ Power Fail signal selector
J15	SRAM battery backup selector
J16	Enable-bus signal 3-state control
J17	Bus system clock selector
J18	U13/U14 devices selector
J19	PG1 page extension selector
J20	RTC battery backup on/off
J23	2M x 1 bit EPROM selection
LED	– Red : SUPERVISOR mode – Green : Halt or Reset state – Yellow : External access

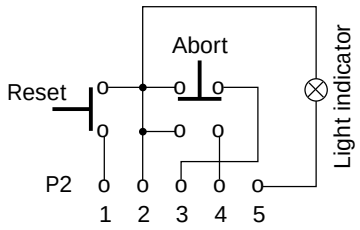
Table 2.1 Connector, switch and jumper identification

2.2 RESTART OPERATION

Power-on reset is automatically generated on the module. External switches for reset and abort can be connected to P2 connector as illustrated on figure 2.2.

The external reset switch reinitializes the GESSBS-6A module and activates the RESET signal on the G-64/G-96 Bus.

1	Reset
2	Ground
3	Abort - NC
4	Abort - NO
5	+ 5 Vdc



P2 pin assignment P2 external connection

Figure 2.2 External Reset/Abort switch connection

2.3 SERIAL COMMUNICATION INTERFACE

2.3.1 GENERAL INFORMATION

The GESSBS-6A provides two RS 232-C serial interfaces driven by the 8530 SCC device

The first serial interface corresponding to channel A of the 8530, allows asynchronous and synchronous communications and provides signals for modem connection.

The second serial interface corresponding to channel B of the 8530, allows only asynchronous communications. This interface is partial, but it is sufficient for terminal, mouse, etc.

Interconnections on J4, J2 permit the configuring of the interface of channels A and B respectively for DCE (Data Communication Equipment) or DTE (Data Terminal Equipment) mode.

The GESSBS-6A uses the GESPAC standard 3M 10-pin RS 232-C connector (P4, P5) for each channel. Standard signals for the RS 232-C are defined in the table 2.2 and the pin assignment of P4/P5 connectors is shown in tables 2.3 and 2.4.

Note :
The theorical speed limitation of the RS 232-C interface is 19200 Bauds with a cable of 15 meters.

Pin No	Signal name	Signal description
1	Protective Ground	Normally connected to chassis
2	Transmit Data (TxD)	Direction : TO modem (DCE). This line transfers data from a terminal to a modem.
3	Receive Data (RxD)	Direction : FROM modem. This line transfers data from a modem to a terminal.
4	Request to Send (RTS)	Direction : TO modem When active (high level), this signal requires a data transfer on TxD from the terminal to the modem.
5	Clear to Send (CTS)	Direction : FROM modem. When active (high level), this signal indicates that the modem is ready to receive a data transfer on TxD. CTS is the modem answer to RTS.
6	Data Set Ready (DSR)	Direction : FROM modem. When active (high level), this signal indicates that the modem is connected and ready to receive terminal commands.
7	Signal Ground (GND)	Signal is used as the reference potential.
8	Data Carrier Detect (DCD)	Direction : FROM modem. When active (high level), this signal indicates that the modem is receiving a telephone modulation within the appropriate modem limits.
9-14	Not used	
15	TxC	Direction : TO modem. Terminal clock output
16	Not used	
17	RxC	Direction : FROM modem. Terminal clock input
18-19	Not used	
20	Data terminal Ready (DTR)	Direction : TO modem. When active (high level), this signal indicates to the modem that the terminal is connected and operational.
21-25	Not used	

Notes : In RS 232-C (V24) sinal names are always specified in conjunction with the DTE
DCE = Data Communication Equipment
DTE = Data Terminal Equipment

Table 2.2 RS 232-C 25-pin delta connector

3M 10-pin P5 pin # (flat cable)	3M 20-pin RS 232-C pin # (flat cable)	25-pin delta RS 232-C pin # (flat cable)	RS 232-C signal
1	1	1	GND
3	3	2	TxD
5	5	3	RxD
7	7	4	RTS
9	9	5	CTS
2	11	6	DSR*
4	4	15	TxC
6	14	20	DTR*
8	15	8	DCD*
10	8	17	RxC*

Table 2.3 Channel A (P5) connector pin assignment

3M 10-pin P4 pin # (flat cable)	3M 20-pin RS 232-C pin # (flat cable)	25-pin delta RS 232-C pin # (flat cable)	RS 232-C signal
1	1	1	GND
3	3	2	TxD
5	5	3	RxD
7	7	4	RTS
9	9	5	CTS
2	11	6	DSR*
4	4	15	–
6	14	20	DTR*
8	15	8	DCD*
10	8	17	–

* Important note : these RS 232-C signals can not be directly connected to a 3M 20-pin RS 232 connector or to a 25-pin delta RS 232 connector. If these signals are used, a Null-Modem box must be inserted between the GESSBS-6A and the transmitter/receiver module connected

Table 2.4 Channel B (P4) connector pin assignment

2.3.2 DCE/DTE CONFIGURATION

Signals defined in table 2.2 are connected to P4/P5 connectors respectively through the interconnection of J4/J2 as illustrated in fugures 2.3 and 2.4.

The figures 2.5 and 2.6 show the configuration of J4/J2 for two standard applications. For special configurations, refer to table 2.2 for signal definition and figure 2.3 and 2.4 for their interconnections.

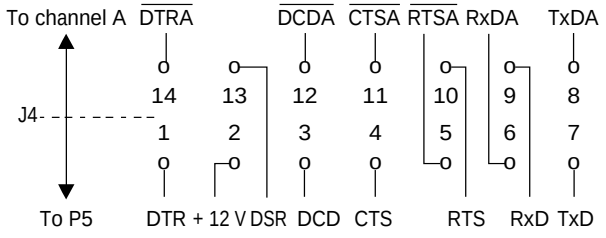


Figure 2.3 J4 pin assignment

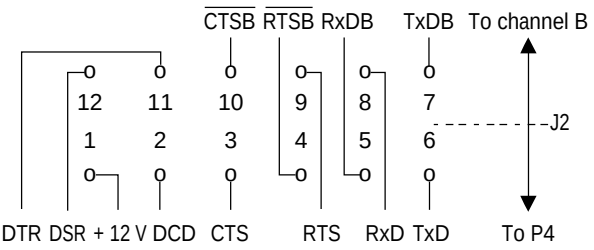


Figure 2.4 J2 pin assignment

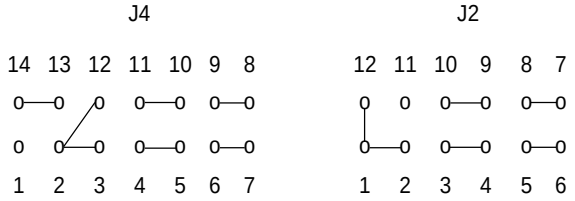


Figure 2.5 DCE configuration

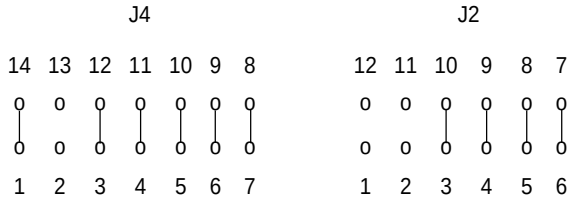


Figure 2.6 DTE configuration

2.3.3 Tx and Rx CLOCK SELECTION

The transmit and receive clock for channel A can be selected to be either internal or external (synchronous operations) of the GESSBS-6A. When internal, the clock are provide by the one-chip baud rate generator (inside the 8530 device). The clock selection for the channel A is shown in figure 2.7.

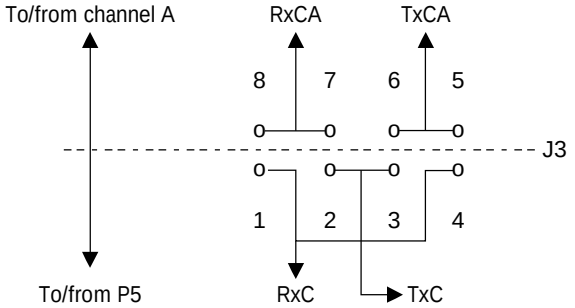


Figure 2.7 Tx and Rx clock selection for the Channel A

2.4 PARALLEL I/O AND TIMERS CONNECTOR

The 8530 CIO's parallel I/O lines are available to the user through connector P3 as shown in table 2.5. Some I/O lines are double function to control the timers/counters as described in table 2.6.

P3 pin #	Signal name	P3 pin #	Signal name
7	PA0	8	PB0
9	PA1	10	PB1
4	PA2	12	PB2
3	PA3	14	PB3
2	PA4	16	PB4
1	PA5	18	PB5
5	PA6	17	PB6
6	PA7	15	PB7
20	PC0	23	+ 12 V
19	PC1	25	- 12 V
13	PC2	21	+ 5 V
11	PC3	22, 24, 26	GND

Table 2.5 P3 Signal identification

Function	Timer 1	Timer 2	Timer 3
Timer Output	PB4	PB0	PC0
Timer Input	PB5	PB1	PC1
Trigger Input	PB6	PB2	PC2
Gate Input	PB7	PB3	PC3

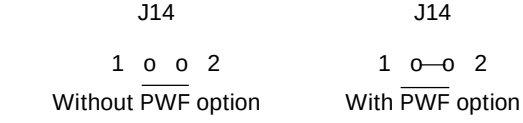
Table 2.6 Counter/Timer external control lines identification

2.5 INTERRUPTS

2.5.1 AC POWER FAIL

The power-fail signal ($\overline{PWF}$) is a high priority non-maskable interrupt input. This interrupt input is connected through the control register (see section 1.5) to the interrupt level 7 of the 68000 device.

An external logic asserts the $\overline{PWF}$ line to indicate the occurence of an AC power failure. PWF selection is shown in figure 2.8.



Note : Make sure that in G-64 environment the - 5 V power supply is not used and not connected on the backplane before placing a jumper on J14 otherwise serious damage may occur on the GESSBS-6A module

Figure 2.8 Power fail selection

2.5.2 INTERRUPT STRUCTURE

The 68000 has 7 interrupt levels which are used by internal devices and by the interrupt-bus lines. The interrupts issued from the on-board peripheral devices are handled by internal interrupt controller which generates an interrupt request on the level 6.

The power-fail bus line ($\overline{PWF}$), the non-maskable interrupt-bus line ($\overline{NMI}$), the ABORT switch and the Watch-dog fail signal ($\overline{WDF}$) are connected through the control register on the level 7.

The interrupt level 1 to 5 are respectively assigned to the interrupt-bus lines IRQ1 to $\overline{IRQ5}$. Table 2.7 summarizes this interrupt structure.

Interrupt	Priority	Mode	Issued from
7	Highest	a	NMI, PWF, ABORT and WDF
6		v	8536 CIO
6		v	8530 SCC
6		a	58274 RTC
5		a/v	$\overline{IRQ5}$-bus line
4		a/v	$\overline{IRQ4}$-bus line
3		a/v	$\overline{IRQ3}$-bus line
2		a/v	$\overline{IRQ2}$-bus line
1	Lowest	a/v	$\overline{IRQ1}$-bus line

v = vectored interrupt mode
a = autovectored interrupt mode

Table 2.7 Interrupt structure

2.5.3 AUTOVECTORED/VECTORED INTERRUPT MODE SELECTION

During an interrupt aknowledge cycle, the processor fetches an 8-bit vector number on the data bus lines. The processor logic translates this vector number to obtain the address of an interrupt handling routine. This process is know as vectoring. If the internal logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level being serviced. This process is known as autovectoring. The interrupt bus line IRQ1 to $\overline{IRQ5}$ work either in the vectored or in the autovectored mode; the jumper J11 make this selection as shown in table 2.8.

Interrupt line	Interrupt mode	
	Autovectored J11	Vectored J11
$\overline{IRQ1}$	8 o—o 17	8 o o 17
$\overline{IRQ2}$	9 o—o 16	9 o o 16
$\overline{IRQ3}$	10 o—o 15	10 o o 15
$\overline{IRQ4}$	11 o—o 14	11 o o 14
$\overline{IRQ5}$	12 o—o 13	12 o o 13

Table 2.8 Interrupt mode selection

2.6 BUS TIMEOUT LOGIC

In bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. An internal circuitry is used to abort a data transfer cycle by generating a bus error to the CPU, if the DTACK bus signal is not returned before 8 or 16 µs. The figure 2.9 shows how to select this timeout.

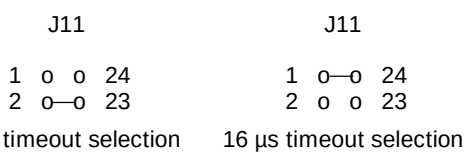


Figure 2.9 8/16 µs timeout selection

2.7 CPU SPEED SELECTION

The GESSBS-6A has been designed to work either with an 8 MHz or 16 MHz 68000 CPU. The figure 2.10 describes the selection that must be made by the user to adapt the GESSBS6-A timings for an 8 MHz or 16 MHz CPU.

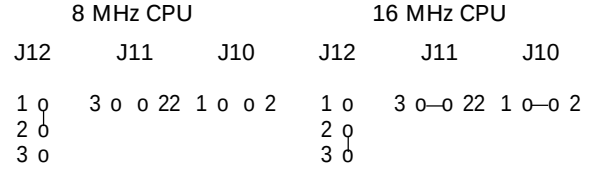


Figure 2.10 8/16 MHz CPU selection

2.8 ENABLE SPEED SELECTION

The GESSBS-6A module provides the Enable signal which is required by all synchronous I/O modules. Furthermore the GESSBS-6A can provide an optional Enable signal for the 2 MHz version of synchronous I/O modules. The Enable speed selection is illustrated in the table 2.9.

Enable clock period	Sync. I/O module type	J11 jumper
1 µs	Standard 1 MHz	4 o o 21
500 ns	Optional 2 MHz	4 o—o 21

Table 2.9 Enable speed selection

2.9 IACK AND BGRT SENSE SELECTION

To ensure the compatibility between the G-64 bus and the G-96 bus, the sense of IACK and BGRT signals are defined by J11 as shown in table 2.10.

J11	Signal sense
5 o o 20 6 o—o 19 7 o o 18	BGRT selection for the G-64 bus IACK selection for the G-64 bus
5 o—o 20 6 o o 19 7 o—o 18	$\overline{\text{BGRT}}$ selection for the G-96 bus $\overline{\text{IACK}}$ selection for the G-96 bus

Table 2.10 IACK and BGRT sense selection

2.10 MEMORY TYPE SELECTION

2.10.1 U15 AND U16 MEMORY TYPE SELECTION

U15 and U16 sockets can be equipped with either 28 or 32-pin JEDEC compatible devices. These two sockets can receive only EPROM devices from 8 Kbytes up to 128 Kbytes (2764, 27128, 27256, 27512, 271001).

The GESSBS-6A module can also be equiped with 4 x 272001 EPROM devices as explained in the section 2.18.

A 28-pin device must be connected at the bottom of the 32-pin socket provided on the GESSBS-6A module. The U15 socket is connected to the lower data D7-D0 and U16 socket to the upper data D15-D8.

Device type selection is made with J9 and J13 jumpers as illustrated in table 2.11.

EPROM	J9	J13
2764 8 Kbytes	1 2 3 o o—o	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5
27128 16 Kbytes	1 2 3 o o—o	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5
27256 32 Kbytes	1 2 3 o—o o	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5
27512 64 Kbytes	1 2 3 o—o o	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5
271001 128 Kbytes	1 2 3 o—o o	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5

Table 2.11 U15 and U16 EPROM selection

2.10.2 U13 AND U14 MEMORY TYPE SELECTION

U13 and U14 sockets can be equiped with either 28 or 32-pin JEDEC compatible devices. These two sockets can receive both RAM and EPROM devices from 8 Kbytes up to 128 Kbytes (2764, 27128, 27256, 27512, 271001, 6564, 65256, 628128).

A 28-pin device must be connected at the bottom of the 32-pin socket provided on the GESSBS-6A module. The U14 socket is connected to the lower data D7-D0 and U13 socket to the upper data D15-D8.

Device type selection is made with J7, J8, J13 and J18 jumpers as illustrated in table 2.12.

The GESSBS-6A module can also be equiped with 4 x 272001 EPROM devices as explained in the section 2.18.

EPROM	J7	J8	EPROM	J13	J18
2764 8 Kbytes	1 2 3 o o—o	1 2 3 4 5 o o o o—o	2764 8 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
27128 16 Kbytes	1 2 3 o o—o	1 2 3 4 5 o o o o—o	27128 16 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
27256 32 Kbytes	1 2 3 o o—o	1 2 3 4 5 o—o o o o	27256 32 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
27512 64 Kbytes	1 2 3 o o—o	1 2 3 4 5 o—o o o o	27512 64 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
271001 128 Kbytes	1 2 3 o o—o	1 2 3 4 5 o—o o o o	271001 128 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
RAM	J7	J8	RAM	J13	J18
6564 8 Kbytes	1 2 3 o—o o	1 2 3 4 5 o o—o o o	6564 8 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
65256 32 Kbytes	1 2 3 o o—o	1 2 3 4 5 o o—o o o	65256 32 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o
628128 128 Kbytes	1 2 3 o o—o	1 2 3 4 5 o o—o o o	628128 128 Kbytes	10 9 8 7 6 o o o o o o o o o o 1 2 3 4 5	1 o 2 o 3 o

Table 2.12 U13 and U14 RAM/EPROM selection

2.11 MEMORY ACCESS TIME

2.11.1 RAM ACCESS TIME SELECTION

The local memory of the GESSBS-6A can operate at zero wait state depending on the CPU speed and the memory access time. Table 2.13 shows the selection for different access times.

	8 MHz CPU		16 MHz CPU	
J6	RAM access time	Wait state	RAM access time	Wait state
1 o 2 o 3 o	250 ns	0	120 ns	0
1 o 2 o 3 o	350 ns	1	180 ns	1

Table 2.13 RAM access time selection

2.11.2 EPROM ACCESS TIME SELECTION

The memory cycle duration can be selected to use EPROM devices with different access times. Table 2.14 shows the selection for different devices.

	8 MHz CPU		16 MHz CPU	
J5	EPROM access time	Wait state	EPROM access time	Wait state
1 o—o 10 2 o o 9 3 o o 8 4 o o 7 5 o o 6	250 ns	0	120 ns	0
1 o o 10 2 o—o 9 3 o o 8 4 o o 7 5 o o 6	350 ns	1	180 ns	1
1 o o 10 2 o o 9 3 o—o 8 4 o o 7 5 o o 6	450 ns	2	240 ns	2
1 o o 10 2 o o 9 3 o o 8 4 o—o 7 5 o o 6	650 ns	4	320 ns	4

Table 2.14 EPROM access time selection

2.11.3 U13 AND U14 TIME ACCESS SELECTION

U13 and U14 sockets can be equipped either with EPROM or RAM devices. By setting the position 5-6 of J5, the access time of U13/U14 devices will follow either the EPROM access time selection (see section 2.11.2) or the RAM acces time selection (see section 2.11.1) as described in figure 2.11.

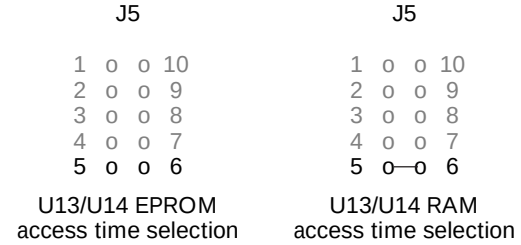


Figure 2.11 U13/U14 devices access time selection

2.12 BUS MEMORY EXTENSION IN G-64 MODE

The G-64 Bus normally addresses directly 128 K x 16 (256 Kbytes) by using A0-A15 and Page0 bus signals.

The GESSBS-6A module has been designed with an additional address line - Page1 to provide the user with more addressing capability. This line allows direct addressing extension on the G-64 Bus up to 256 K x 16 (512 Kbytes).

In order not to change the G-64 stucture, the CHAIN IN bus line that is not used on a CPU module has been chosen as Page1. This permits placing the memory modules on one side of the CPU module (CHAIN IN side), while the chain structure is still available on the other side of the CPU module (CHAIN OUT side).

The new 16-bit memory module have a connection between the CHAIN IN and CHAIN OUT lines. In this way, if the memory boards are connected into consecutive connectors beside the GESSBS-6A module, the Page1 signal will be transmitted from the CPU to the last memory board. When one or more connectors are left free between two memory modules, the CHAIN IN and CHAIN OUT lines must be short circuited.

To make the selection of the Page1 signal to the bus, place a jumper on position 1-2 of J9 as shown in figure 2.13

Figure 2.12 illustrates the arrangement of the module on the bus to allow 512 Kbytes adressing and chain structure capability.

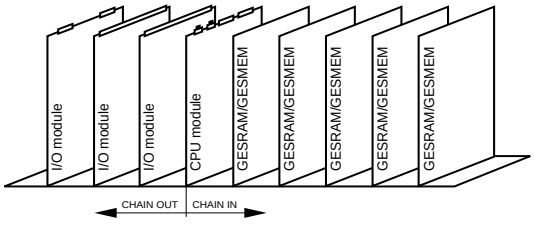


Figure 2.12 Module disposition for addressing extension

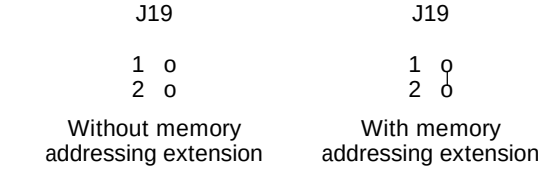


Figure 2.13 Memory addressing extension selection

2.13 ENABLE AND SYCLK CLOCK CONTROL

The Enable and SYCLK bus signal can be selected on J16 to be TTL or 3-states. In TTL mode, Enable and SYCLK signals are active during DMA operations, but at high impedance if the 3-state mode is selected. The 3-state mode is controlled by J16 jumper, as shown in table 2.15.

J16	Function
1 2 3 o—o o	Enable and SYCLK signals are free running on the bus during DMA operations
1 2 3 o o—o	Enable and SYCLK signals in the high impedance state during DMA operations

Table 2.15 Enable and SYCLK 3-state control

2.14 SYCLK SIGNAL SELECTION

The system clock (SYCLK) signal on the bus can be selected on J17 to run at 16 MHz or to follow the CPU clock (8/16 MHz). The SYCLK signal selection is shown in table 2.16.

J17	1 2 3 o o—o	1 2 3 o—o o
SYCLK	16 MHz	CPU clock

Table 2.16 SYCLK signal selection

2.15 BATTERY OPERATION

2.15.1 RTC BATTERY POWER SWITCH

An on-board battery provides the standby power supply for the real-time-clock, when the main power supply is turned off. The battery can be disconnected by removing the position 1-2 of J20, also ensure that a jumper is in place when the GESSBS-6A is operational.

Figure 2.14 RTC standby battery power switch

2.15.2 RAM STANDBY BATTERY POWER SWITCH

An external battery connected on the + 5 V bat. bus line can provide the standby power supply to the Low Power Static RAM (in SMD package) located at CPU addresses $F40000-$F7FFFF (256 Kbytes), when the main power supply is turned off.

The RAM equipped on U13 and U14 sockets are not protected against the power fail.

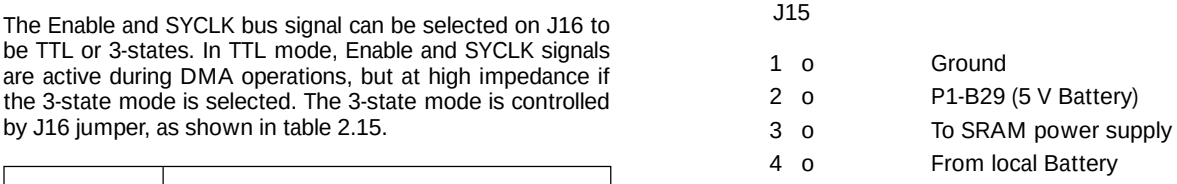


Figure 2.15 RAM standby battery power switch

2.16 WATCHDOG SELECTION

The GESSBS-6A module implements a Watchdog function which is, in fact, a retriggerable monostable circuit. This monostable is triggered each time that positions $810069 are accessed (read and write mode).

If the monostable has not been accessed before the end of time T1, it will generate a Watch Dog Fail ($\overline{WDF}$) signal which can be wired on the interrupt level 7 through the control register or on the reset line as shown in figure 2.16.

The refresh time T1 and the duration time T2 of $\overline{WDF}$ have been fixed respectively at 1.3 s. and 1.3 ms. But by simple hardware modifications, it is easy to change these values :

Formula T1 = 0.28 x R2 [ohm] x C3 [f]
T2 = 0.28 x R4 [ohm] x C2 [f]

Standard values of R2/R4 and C3/C2 : 470 K/47 K and 10 µf /0.1 µf.

Notes : - The Watchdog function is started at first access of positions $810061-$81007F.
- If $\overline{WDF}$ signal is wired on the reset line, it is recommended not to use the external reset switch.

Figure 2.16 Watch Dog Fail signal selection

2.17 LED INDICATORS

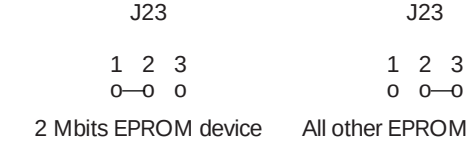
The GESSBS-6A module is supplied with three indicators, a red LED which is switched on when the processor is in the supervisor mode, a yellow LED which is switched on when the processor accesses external modules and therefore uses the G-64/G-96 Bus and finally a green LED which is switched on when the processor is halted or during reset operation.

2.18 2 Mbits EPROM SELECTION

The four sockets U13, U14, U15 and U16 can be equiped with 2 Mbits EPROM devices.

WARNING : *this configuration requires a specific decoding PAL device. Please contact GESPAC for more informations.*

The jumper J23 makes this selection as shown below :



2 Mbits EPROM device — All other EPROM devices

Note : All the jumpers J7-J8-J9-J13 and J18 must be set for a 128 K x 8 EPROM device type (271001).

Figure 2.17 2 Mbits EPROM selection

CPU Byte address (hexadecimal)	BUS Word address (hexadecimal)	Field size	Physical address space
FFFFFF F80000	Do not care	512 Kbytes	Internals EPROM/ SRAM U13, U14
F7FFFF F00000	Do not care	512 Kbytes	Internals EPROM U15, U16
EFFFFF EC0000	Do not care	256 Kbytes	Internal Low Power SRAM

Note : Other field are not changed.

Table 2.17 2 Mbits EPROM memory map

2.19 INTERFACE WITH THE G-96 BUS

The GESSBS-6A module interconnects directly on a G-96 bus. Signals used by the module are identified in table 2.18

For more information on the bus, refer to the G64/G96 Bus Specification Manual.

ROW C	ROW B	ROW A		Definition
GND	GND	GND	1	Power
A16 A17 A18 A19 A20 A21 A22 A23	A8 A9 A10 A11 A12 A13 A14 A15	A0 A1 A2 A3 A4 A5 A6 A7	2 3 4 5 6 7 8 9	Address Lines A0 to A23
Reserved Reserved Reserved GND Reserved Reserved IRQ3 IRQ5 VED *	BRQ DS1 BGACK/BBUSY Enable RES NMI IRQ1 IRQ2 IACK	BGRT DS0 HALT SYCLK VPA RDY/DTACK VMA R/W IRQ4	10 11 12 13 14 15 16 17 18	Control and Interrupt Lines
GND P5 * P4 * P3 * P2 * P1 * P0 * Reserved	D12 D13 D14 D15 D4 D5 D6 D7	D8 D9 D10 D11 D0 D1 D2 D3	19 20 21 22 23 24 25 26	Data Lines D0 to D15 and Arbitration Lines
SYSFAIL * EVCLK *	BERR Chain in **	Page Chain out	27 28	Misc.
Reserved Reserved + 5 V GND	+ 5 V bat. – 12 V + 5 V GND	PWF +12 V + 5 V GND	29 30 31 32	Power

* Not used in the GESSBS-6A module.
** Used as address extension in G-64 mode (see section 2.12)

Table 2.18 P1 connector, G-96 Bus

3. DYNAMIC CHARACTERISTICS FOR SYNCHRONOUS OPERATIONS

3.1 GENERAL INFORMATION

Dynamic characteristics that will be defined correspond to the G-96 Bus signals. Symbols used are shown in figure 3.1.

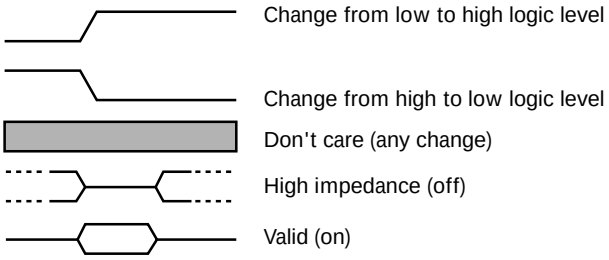


Figure 3.1 Signal symbols

3.2 READ-WRITE OPERATION

All transfers are synchronous with ENABLE signal and controlled by R/W and VPA signals, as shown in figure 3.2. Timing values are given in tables 3.1 and 3.2.

Signal name	Description	Value (ns)		
		Min.	Typ.	Max.
tE	Cycle time		1000	
tEL	Pulse width low		500	
tEH	Pulse width high		500	
tEAL	Address lead time	200		
tEPL	$\overline{VPA}$ command lead time	170		
tEWPL	Write lead time for peripheral	170		
tEWDS	Data set-up time for write cycle			0
tERDS	Data set-up time for read cycle			325
tH	Hold time	10		

Table 3.1 Timing for synchronous peripherals (1 MHz)

Signal name	Description	Value (ns)		
		Min.	Typ.	Max.
tE	Cycle time		500	
tEL	Pulse width low		250	
tEH	Pulse width high		250	
tEAL	Address lead time	200		
tEPL	$\overline{VPA}$ command lead time	170		
tEWPL	Write lead time for peripheral	170		
tEWDS	Data set-up time for write cycle			0
tERDS	Data set-up time for read cycle			325
tH	Hold time	10		

Table 3.2 Timing for synchronous peripherals (2 MHz)

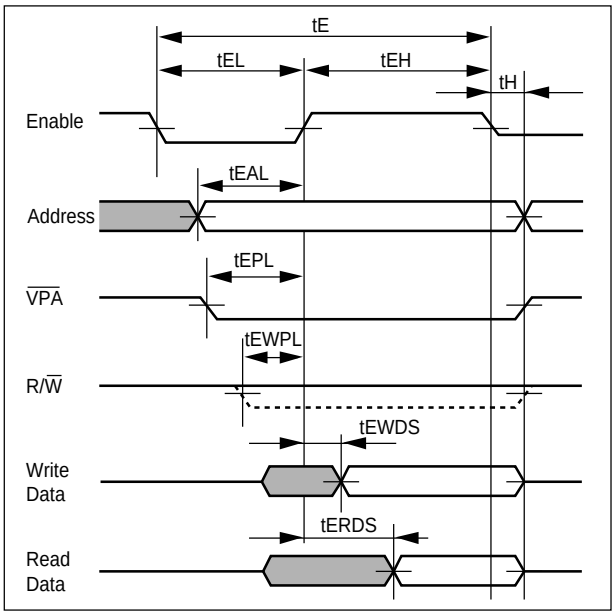


Figure 3.2 Read-Write operation

4. DYNAMIC CHARACTERISTICS FOR ASYNCHRONOUS OPERATIONS

4.1 READ-WRITE OPERATION

An asynchronous read sequence is shown in figure 4.1 and a write sequence in figure 4.2. Refer to the diagram of figure 4.3 and table 4.1 for the timing.

The figure 4.4 illustrates an interrupt aknowledge sequence.

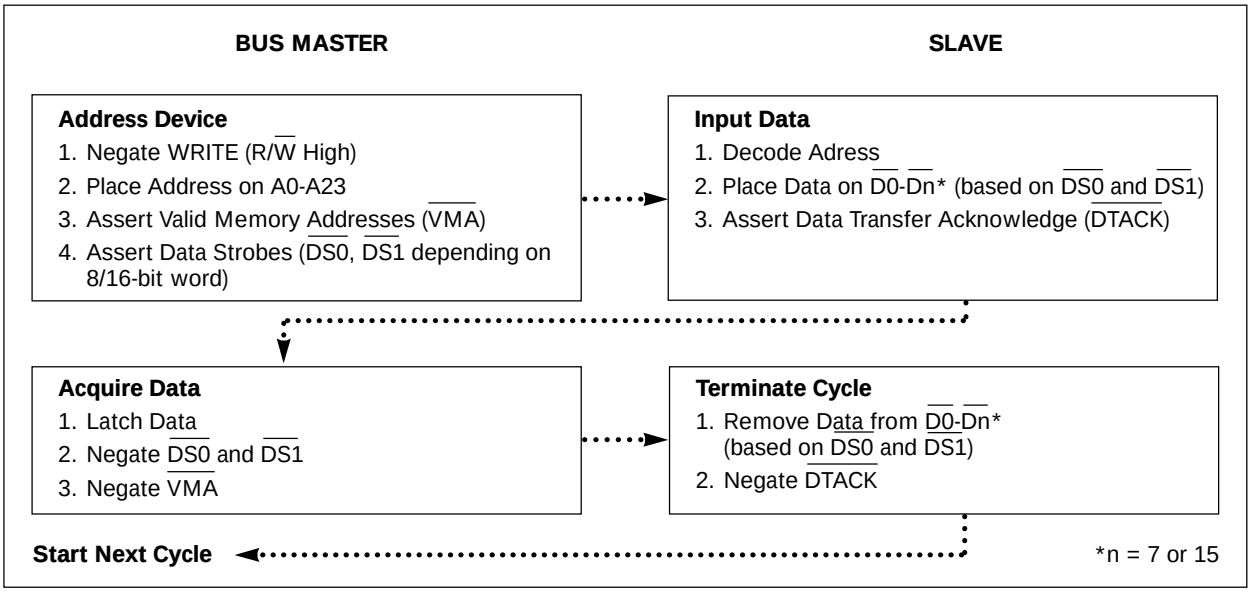


Figure 4.1 Asynchronous Read sequence

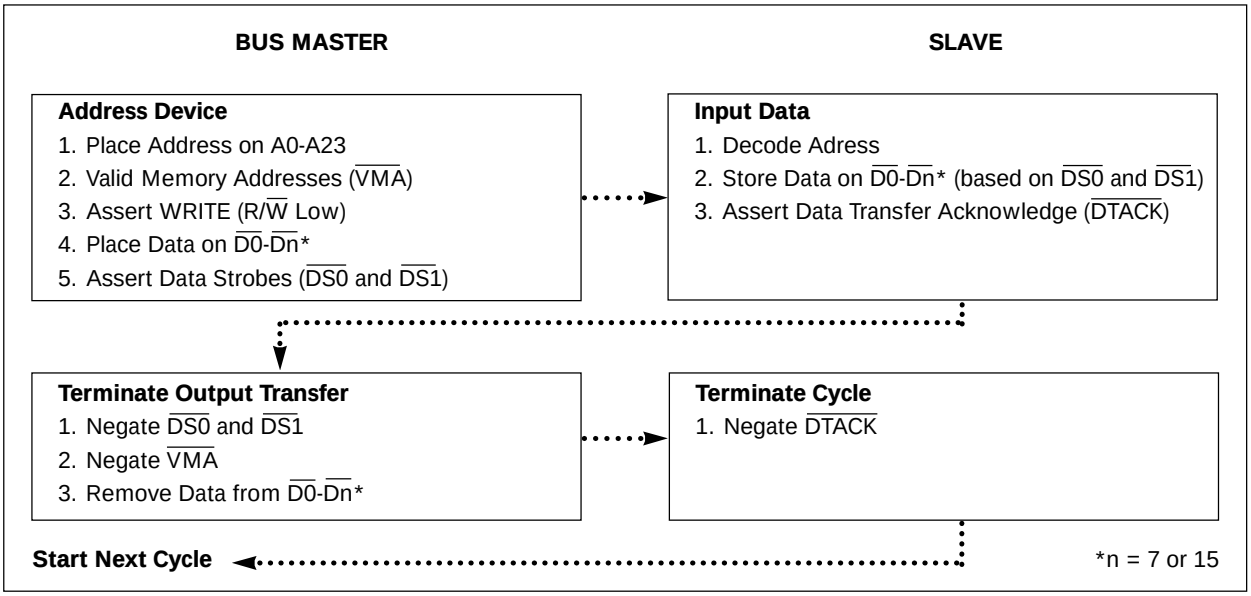


Figure 4.2 Asynchronous Write sequence

Signal name	Description	8 MHz CPU				16 MHz CPU				Unit
		Read value		Write value		Read value		Write value		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tAH	Address hold time	10		10		10		10		ns
tAL	Address lead time	30		30		30		30		ns
tASDS	Address Strobe DS delay	0		40		0		0		ns
tASH	Address Strobe High	150		150		80		80		ns
tASL	Address Strobe Low	240[1]		365[1]		120[1]		180[1]		ns
tCY	Cycle periode	500[1]		625[1]		240[1]		300[1]		ns
tDSDT	$\overline{DS}$ to $\overline{DTACK}$		50		50		20		20	ns
tDSL	Data Strobe Low	240[1]		240[1]		120[1]		140[1]		ns
tDHT	$\overline{DTACK}$ hold time	0		0		0		0		ns
tRDS	Read data set-up time		70				10			ns
tR/WH	$\overline{R}$/W signal hold time	10		10		10		10		ns
tR/WL	$\overline{R}$/W signal lead time	60		80		50		20		ns
tWDH	Write data hold time			10				10		ns
tWDL	Write data lead time			30				20		ns

Note : [1] These values can be increased by steps of one CPU clock period, if the tDSDT parameter can not be met.

Table 4.1 Asynchronous timing

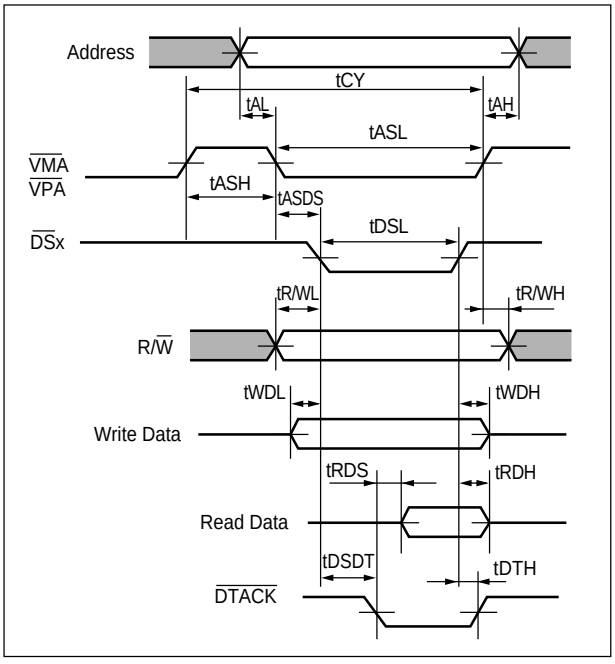


Figure 4.3 Read-Write operation

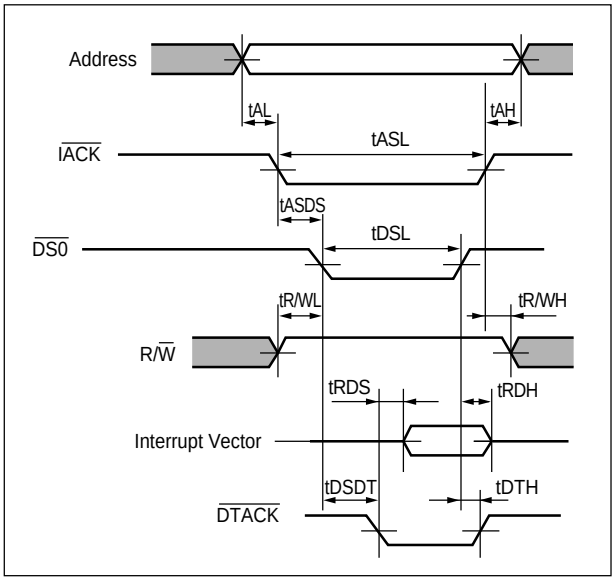


Figure 4.4 Interrupt acknowledge operation

4.2 BUS TIMEOUT LOGIC

In bus architecture that requires an handshake from an external device, the possibility exists that the handshake might not occur. An internal circuitry is used to abort a data transfer cycle if it exceeds the timeout value. In this case, the processor initiates a bus error exception sequence.

This restriction is made to guarantee that the processor does not loop indefinitely on a non-present device. Figure 4.5 shows a bus error sequence. Timing values are given in table 4.2.

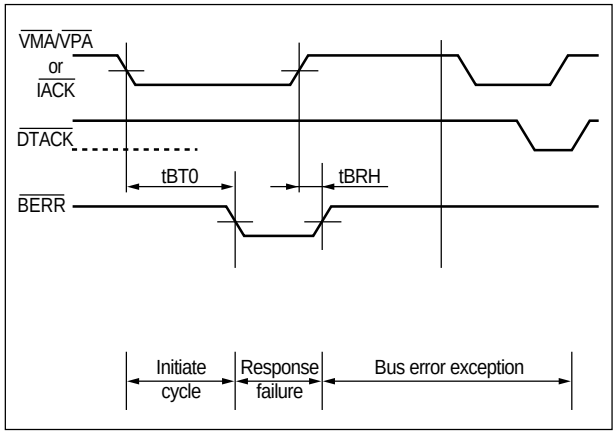


Figure 4.5 Bus error exception sequence

Signal Name	Description	Min.	Max.	Unit
tBTO	Bus timeout delay	8	16	µs
tBRH	BERR hold time	0	40	ns

Table 4.2 Bus error timing

5. BUS ARBITRATION

5.1 BUS ARBITRATION

A device may request the use of the G-96 Bus from the Bus arbiter via the wired-Or Bus request line BRQ.

A Bus Grant (BGRT) and a Bus Grant Acknowledge (BGACK) lines are provided and the Daisy chain line (Chain in, Chain out) can be used when priority is required.

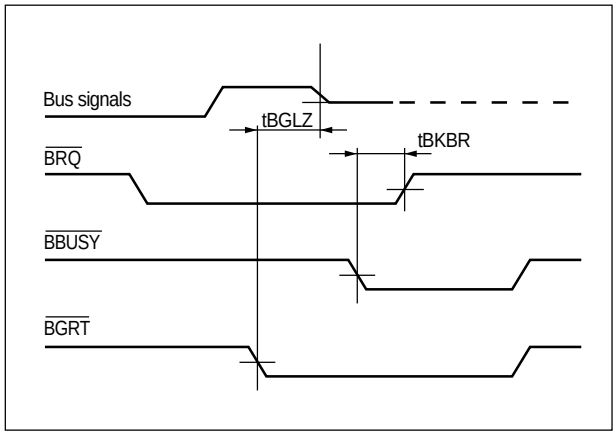


Figure 5.1 Bus Arbitration timing diagram

Signal name	Description	8 MHz CPU value (ns)		16 MHz CPU value (ns)	
		Min.	Max.	Min.	Max.
BGLZ	BGRT low to Bus High Impedance		50		50
tBKBR	BGACK low to BRQ high	50		50	

Table 5.1 Timing values for Bus Arbitration

NOTES

NOTES

NOTES :

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