

POS Control Boards

Various Performance Level to Fit Your Application & Budget

Powerful All-in-one POS Control Boards



Advantech's POS control board series is designed specifically for the POS and related multimedia applications that require array of I/O connections at an affordable price. All POS control boards follow the commercial All-In-One WD/LPX form factor with over 50% of required IOs directly accessible from the rear. This allows for easy OEM system integration as well as easy adaptability to lower cost commercial chassis.

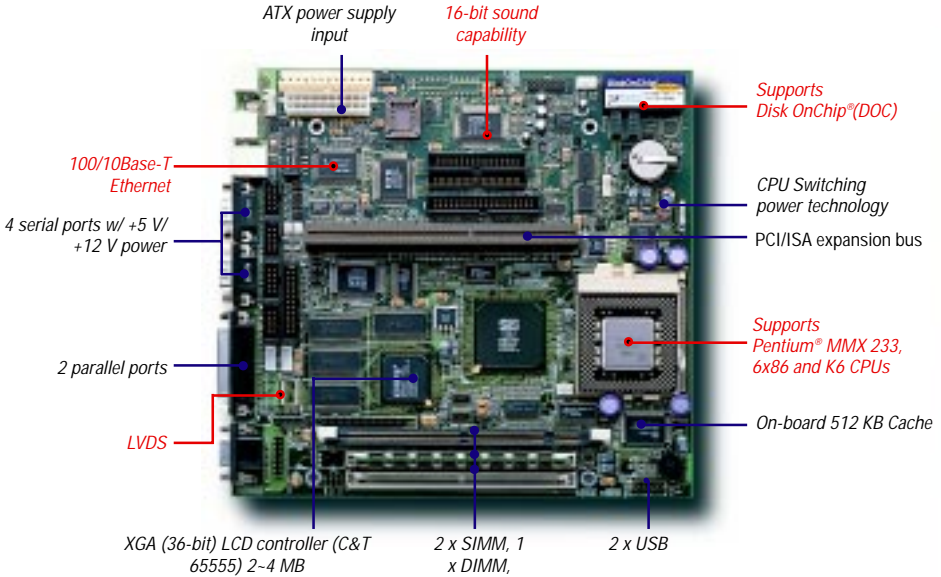
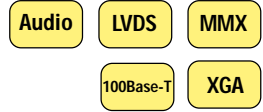
Retaining Advantech's industrial grade performance, the POS control boards starts with POS-460 at 486 entry level and moves to POS-560 supporting up to 233Mhz 586 MMX CPUs. Our latest addition is the POS-562 Super POS with on-board 100 base-T, audio and LVDS interface. Common features on all POS control boards are 4 serial ports with power, SSD, LCD, VGA and PCI/ISA expansion bus. The POS control board series stands ready to accommodate all your special embedded PC requirements.

Reliable, Affordable and Flexible

All-in-one Control Board for POS and Related Multimedia Applications

POS-562

Pentium MMX SBC with 100BaseT, Audio and LVDS



220 mm x 235 mm (8.7" x 9.3")

Ordering Information

POS-562-00A1	586 based SBC with 100/10 BASE-T ETHERNET, VGA, LCD, LVDS, Audio, On board 512 KB cache and 2MB VDRAM. (No CPU, DRAM, SSD memory)
POS-562L-00A1	586 based SBC with 100/10 BASE-T ETHERNET, VGA, LCD, LVDS, On board 512 KB cache and 2MB VDRAM. (No CPU, DRAM, SSD memory) No Audio.
POS-560-00A1	586 based SBC with 10 BASE-T ETHERNET, VGA, LCD. On board 512 KB cache and 1MB VDRAM. (No CPU, DRAM, SSD memory)
POS-560-20A1	586 based SBC with 10 BASE-T ETHERNET, VGA, LCD, LVDS, On board 512 KB cache and 2MB VDRAM. (No CPU, DRAM, SSD memory)
POS-460-00A2	486 SBC w/ VGA, LCD, SSD, 10 BASE-T ETHERNET w/ 512KB VDRAM, (No DRAM, SSD memory, CPU and cache.)
POS-460-40A2	486 SBC w/ VGA, LCD, SSD, 10 BASE-T ETHERNET w/ 512KB VDRAM, 4M on board DRAM, (No SSD memory, CPU and cache.)