DC MOTOR FULL BRIDGE 1A

E192.01

PRODUCTION DATA - JUL 25, 2011

RoHS compliant

Features

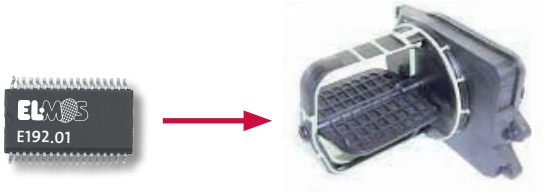
- Supply voltage range 5.5V to 19V
- Two push pull low drop power outputs for 1A nominal current with slew rate control
- Internal charge pump
- Control logic
- Shut down capabilities via an integrated timer or a trigger signal
- Over voltage protection
- Under voltage detection
- Over temperature protection
- A clamped 12V supply voltage for an external hall cell
- Power on circuit
- 50mA Open-drain low side driver with battery voltage capability
- Operating temperature range –40°C to + 132°C
- QSOP36 package

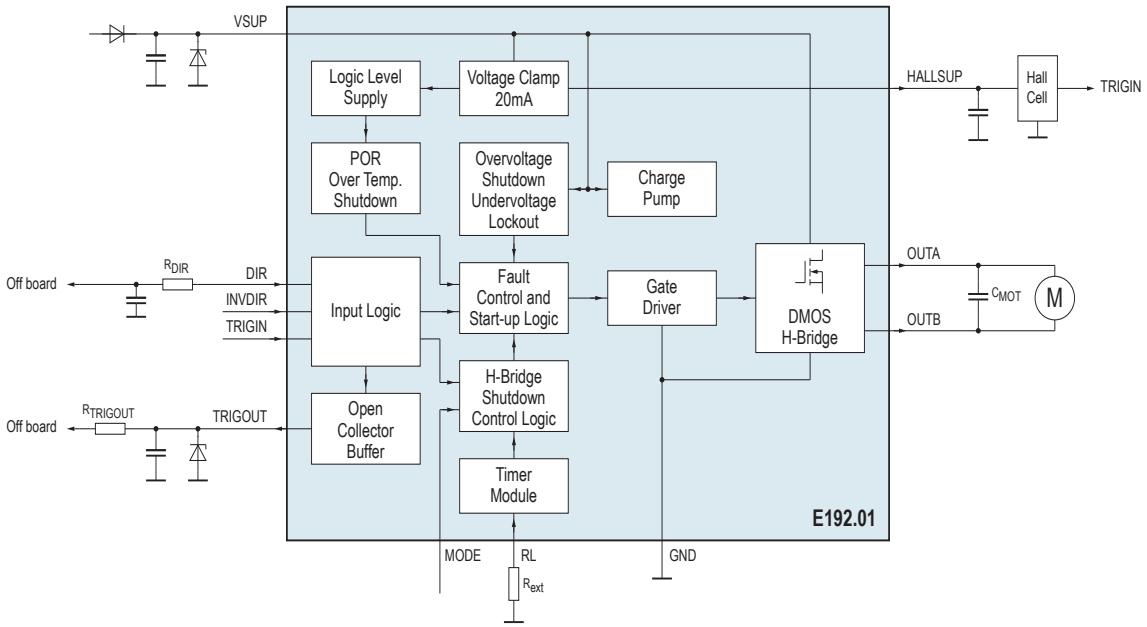
General Description

This IC combines several key functions of DC Motor Controller used in an automotive under-hood application. It contains all function blocks to run the motor bidirectional or to brake it.

Applications

- Intake manifold
- Powertrain





1 General Device Specification

1.1 Absolute Maximum Ratings

Operation of the device above these ratings is not permitted!

Parameter	Condition	Symbol	Min	Max	Unit
Long term Power Dissipation	Ta < +105°C	P_{NO105}		800	mW
	Ta = +125°C	P_{NO125}		450	mW
	Ta = +132°C	P_{NO132}		330	mW
Thermal resistance (Junction to Ambient)	Continuously [1])	R_{TJ-A}		55	K/W
Junction Temperature		T_J	-40	150	°C
Operating Temperature Range		T_{OPT}	-40	132	°C
Storage Temperature Range		T_{STG}	-40	150	°C
Supply voltage **VSUP**	T=0.5ms	V_{SUP_pku}	- 0.3	50	V
Output voltage **TRIGOUT**	T=500ms	V_{SUP_pkm}	- 0.3	40	V
Input voltage **DIR**	Continuously	V_{SUP_max}	- 0.3	26.5	V
Output current **TRIGOUT**	Peak, T=500ms	$I_{TRIGOUT}$	-25	[2])	mA
	Continuously		0	25	mA
Voltage at **OUTA**, **OUTB**	Continuously		- 0.3	19	V
Current **OUTA**, **OUTB**	Peak, T=50ms	I_{PEAK}	-3.8	3.8	A
	Continuously	I_{NOM}	-1	+1	A
Input voltage of all digital input pins	Peak [3])	V_{DIGin_p}	- 0.3	V_{DD}+0.3	V
Output current **HALLSUP**	Peak, T=500ms	$I_{HALLSUP\_p}$	-5	[1])	mA
	Continuously	$I_{HALLSUP\_c}$	0	20	mA

[1]) with a 2inch² copper area on board as heat sink connected to the six fused pins and two additional one.
[2]) Internally limited
[3]) V_{DD} = 4…6V, if V_{SUP}>6.5V

1.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Operating Temperature Range		T_{OPT}	-40		105	°C
Extended Operating Temperature Range		T_{OPTEXT}	-40		132	°C
Supply Voltage Range		V_{SUP}	6,5	13.6	16	V
	For the **TRIGOUT** function only [4]		5.5	13.6	16	V

All of the following parameters are valid for an operating temperature range of -40°C to 125°C and the supply voltage range, unless otherwise specified.
Voltage reference is GND, if not otherwise specified. The current values are positive, if flowing into the circuit.

1.2.1 IC mounting notes

The board layout has a huge effect on the thermal performance of this application. A sophisticated board layout can reduce the R_{TJ-A} down to **40K/W** or lower!
This IC is delivered in a power package with fused leads. Pins 8, 9, 10, 26, 27 and 28 have direct metal connection to the lead paddle and that way to the silicon. These pins are the most efficient thermal bridges to ambient. For a good thermal performance it is strongly recommended to connect these pins to large copper areas on the board.
Connecting all other pins to large copper areas will improve the thermal performance. One should leave as much copper as possible in the direct surrounding of the IC. Metal gaps on the board between pins on same potential enlarge the thermal impedance and should be avoided!
Some pins are assembled in groups with same electrical potential. One should take care, that those pins (like **GND** pins 1-2-35-36, pins 17-18-19 or the **NC** with the **VSUP** pins 5-6, 13-14, 23-24 and 31-32) are connected each to a non-interrupted and gap-less copper area! For the **VSUP** – **NC** connection for instance this leads to a wider metal wire. Its width is two times the pin width plus the pin distance compared to a simple connection to a single pin.

[4]) According to description in chapter 2.1.1 and 3.2.5

1.2.2 Load conditions and thermal requirements

The IC E192.01 controls with its integrated H-Bridge a DC-Motor. This Motor moves a valve between two determined positions. The current draw during one motion period is shown in ***Figure 1.2.2-1.*** At the end of each motion period the valve is running in a soft mechanical blocking performed by a spring. In one type of application a Hall-Cell detects the end of the motion and sends a signal to the IC, which shuts down the H-Bridge as soon as the end position is reached. Another type of application works without a hall cell. In this application the IC will shut down the motor after a certain time.

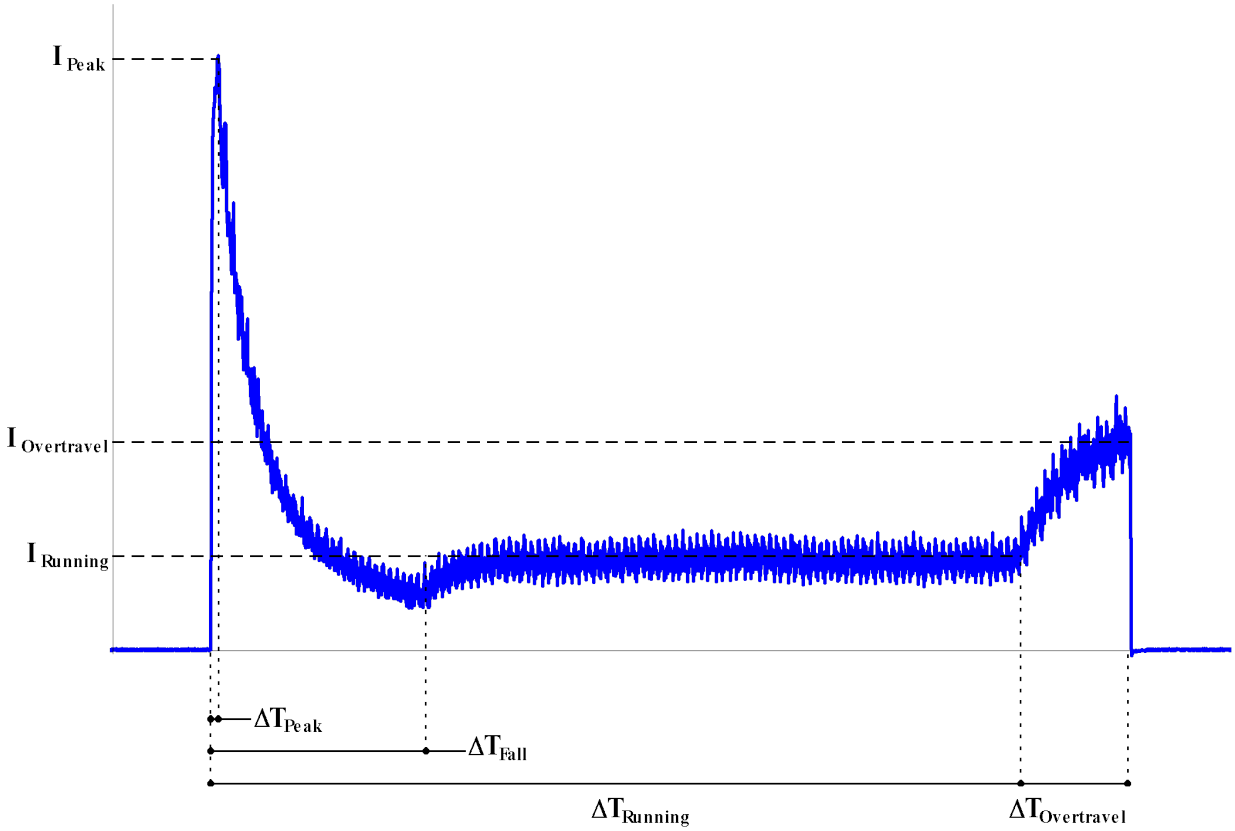


Figure 1.2.2-1 Current draw of the DC-Motor during one motion period

The power dissipation peaks (under worst case conditions up to 6W) with the current draw since the on-resistance of the integrated H-bridge is independent on the current. So the short-term power dissipation can exceed the long-term power dissipation by a factor of ten or more.
The long-term thermal resistance R_{TJ-A} of the QSOP36 package is 55K/W [5]**)**, a suitable PCB layout taken for granted (refer to chapter 2.2.1). That means, that at 125°C for instance the long-term power dissipation should not exceed 450mW in order to prevent a silicon temperature above 150°C. An additional power dissipation of the voltage clamp for **HALLSUP** has to be taken into account.
Since the power dissipation in case of continuously high duty-cycles is too large, it is necessary to limit the duty-cycle in order to reduce the average power dissipation in the IC. Referring to ***Figure 1.2.2-2*** a higher power dissipation for short time periods the can be accepted.
However, due to the limited average power dissipation there are cool–down periods with a low duty-cycle required. ***Table 1.2.2-1*** lists the maximum duty-cycle for a certain condition.

[5]) A sophisticated board layout can reduce R_{TJ-A} down to 40K/W.

Voltage [V]	Current Characteristics						Ambient temp. [°C]	Duration [sec]	Duty-Cycle [%]
	I_{Peak} [A]	$I_{Running}$ [A]	$I_{Overtravel}$ [A]	ΔT_{Peak} [msec]	$\Delta T_{Running}$ [msec]	$\Delta T_{Overtravel}$ [msec]			
13.5	2	0.30	0.65	5	500	60	105	1 time	100
								5	50
Nominal								10	50
								20	50
								Continuous	25
16	2	0.75	0.75	5	500	60	105	1 time	100
								5	50
Maximum ratings at Upper temperature range								10	40
								20	25
								Continuous	10
16	1.75	0.75	0.75	5	500	60	132	1 time	100
								5	40 [6])
Maximum ratings at Extreme temperature range								10	25 [6])
								20	10 [6])
								Continuous	10 [6])
16	1.75	1.40	1.85	4	500	42	132	1 time	100
Extreme ratings at Extreme temperature range									

Table 2.2.2-1 List of allowed duty-cycles for various conditions.

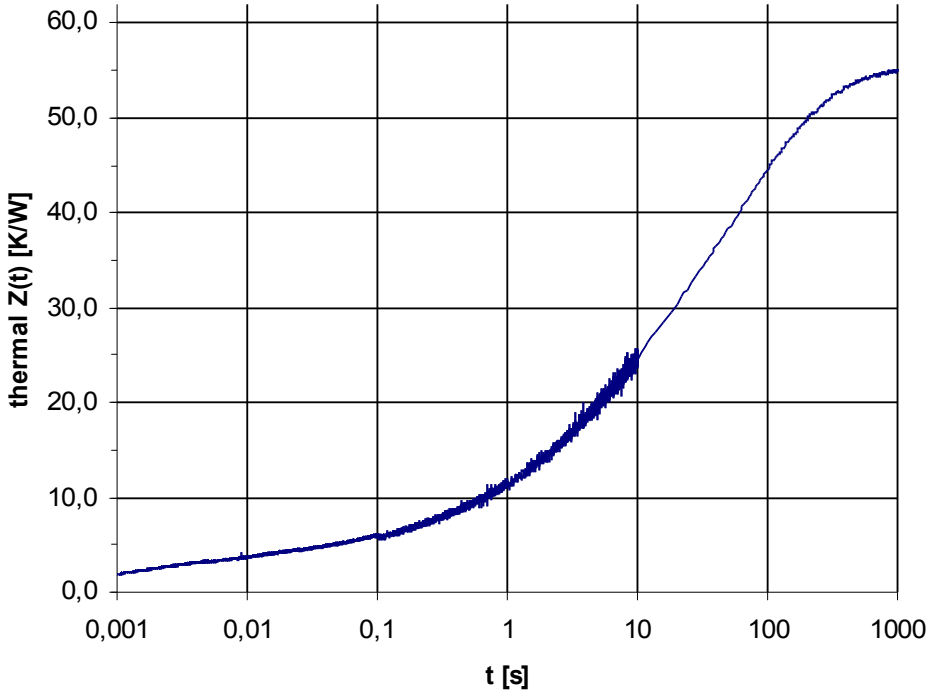


Figure 1.2.2-2 Thermal impedance between the silicon chip and the board environment of the QSOP36 package as a function of t. Pins 8 to 11 and 26 to 29 are connected to a 2inch² on-board copper area.

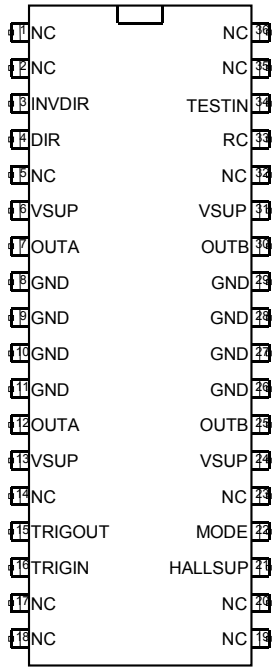
[6]) Not recommended

1.3 Package

QSOP36 (fused) Package

ELMOS packages meet the requirements of the latest JEDEC outline specification. All JEDEC outline specifications can be free downloaded from http://www.jedec.org or please contact your local ELMOS-Key-Account-Manager

1.4 Package Pin Out



1.5 Pin Description

Pin Number	Pin name	Function
8, 9, 10,11, 26, 27, 28, 29	**GND**	Supply Ground
3	**INVDIR**	**INVDIR** = L ⇒ Inverts the meaning of **DIR**: Logic input, standard 5V logic level.
4	**DIR**	Direction Command: HV Logic input, 16V logic level.
1, 2, 5, 14, 17, 18, 19, 20, 23, 32, 35, 36	**NC**	Not internally connected. Connect to anywhere.
6	**VSUP**	Power supply voltage for the H-bridge (pin 7) and internal supply.
13, 24, 31	**VSUP**	Power supply voltage for the H-bridge only. Internally connected via resistors.
7,12	**OUTA**	DIMOS H-Bridge Output A.
15	**TRIGOUT**	Buffered Shutdown Trigger: Open drain output for 50V max.
16	**TRIGIN**	Shutdown Trigger: Logic input with internal pull up, standard 5V logic level.
21	**HALLSUP**	Clamped supply voltage for external Hall-Cell.
22	**MODE**	Logic input with internal pull up to 5V, connect not, to GND or HALLSUP
25, 30	**OUTB**	DIMOS H-Bridge Output B.
33	**RC**	Timing resistor for internal oscillator.
34	**TESTIN**	Test mode enable input. Should be connected to GND.

2 Detailed Electrical Description

The following parameters are valid for the operating conditions mentioned in Chapter 2.2 unless otherwise specified.

2.1 DC Characteristics

2.1.1 Supplies and Outputs

Parameter VSUP	#	Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage range	06.01		V_{SUP}	6.5	13.6	26.5	V
	06.02	For the **TRIGOUT** function only [7])	V_{SUP}	5.5	13.6	26.5	V
OVLO Enable threshold	06.03	[8])	V_{thOVLO}	16,1	17.6	19	V
OVLO Enable hysteresis	06.04		$V_{thOVHys}$	300		1200	mV
UVLO Enable threshold	06.05		V_{thUVLO}	7	7.3	7.6	V
UVLO Enable hysteresis	06.06		$V_{thUVHys}$	80		600	mV
Power on reset threshold	06.07	V_{SUP} ↗	V_{thPORH}	3.9		5.5	V
Power off reset threshold	06.08	V_{SUP} ↘	V_{thPORL}	3.8		5.4	V
Power on/off reset hysteresis	06.09		V_{hysPOR}	0.1		1.7	V
Supply current	06.10	no load	I_{BB}			2	mA

Parameter OUTA/OUTB	#	Conditions	Symbol	Min	Typ	Max	Unit
Leakage current high side drivers	07.01	OUTA=Z or OUTB=Z [9])	I_{DSSH}			60	µA
Leakage current low side drivers	07.02	OUTA=Z or OUTB=Z	I_{DSSL}			60	µA
Output on resistance	07.03	$T_a \leq 25°C$, $V_{SUP} \geq 10V$	R_{DSON_high}		0.25	0.4	Ω
	07.04	$T_a \leq 25°C$, $V_{SUP} \geq 10V$	R_{DSON_low}		0.25	0.4	Ω
	07.05	$T_a \leq 125°C$, $V_{SUP} \geq 10V$ [10])	R_{DSON_high}		0.6	0.8	Ω
	07.06	$T_a \leq 125°C$, $V_{SUP} \geq 10V$ [10])	R_{DSON_low}		0.6	0.8	Ω
	07.07	$T_a \leq 25°C$, $7.1V < V_{SUP} < 10V$ [11])	R_{DSON_high}		0.35	0.55	Ω
	07.08	$T_a \leq 25°C$, $7.1V < V_{SUP} < 10V$	R_{DSON_low}		0.35	0.55	Ω
	07.09	$T_a \leq 125°C$, $7.1V < V_{SUP} < 10V$ [10]) [11])	R_{DSON_high}		0.8	1.1	Ω
	07.10	$T_a \leq 125°C$, $7.1V < V_{SUP} < 10V$ [10])	R_{DSON_low}		0.8	1.1	Ω

[7]) According to description in chapter 3.1.1 and 4.2.5

[8]) Concerning power dissipation and thermal requirements the IC is designed for the maximum V_{thOVLO}.

[9]) The Gate driver circuit of the HSDs sinks current, if the HSDs are switched off.

[10]) T_a=125°C is the test temperature. Beyond this, values are valid up to 132°C (for information only).

[11]) Not available at V_{SUP}<UVLO. This parameter will be tested at V_{SUP}=7.6V and then extrapolated to 7.1V

Parameter HALLSUP	#	Conditions	Symbol	Min	Typ	Max	Unit
Output voltage	20.01	$I_{HALLSUP}$=0, V_{SUP}≥5.5V	$V_{HALLSUP0}$	4.35	12	15	V
	20.02	$I_{HALLSUP}$=20mA, V_{SUP}≥5.5V	$V_{HALLSUP}$	4.35	11	14	V
Short circuit current	20.03	V(**HALLSUP**)≤$V_{HALLSUP}$ -4V, Ta≥125°C	$I_{scHALLSUP}$ [12])	-120	-70	-25	mA
	20.04	V(**HALLSUP**)≤$V_{HALLSUP}$ -4V, Ta≥-40°C	[12])	-240		-25	mA

Parameter TRIGOUT	#	Conditions	Symbol	Min	Typ	Max	Unit
Saturation voltage	15.01	I_{force}<25mA, Ta≤25°C	V_{SAT25}			0.4	V
	15.02	I_{force}<25mA, 125°C<Ta<25°C	V_{SAT}	linearly interpolated from 0.4V to 0.6V versus 125°C<Ta<25°C			
	15.03	I_{force}<25mA, Ta≥125°C	V_{SAT125}			0.6	V
Leakage current	15.04	$V_{TRIGOUT}$=16V, **TRIGOUT**=Z	I_{LK}			10	µA
Short circuit current	15.05	26.5V>$V_{TRIGOUT}$>2V	$I_{scTRIGOUT}$	30	50	90	mA
	15.06	2V>$V_{TRIGOUT}$>1V		30		240	mA
Clamping voltage	15.07	$I_{TRIGOUT}$ = 200µA	$V_{clTRIGOUT}$	42	50	62	V

2.1.2 Thermal shutdown

Parameter	#	Conditions	Symbol	Min	Typ	Max	Unit
Thermal shutdown temperature	07.10	[13])	T_{SD}	150	160	170	°C
Thermal shutdown hysteresis	07.11		ΔT_{SD}	5		15	°C

2.1.3 Inputs

Parameter	#	Conditions	Symbol	Min	Typ	Max	Unit
Thresholds of **DIR**	04.01	[14])	V_{thL}	1.5			V
	04.02	[15])	V_{thH}			3.5	V
	04.03		V_{HYS}	0.6	1.3	1.8	V
Thresholds of **INVDIR**, **MODE** and **TRIGIN**	03.01	[16])	V_{thL}	0.8			V
	03.02	[17])	V_{thH}			2.4	V
	03.03		V_{HYS}	100	250	400	mV
Pull up current of **DIR, INVDIR**, **MODE** and **TRIGIN**	03.04	VIN=2.4V	I_{PU_MODE}	-60	-25	-10	µA
Pull down current **TESTIN**	34.01	1.5V≤ V_{TESTIN}≤5V	I_{pdTEST}	10	30	60	µA

12) Not tested in production, verified during prototyping.
13) T_{SD} = Junction temperature. Guaranteed by design.
14) Voltages = 1.5V must be recognized as low level.
15) Voltages = 3.5V must be recognized as high level.
16) Voltages = 0.8V must be recognized as low level.
17) Voltages = 2.4V must be recognized as high level.

2.2 AC Characteristics

2.2.1 Motor Drivers

Parameter OUTA/OUTB	#	Conditions	Symbol	Min	Typ	Max	Unit
Propagational delay [18]	07.12	Switching delay to LS ON	T_{LSON}			10	µs
	07.13	Switching delay to LS OFF	T_{LSOFF}			25	µs
	07.14	Switching delay to HS ON	T_{HSON}			25	µs
	07.15	Switching delay to HS OFF	T_{HSOFF}			25	µs
Slew rate [19]	07.16	Falling edge, R_{LOAD}=24Ω		12		36	V/µs
	07.17	Rising edge, R_{LOAD}=24Ω		1.5		15	V/µs

2.2.2 RC Timer function

Parameter RC	#	Conditions	Symbol	Min	Typ	Max	Unit
Resistor value range	34.01			50		500	kΩ
One-shot Time-out period	34.02	Rext = 200kΩ [20]	$T1_{timed}$	0.86	1	1.14	s
	34.03	Rext = 50 … 500kΩ [21]	$T1_{timed}$	Rext / 232kΩ	Rext / 200kΩ	Rext / 175kΩ	s
	34.04	Rext = 200kΩ [22]	$T1_{triggered}$	1.72	2	2.28	s
	34.05	Rext = 50 … 500kΩ [17]	$T1_{triggered}$	Rext / 116kΩ	Rext / 100kΩ	Rext / 87.5kΩ	s
Delay time in case of direction reversal operations	34.06	Rext = 50 … 500kΩ [17]	D1	Rext / 7.3MΩ	Rext / 6.4MΩ	Rext / 5.5MΩ	s
	34.07	Rext = 200kΩ	D1		31.25		ms
Fault condition debouncing time	34.10	Rext = 50 … 500kΩ [17]	t_{bfault}	Rext / 300kΩ	Rext / 200kΩ	Rext / 100kΩ	ms
	34.11	Rext = 200kΩ	t_{bfault}		1		ms

[18]) For information only. Guaranteed by design and verified during prototyping. The propagational delay is an internal delay, which cannot be measured in production. It ensures the break-before-make feature of the H-bridge.

[19]) Guaranteed by design, not tested in production and verified during prototyping.

[20]) Timed Shutdown Mode.

[21]) Tested on three points with 50kΩ, 200kΩ and 500kΩ.

[22]) Triggered Shutdown Mode.

3 Functional Description

3.1 Block Diagram

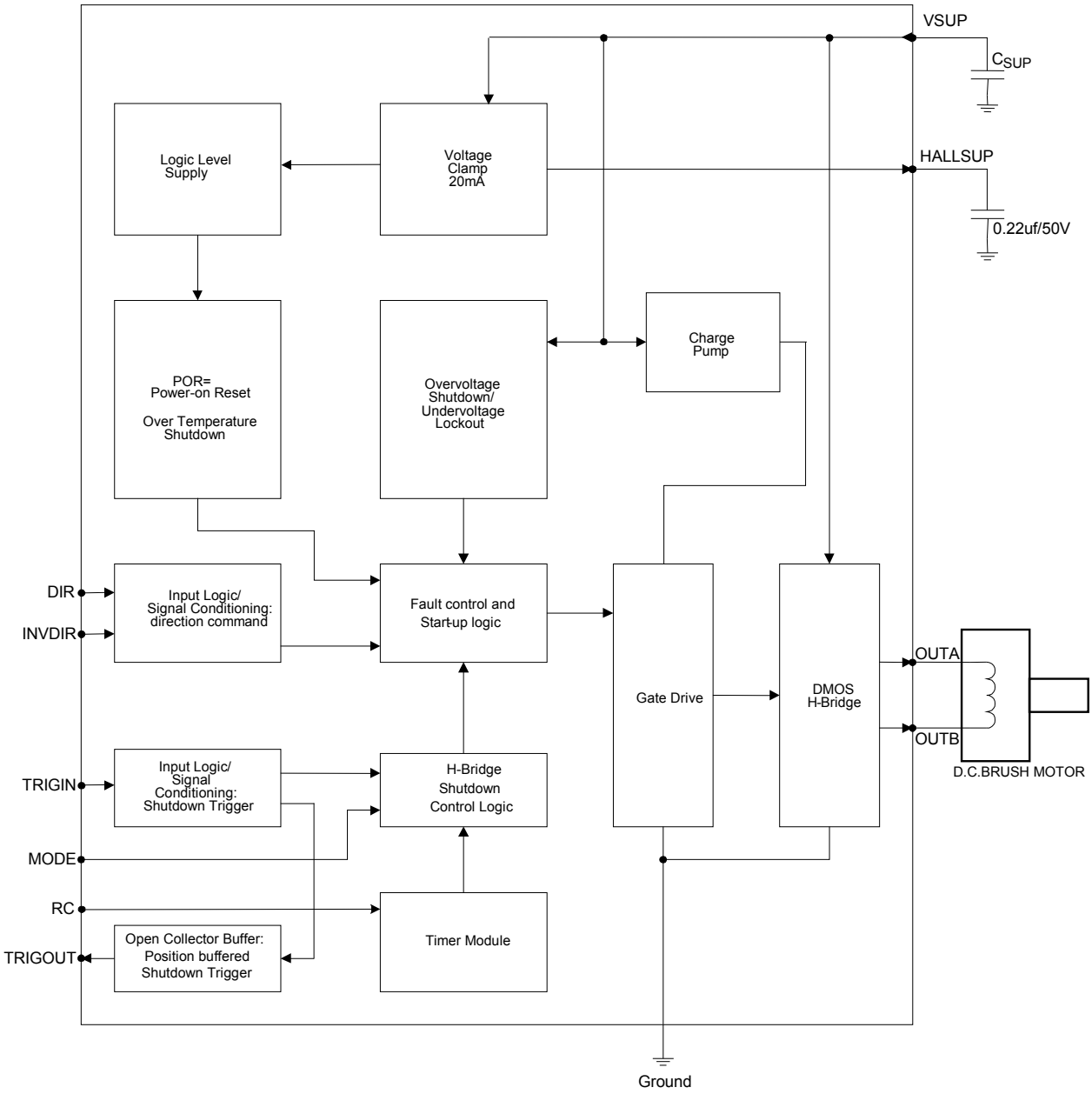


Figure 3.1-1 Functional block diagram of the IC

3.2 Detailed Functional Description

The IC contains a H-bridge for driving a DC motor bi-directionally. The internal support logic takes care that at each state change of the H-bridge the active output driver transistors get switched off first (break before make). As soon V_{SUP} reaches V_{thPORH} the IC awakes from reset. After reset the Motor is braked. Both low side drivers are switched on.
The IC supports two modes of operations: *Timed Shutdown* and *Triggered Shutdown*. The mode of operation is selectable via a logic level input pin **MODE** on the IC. An internal 25µA pull-up pulls the **MODE** pin up to the internal 5V-supply voltage.

3.2.1 Timed Shutdown Mode of Operation: MODE=open (high)

This mode of operation is selected by a logic high signal applied to the **MODE** pin. Due to the internal pull-up the Timed-Shutdown mode is selected simply by leaving the **MODE** pin open (nc).

This mode of operation provides one-shot timed control of the H-bridge in response to a transition on the **DIR** input. In the steady state, the H-bridge will revert to a motor braking function, that is, both low-side drivers of the H-bridge will shunt the DC motor terminals to ground. Upon a valid transition of the **DIR** input, the 1-second one-shot Timer is activated, along with the H-bridge, to drive the DC motor in the specified direction (see table in the „Normal Operation“ section that follows). Assuming a stable **DIR** input, the Timer will timeout after the 1-second duration (T1) and the control logic will then revert to the steady-state condition of „braking“ the motor (low-side switches on).

Should the **DIR** experience another state change midst the Timer operation (mid-travel reversal), the control logic brakes immediately the motor (both low-side drivers on) for a period of t_{dref} (nominally 31ms) followed by a restart the one-shot Timer and H-bridge polarity reversal (to support mid-travel reversal **DIR** request). See state table *Tab. 3.2.1-1* for details.

After POR the IC enters its normal operation mode. The IC controls the H-bridge according to the **DIR** input, the current state of the H-bridge, and the state of the one-shot Timer.

Transition on DIR Pin (@T0+)	T0- State		T1 State One-shot Timed		T2 State		Comments
	OUT A	OUT B	OUT A	OUT B	OUT A	OUT B	
↑	-	-	+	-	-	-	Motor runs →
↑	-	+	+	-	-	-	Direction Reversal
↓	-	-	-	+	-	-	Motor runs ←
↓	+	-	-	+	-	-	Direction Reversal

Tab. 3.2.1-1: State table for the outputs OUTA and OUTB in Timed-Shutdown Mode.
„-„ = GND-level, „+„ = VSUP-level
T0+ represents the state at DIR transition.
T0- represents the state prior to DIR transition.
T1 represents One-shot timed H-bridge the state of nominal 1-second duration.
T2 represents the post-Timer period and final stable state.

Prior a direction reversal operation the delay time D1 (nominally 31ms) is added in order to prevent high peak currents. During D1 the IC breaks the motor (both low sides switches on). The One-shot Timer restarts after D1 on a reversal condition (new Timer event of 1s).
A „-„ state for both OUTA and OUTB represent motor braking with both low sides of the H-bridge shorting the motor leads to ground.

3.2.2 Triggered Shutdown Mode of Operation: MODE=low

This mode of operation is selected by a logic low signal applied to the **MODE** pin. This is accomplished by simply grounding the **MODE** pin.

This mode of operation provides control of the H-bridge in response to a transition on the **DIR** input and feedback from the **TRIGIN** pin. In the steady state the H-bridge will revert to a motor braking function (both low-side drivers of the H-bridge shunts the DC motor terminals down to ground). Upon a valid transition of the **DIR** input, the H-bridge is activated to drive the DC motor in a specified direction (see the state table *Figure 4.2.2-2*) and the one-shot Timer is started. The H-bridge remains in this state until one of either two conditions are met: the appropriate Shutdown Trigger signal state is applied, or the one-shot Timer times out. After one of these conditions is met, the control logic brakes the motor by turning on both low-side drivers of the H-bridge. This is the steady-state condition.
The one-shot Timer serves only as a safety function. In normal operation the Shutdown Trigger event on the **TRIGIN** pin occurs prior to a time out event. If for some reason the DC motor encounters a stall condition or the Shutdown Trigger signal faults, the one-shot timer will disable the drive stage (motor braking function), protecting the DC motor and the IC from excessive current.
A rather immediate reversal is possible if the **DIR** transitions at the exact moment that the previous move terminates. This can result in excessive peak currents. In order to avoid high peak transients, the IC adds D1 (nominally 31ms) under this „transient“ reversal condition.

Name	Value	Unit
D1	31	ms
T1	2000	ms

Table 3.4.2-1 Delay times for the Flow Chart

After POR the IC waits first 31ms (D1) before it enters its normal operation mode. The IC controls the H-bridge according to the **DIR** input, the current state of the H-bridge, and the state of the one-shot Timer (*Figure 3.4.2-1*)

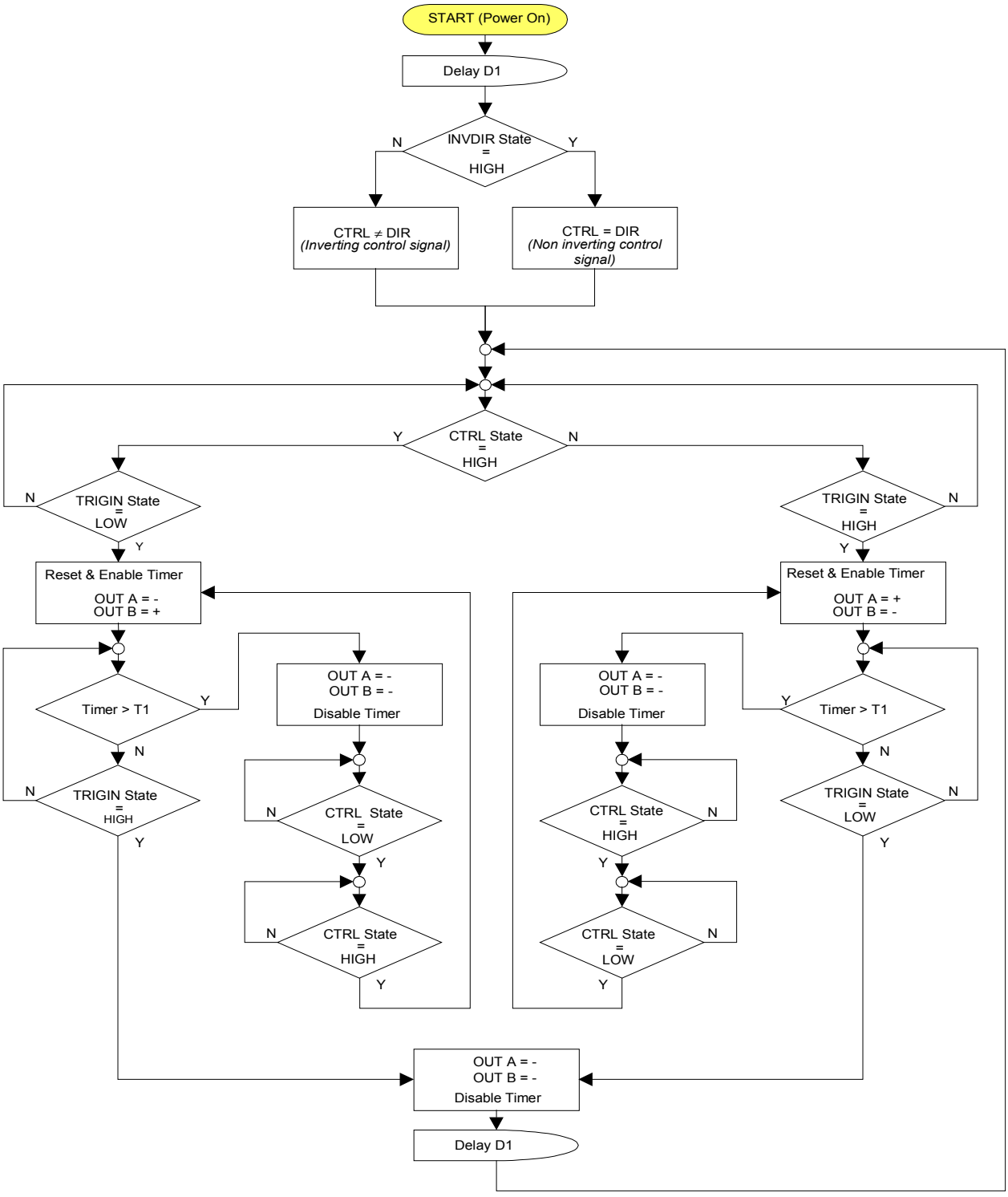


Figure 3.2.2-1 Control Flow Chart of normal operation in triggered shut down mode

INVDIR state	**DIR** state	**TRIGIN** state	One-Shot Timer (T1) state	H-Bridge				Comments
				Current State		Next State		
				OUT A	**OUT B**	**OUT A**	**OUT B**	
Example of normal run								
0	0	1	0	-	-	-	-	Rest position
0	1	1	0	-	-	-	+	Start motion
0	1	1	0	-	+	-	+	Motion in progress
0	1	0	0	-	+	-	-	Brake DC motor, wait 31 ms
Example of normal run with immediate reversal (DIR changes during motion)								
0	0	1	0	-	-	-	-	Rest position
0	1	1	0	-	-	-	+	Start motion
0	0	1	0	-	+	-	+	Motion in progress
0	0	0	0	-	+	-	-	Brake DC motor, wait 31 ms
0	0	0	0	-	-	+	-	Starts motion
0	0	0	0	+	-	+	-	Motion in progress
0	0	1	0	+	-	-	-	Brake DC motor, wait 31 ms
Example of Timeout with re-trial (and second timeout)								
0	1	0	0	-	-	-	-	Rest position
0	0	0	0	-	-	-	+	Start motion
0	0	0	0	-	+	-	+	Motion in progress
0	0	0	1	-	+	-	-	Timeout - Break DC motor
0	0	0	0	-	-	-	-	Wait for DIR event (High)
0	1	0	0	-	-	-	-	Wait for DIR event (Low)
0	0	0	0	-	-	-	+	Re-Start motion
0	0	0	0	-	+	-	+	Motion in progress
0	0	0	1	-	+	-	-	Timeout - Brake DC motor
Example of normal Initialization								
0	0	0	0	-	-	-	-	Rest position
0	1	1	0	+	-	-	-	Break DC motor, wait 31 ms
0	0	0	1	-	+	-	-	Timeout - Brake DC motor
0	0	1	0	+	-	-	-	Brake DC motor, wait 31 ms
0	0	0	0	-	+	-	-	Brake DC motor, wait 31 ms
Example of normal run with inverted DIR logic								
1	0	0	0	-	-	-	-	Rest position
1	1	0	0	-	-	+	-	Start motion
1	1	0	0	+	-	+	-	Motion in progress
1	1	1	0	+	-	-	-	Brake DC motor, wait 31 ms
LOW =0 HIGH = 1	LOW =0 HIGH = 1	LOW =0 HIGH = 1	0 = No Timeout 1 = Timeout					
Note: OUT A = - and OUT B = - is called “braking” the DC motor								

Table 3.4.2-2 State Table for triggered Shutdown Mode

3.2.3 One-shot retriggerable Timer

The pin **RC** provides a terminal for an external resistor that determines the frequency of an internal oscillator. The delay time T1 (1s or 2s) of the one-shot retriggerable Timer is generated digitally from its output frequency. Also the time D2 (31 ms) is generated from this oscillator output.

3.2.4 Voltage clamp for the Hall Cell HALLSUP

The IC contains a clamped 12V voltage supply. It is used as the supply voltage source for an Allegro 3281 series Hall Cell for protecting it against voltages higher than 16V.

3.2.5 Buffered shutdown trigger output TRIGOUT

In normal operation, a Hall Cell open-collector output feeds the pin **TRIGIN**. This Hall Cell is also responsible for providing position information to an external control module (customer interface). This externally reported position requires an open-collector output. In order to avoid contention at the Hall Cell's open-collector output due to the interaction of the IC's internal pull-up on the **TRIGIN** pin and the pull-up at the customer interface (for position reporting), a buffered/isolated Hall Cell output is provided by the pin **TRIGOUT**.

3.2.6 Over Temperature, Over Voltage and Under Voltage Shutdown

The IC monitors the temperature and V_{SUP}, the voltage on the **VSUP** pin and protects itself against conditions out of the normal operating limits. In particular the following three conditions are continuously monitored: *Over-temperature*, *Under Voltage*, and *Over Voltage*. The fault strategy includes non-latching and self-clearing strategy for recovery. The function of the **TRIGOUT** pin is not effected by any fault conditions. It remains valid. The response of all fault conditions is delayed by the debouncing time t_{bfault}, so that short glitches have no impact on the application.

In the event of an Over Temperature condition, the IC disables the four drivers of the H-bridge output to avoid damage due to excessive current. The control logic ignores processing of the **DIR**, **TRIGIN**, and One-shot Timer activity. Upon clearing of the fault condition, the IC carries out a Power-On-Reset and arm the One-shot Timer prior to any processing of the **DIR** or **TRIGIN** signals. The IC resumes immediately if the Tj is lower than T_{SD} and the fault is clear.

The Over Voltage event is detected, if the V_{SUP} is higher than the V_{thOVLO}. In order to protect the high side drivers the IC shuts down only these. That means if the IC is in „brake„-mode, nothing changes. If the IC is in „driving„-mode, one side of the H-bridge is high Z and the timer is frozen. This behavior reduces the effect of an Over Voltage event on the application to a minimum.
The control logic ignores processing of the **DIR**, **TRIGIN**, and One-shot Timer activity. The IC resumes immediately if V_{SUP} is lower than V_{thOVLO} and the fault is cleared.

The Under Voltage event is detected, if the V_{SUP} is lower than the V_{thUVLO}. The IC disables the high side drivers of the H-bridge and brakes the motor. The control logic ignores processing of the **DIR**, **TRIGIN**, and One-shot Timer activity. Upon clearing of the fault condition, the IC arms the One-shot Timer prior to any processing of the **DIR** or **TRIGIN** signals. The IC resumes immediately if V_{SUP} is larger than V_{thUVLO} and the fault is cleared.

Conditions			H-bridge						Comments
Over Temperature	Under Voltage	Over Voltage	State before trouble			State after trouble			
			OUTA	OUTB	*Motor*	OUTA	OUTB	*Motor*	
-	-	-	H	L	+	H	L	+	Motor runs positive
-	-	-	L	H	-	L	H	-	Motor runs negative
-	-	-	L	L	Brake	L	L	Brake	Motor is braked
+	X	X	X	X	X	Z	Z	Z	IC in RESET
-	+	-	H	L	+	L	L	Brake	Motor is braked
-	+	-	L	H	-	L	L	Brake	Motor is braked
-	+	-	L	L	Brake	L	L	Brake	Motor is braked
-	-	+	H	L	+	Z	L	Z	Motor is free
-	-	+	L	H	-	L	Z	Z	Motor is free
-	-	+	L	L	Brake	L	L	Brake	Motor is braked

Tab. 3.2.6-1: Effect of trouble conditions on the motor. OUTX=H means $V_{OUTX}=V_{SUP}$, OUTX=L means V_{OUTX}=GND, OUTX=Z means H-bridge in high Z.

3.2.7 Test modes

The IC provides three test modes, which eases the test and measurement of the IC. The test modes are accessed by positive transitions on the **TESTIN** pin. Although there is a 30µA pull down integrated it is strongly recommended to connect the **TESTIN** pin in the final application to GND!

Test mode	Access code/ condition	Description
#1	One positive transition on **TESTIN**	In this test mode **TRIGOUT** doesn't show an image of **TRIGIN**, but is the output of an exor-chain. Connected to this exor-chain are all input Schmitt-triggers and the comparator outputs for under voltage, over voltage and over temperature monitoring. Thus all thresholds can be measured in this test mode.
Thermal shutdown threshold	Force a current of 0 … 2mA in the **TESTIN** pin	Staying in test mode #1 the threshold of the over temperature monitoring can be reduced by forcing a current in the **TESTIN** pin. The ratio between the pull down current and this forced current is a measure for the shut down temperature. See description below.
#2	2nd positive transition on **TESTIN**	In this test mode one half of the H-bridge is disabled. Pin 12 and 25 remain in high-Z state and it is possible to use these pins as sense connections to the driver transistor on pin 7 and 30 since internal resistors connect pin 7 to pin 12 and pin 25 to 30. Moreover there are resistors between the supply pins 13 and 7 as well as between 24 and 31. So by using pin 6 and 31 as supply pins only the pins 13 and 24 as sense pins, which make an accurate measurement of the high side driver on resistance possible. For the low side drivers one of the GND may be used as sense pin. The oscillator frequency (divided by 32) can be measured on the **TRIGOUT** pin.
#3	3rd positive transition on **TESTIN**	In this test mode the internal oscillator is disabled, a power on reset is performed (except for the test mode control logic) and the 32-bit oscillator frequency divider is bypassed. The **RC** pin serves as input for the external clock. This test mode is designed for a fast digital pattern test.
Normal	4th positive transition on **TESTIN**	The IC will return to normal mode.

Tab. 3.2.7-1: Test mode functions and access pattern

In test mode #1 the thermal shutdown threshold can be measured by forcing a certain current in the **TESTIN** pin. This current reduces the thermal shutdown threshold to the current test temperature T_{test}.

With
I_{force} = forced current for reducing the threshold, I_{pdTEST} = pull down current of the **TESTIN** pin,
T_{sdH}= real thermal shut down temperature without a forced current and
T_{sdL}= real thermal recovery temperature without a forced current

$$T_{sdH} = X_H \cdot \frac{I_{force} - I_{pdTEST}}{I_{pdTEST}} + T_{test} \qquad T_{sdL} = X_L \cdot \frac{I_{force} - I_{pdTEST}}{I_{pdTEST}} + T_{test}$$

The constants X_H and X_L are around 6°C and must be verified during qualification.

3.3 Application Circuit

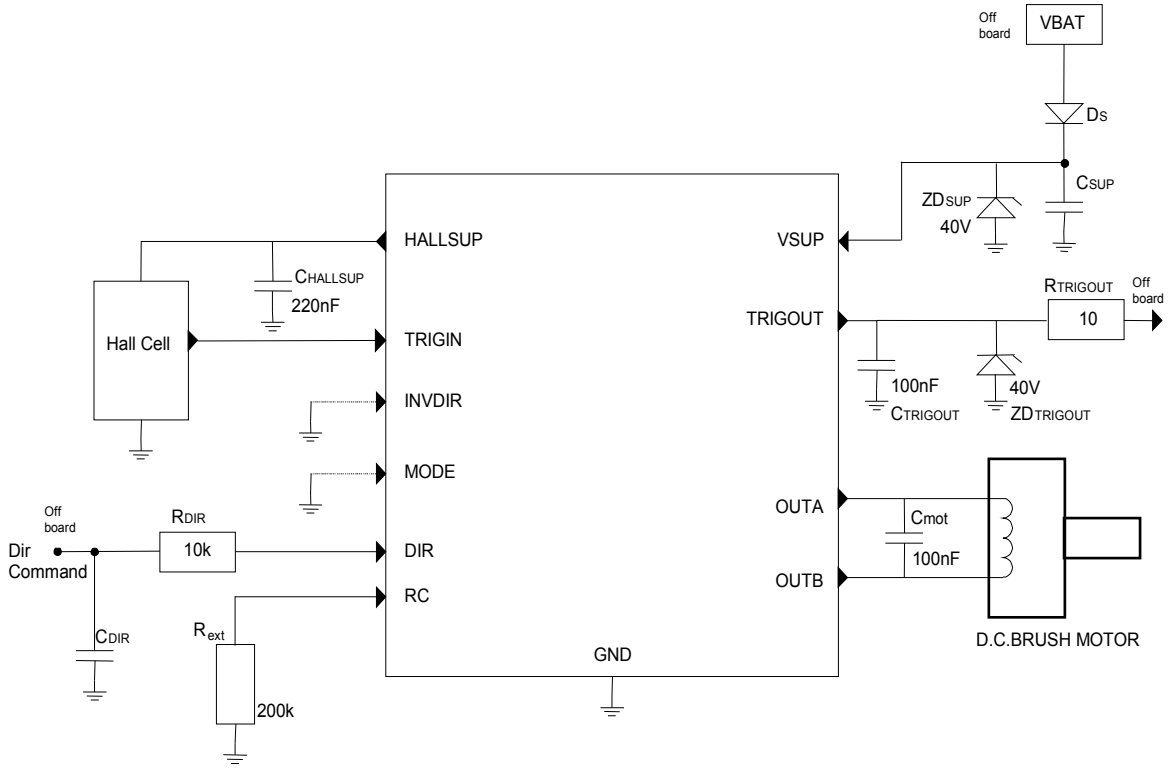


Figure 3.3-1 Application diagram of the IC, CDIR is optional, for the protection circuitry refer to chapter 4.4.

3.3.1 Application notes

This IC is designed for conditions described in chapter 2.1 and 2.2. If the electrical environment is rougher than specified in chapter 2.1 a sufficient protection circuitry is required to absorb destructive energies off the IC. Please refer to figure 4.3-1 and to chapter 4.4.
For proper operation of the IC the use of the devices RDIR, ZDTRIGOUT and ZDSUP is strongly recommended. The capacitor across the DC motor is required.

3.4 Noise Immunity

The application with the E192.01 is designed to meets the following requirements of ISO 7637:

VSUP				
Parameter	**Condition**	**Cycles**	**Coupling**	**Comment**
Pulse 1	t_1 = 5s / U_S = -100V	100 pulses	direct	A serial (D_S) protection diode is required. A parallel capacitor (C_{SUP}) is recommended.
Pulse 2	t_1 = 0,5s / U_S = 100V	1000 pulses	direct	A Zener-Diode (ZD_{SUP}) is required. [23)]
Pulse 3a/b	ISO 7637 U_S = -150V / U_S = 100V	1000 Bursts	direct	A serial protection diode (D_S) and a Zener-Diode (ZD_{SUP}) is required. A parallel capacitor (C_{SUP}) is strongly recommended. [15)]
Pulse 4	U_S = -6V / U_a = -5V t_8 = 5s	10 pulses	direct	A serial protection diode (D_S) is required
Pulse 5	R_i = 2Ω, t_D = 250ms t_r = 0,1ms U_P+U_S= 40V	10 pulses at 1 minute intervals	direct	A Zener-Diode (ZD_{SUP}) is required. A parallel capacitor (C_{SUP}) is recommended. [15)]

Tab. 3.4-1 Schaffner-Pulses 1, 2, 3, 4 and 5 applicable to battery lines

DIR				
Parameter	**Condition**	**Cycles**	**Coupling**	**Comment**
Pulse 3a/b	ISO 7637 U_S = -150V / U_S = 100V	1000 Bursts	resistive	A serial protection resistor (R_{DIR}≥10kΩ) is required.
	40V for 2min 50V for 500ms	single pulses	resistive	A serial protection resistor (R_{DIR}) is recommended.

Tab. 3.4-2 Noise immunity of pin DIR

TRIGOUT				
Parameter	**Condition**	**Cycles**	**Coupling**	**Comment**
Pulse 3a/b	DIN 40 839 Part 3 U_S = -150V / U_S = 100V	1000 Bursts	capacitive, via 4.7nF	A serial protection resistor ($R_{TRIGOUT}$) + a capacitor ($C_{TRIGOUT}$=22nF for a couple capacitor of 4.7nF) is recommended. Alternatively a Zener-Diode ($ZD_{TRIGOUT}$) is recommended. [24)][15)]
Pulse 3a/b	DIN 40 839 Part 3 U_S = -150V / U_S = 100V	1000 Bursts	direct	A Zener-Diode ($ZD_{TRIGOUT}$) is required. [15)]
	40V for 2min 50V for 500ms	single pulses	resistive	A serial protection resistor ($R_{TRIGOUT}$) is recommended.

Tab. 3.4-3 Noise immunity of pin TRIGOUT

[23)] The Zener Diode should have a clamping voltage of about 30 to 45V.

[24)] The expenditure of external protection circuitry is depending on the size of the couple capacitor, thus on the energy reaching the IC.

3.5 ESD Protection

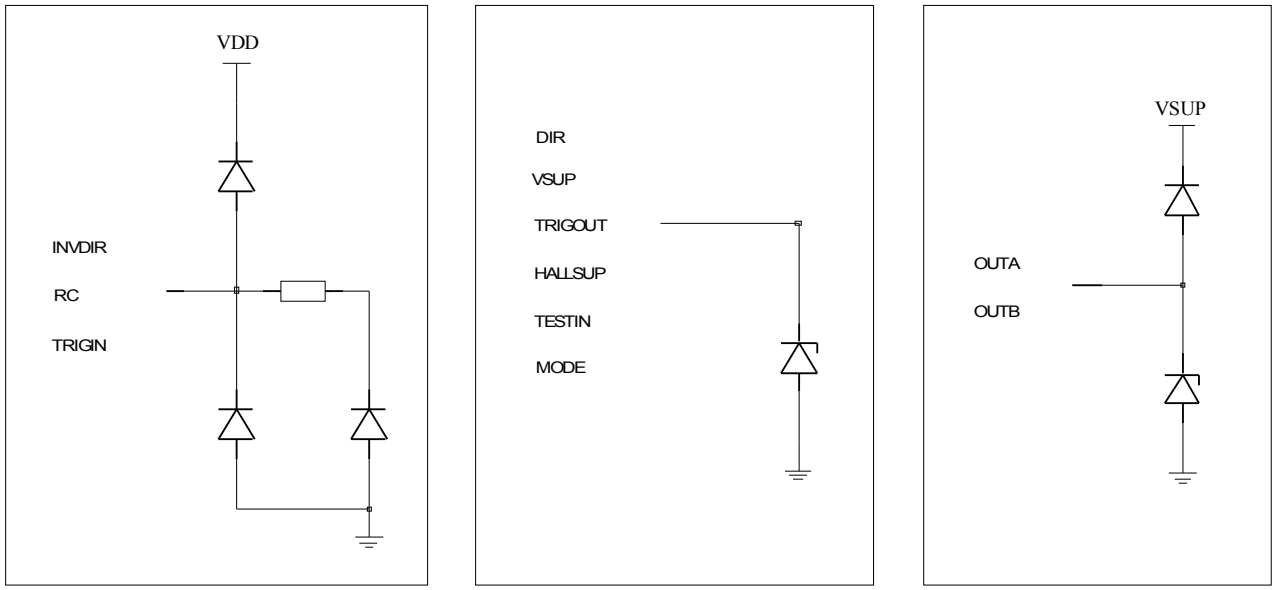


Fig. 3.5-1 ESD-Structures

Test Method:

The ESD Protection circuitry is measured using „Human Body Model“ (JESD22A114A) and „Machine Model“ (JESD22A115A) with the following conditions:

	Human Body Model	Machine Model	Unit
V_{IN}	2000	200	V
R_{EXT}	1500	0	Ω
C_{EXT}	100	200	pF

Tab. 3.5-1 ESD-Test Models

4 Handling, Packing

4.1 Handling

Devices are sensitive to damage by Electro- Static Discharge (ESD) and should only be handled at an ESD protected workstation.

4.2 Packing

SMD devices are taped in acc. to DIN IEC 286 part3.

JEDEC A112 Level 3 SMD devices are dry packed.

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