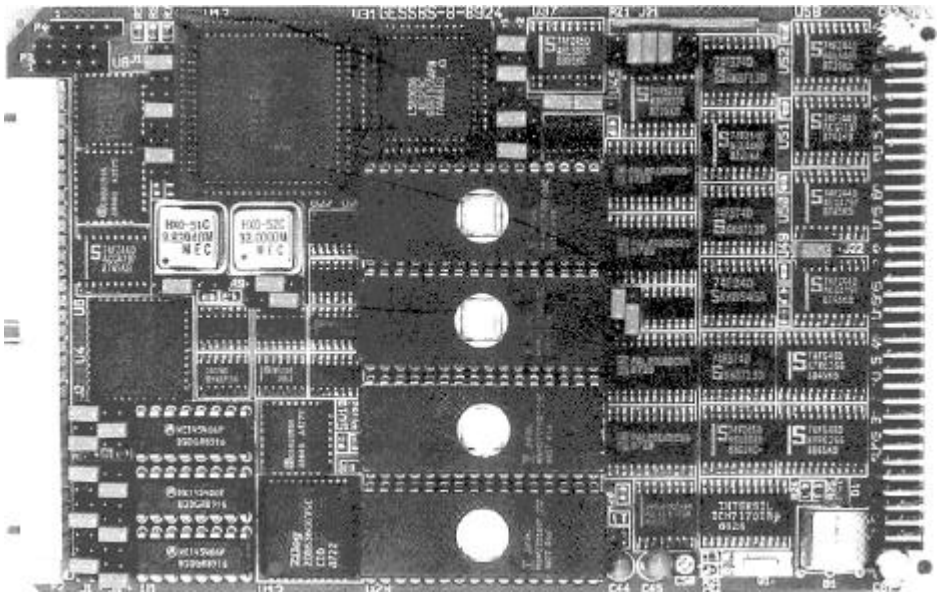
Gespac	GESSBS-8
	PROCESSOR

8OC186 SINGLE BOARD SYSTEM

The GESSBS-8 Single Board System is a general purpose, 16-bit computer system on the G-96 Bus. This state-of-the-art product offers unique features in a single Eurocard format. Designed around the powerful 80CI 86 processor running at 16 Mhz, this module has 256 Kbytes of zero wait-state CMOS RAM. Four 32-pin JEDEC sockets support up to 512 Kbytes of EPROM or 256 Kbytes of EPROM plus 256 Kbytes of SRAM. The unused memory area is available on the G-96 Bus in the VMA field and allows system memory extension. All basic 1/0 such as timers, RS-232, interrrupt controllers, Real-time Clock/Calendar, and parallel 1/0 are implemented on-board providing a complete system suited to most embedded applications. Additionally, an 80C187 coprocessor can be added for high performance numerics processing.

Technical features

- 8OC186-16 microprocessor (16 Mhz)
- 256 Kbytes of CMOS static RAM protected against power-failure
- Up to 512 Kbytes of SRAM and 256 Kbytes of EPROM or up to 256 Kbytes of SRAM and 512 Kbytes of EPROM
- Total addressing capability up to 1 Mbyte
- Two independent synchronous/asynchronous Serial Channels (85C30)
- Three 16-bit counters/timers (82C54)
- Three 8-bit bidirectionnal 1/0 ports (82055)
- Optional numeric coprocessor 8OC1 87-16 (16 Mhz)
- 1 DMA channel available on the external connector (coupled with the 82C55)
- Real-time Clock/Calendar with 51 bits of SRAM and on-board battery backup
- Two interrupt controllers allowing 5 auto-vectored interrupts on the G-96 Bus
- Internal 1/0 processor (timers and interrupt controller)
- Fully compatible with the G-96 Standard Bus
- Standard power supply: +5 V, +12 V, -12 V



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References

GESSBS-8/256: High performance 8OC186 single board system (1 6 bits) with 256 K SRAM (TTL version)
GESSBS-8U256: High performance 8OC186 single board system (1 6 bits) with 256 K SRAM (CMOS version)
GESSBS-8F/256: Idem GESSBS-8 with BOC187-16 Numeric Processor
GESSBS-8LF/256: Idem GESSBS-8L with 80C187-16 Numeric Processor

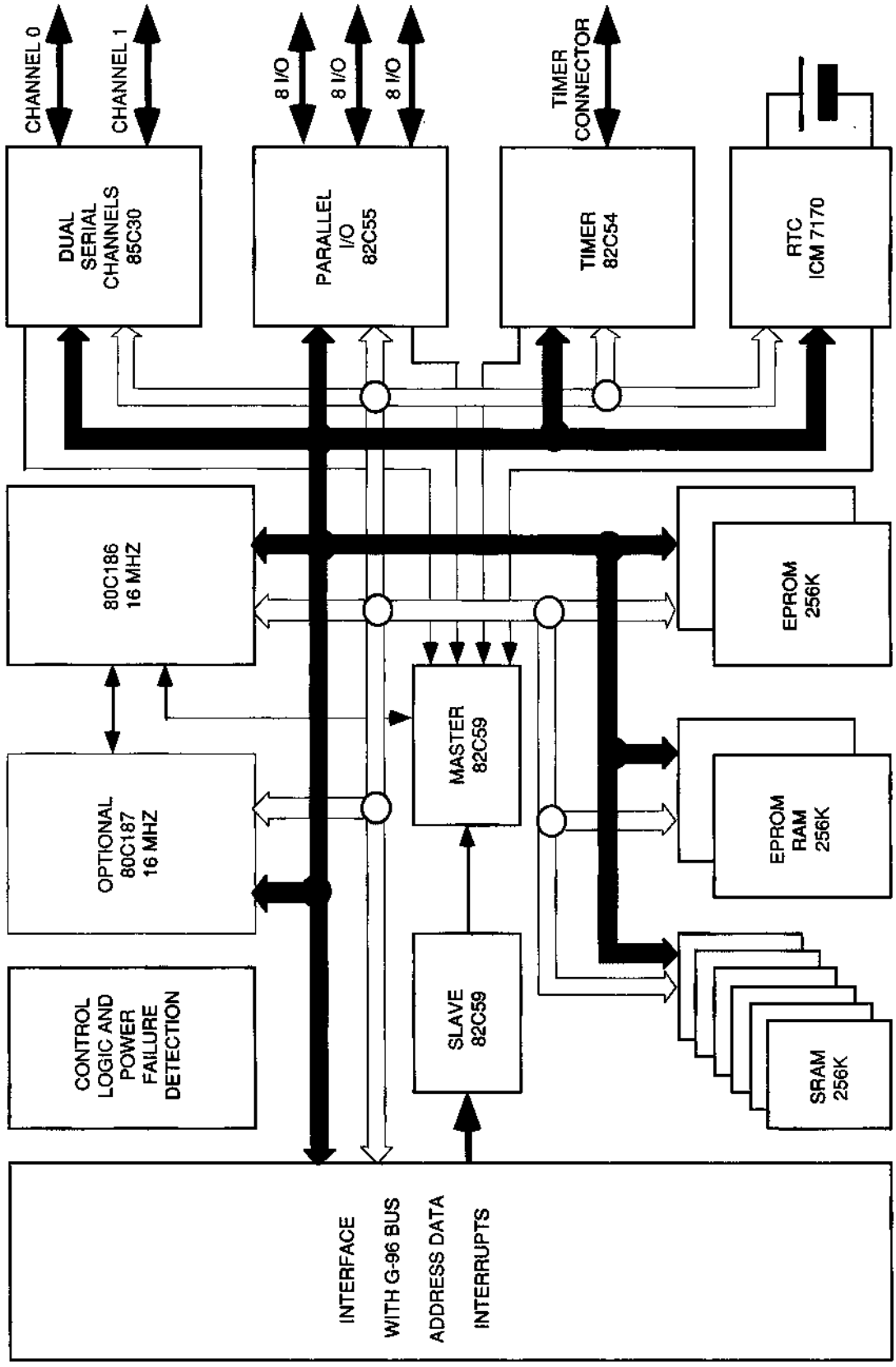


Figure1.1 Block Diagram

1. GENERAL INFORMATION

1.1 DESCRIPTION

Using surface mount devices on both sides and state-of-the- art PCB technology, GESPAC offers a complete 8OC186 system in single Eurocard format. Designed around the advanced, high integration 80CI 86 microprocessor running at 16Mhz, the GESSBS-8 board is upward compatible with 8086, 8088, and 80286 software. When equipped with the numeric processor extension (80CI 87-16), the GESSBS-8 module provides a solution for high performance numerics processing. The 8OC187 is upward object-code compatible with the 8087 numeric coprocessor and completely object- code compatible with the 80387 numeric coprocessor.

The GESSBS-8 module has 256 Kbytes of CMOS RAM with zero wait-state. A power-failure logic circuit with an external battery provides data integrity in static RAM. Four 32-pin JEDEC sockets support up to 512 Kbytes of EPROM or 256 Kbytes of EPROM plus 256 Kbytes of static RAM. The EPROM/RAM extension can operate from zero to three wait- states. The unused memory area can be addressed on the G-96 Bus allowing full I Mbyte 80CI 86 addressing capability.

The GESSBS-8 module includes a dual-channel Serial Communication Controller (SCC 85C30). The SCC can be software-configured to satisfy a variety of serial communication applications, and includes on-chip baud rate generators. These serial channels can be configured as DCE and DTE connection to allow downloading, uploading or other useful functions. The board contains three 16-bit timers providing many functions typically required for multitasking systems such as real-time clock function, measurement of elapsed time or events counting. A CMOS Real-time Clock/Calendar with on-board battery backup gives complete time information (year, month, day, h, m, s), multiple RTC interrupts and additionally, 51-bits of RAM which can be used for storing the system configuration.

The module includes a 82C55 general purpose programmable 1/0 device. It provides 24 1/0 pins which may be programmed in two groups of twelve, used in three major modes of operation (input, Output or bidirectional bus with handshaking).

The GESSBS-8 board was designed to provide a powerful interrupt structure to increase efficiency and versatility (i.e, iRMX86 mode interrupt structure). A master interrupt controller manages the internal interrupt sources; a slave interrupt controller manages five auto-vectored interrupts through the G-96 Bus. The 8OC186 NMI line can be routed on the G-96 Bus PWF or NMI line, or time-out logic in the case of addressing an asynchronous area not present on the bus.

The GESSBS-8 module is fully compatible with the G-96 Bus as described in the GESPAC *G-64IG-96 Bus Specification Manual* and can be used with all asynchronous or synchronous G-64/G-96 1/0 modules. The block diagram in Figure 1.1 illustrates the different module parts.

1.2 SPECIFICATION

CPU Clock	16 Mhz
Addressing capability Internal memory:	
TOP EPROM: I	From 8 Kbytes to 256 Kbytes (two 271 001) 0 - 3 programmable wait-states
LOW RAM	256 Kbytes of CMOS static RAM 0 wait-state for GESSBS-8 1 wait-state for GESSBS-8L
MEDIUM MEMORY	From 16 Kbytes to 256 Kbytes RAM or EPROM 0 - 3 programmable wait-states
External Memory	From 256 Kbytes to 512 Kbytes (On-board memory dependent)
External peripherals	I K x 16 Asynchronous 1 K x 16 Synchronous
Internal peripherals:	
Coprocessor:	Optional 8OC1 37-16 (16 Mhz) Serial
controller:	Two RS-232 type or synchronous, SDLC,HDLC
Baud Rate:	Software programmable to 38,4 Kbits/s in RS-232 (quartz = 4,9152 Mhz)
Timers:	Three independent 16-bit counters/timers (8254) and three internal 80186 16-bit timers
Parallel 1/0:	24 general purpose 1/0 pins (8255)
Real Time Clock:	Year, month, day, hours, minutes, seconds, periodic interrupts, alarm and 51 bits of non-volatile RAM
Interrupts:	Two external interrupt controllers
Master:	Handles internal interrupts
Slave:	Handles five G-96 interrupt lines
80186 int. controller	Slave mode wired on the master -
Bus Interface:	Address bus: tri-state TTL compatible - Data bus: tri-state TTL compatible -Other signals: TTL compatible 8- or
Bus Data Transfer:	16-bit Sync/Asynchronous
Power requirements. (GESSBS-8/256) (TTL Version)	+ 5 V / 1.7 A typ. (TTL version) +1 2 V / 20 mA typ. (TTL version) -1 2 V / 20 mA typ. (TTL version)
Power requirements (GESSBS-8U256) (CMOS Version)	+ 5 V / 0.320 A typ. +1 2 V / 20 mA typ. -1 2 V / *20* mA typ.
Operating temp.:	+ 5' to +55' C (TTL version)
PCB dimension:	100 x 160 mm

Table 1.1 Specifications

1.3 MEMORY MAP

The GESSBS-8 was designed to provide maximum internal addressing capability minimizing the access time during memory cycles. The 80186 CPU includes integrated chip selection logic used to enable memory devices. Memory chip selection lines are split into three groups that separately address major memory areas. Only two chip selection lines are used inside the GESSBS-8 module: UCS upper memory for resetting ROM and LCS lower memory chip selection for system RAM. Other memory areas (internal RAM/EPROM extension and VMA signal) are hardware decoded. The UCS and LCS area sizes are programmable. Starting and ending locations of lower and upper memory are fixed at OOOOOH and OFFFFFH, respectively. The starting location of mid-range memory (internal RAM/EPROM extension) is programmable via a set of jumpers. Each programmed chip selection area has a set of associated programmable ready bits. These readybitscontrolthe8OCl 86 integrated wait-state generator. This allows a programmable number of wait-states (O - 3) to be automatically inserted whenever an access to a particular chip selection area is made. LCS size is fixed at 256 Kbytes and the UCS size is dependent on the user installed EPROM. Table 1.2 shows the GESSBS-8 standard memory map and Tables 1.3, 1.4 and 1.5 show examples using the internal extension memory sockets with different EPROM/RAM sizes. Refer to Section 4 for EPROM/RAM wait-state considerations.

Device/Field	CPU byte address	G-96 Bus word address
EPROM Top	FFFH	none
EPROM Base 2764 27128 27256 27512 271001	 FC 000H F8 000H F0 000H E0 000H C0 000H	none
VMA or Mid-Range Top address when using		
2764 27128 27256 27512 271001	FB FFFH F7 FFFH EF FFFH DF FFFH BF FFFH	7D FFFH 7B FFFH 77 FFFH 6F FFFH 5F FFFH
VMA or Mid-Range Base address		
	40 000H	20 000H
Internal SRAM Top Address Base Address	 3F FFFH 00 000H	 none none

Table 1.2 Memory Map

Device/Field	CPU byte address	G-96 Bus word address
2 x 2764 installed on U24 and U26 sockets		
EPROM Top EPROM Base	FF FFFH FC 000H	none none
2 x 2764 installed on U23 and U25 sockets		
Mid-Range Top address Mid-Range Base address	FB FFFH F8 000H	none none
VMA Top address VMA Base address	F7 FFFH 40 000H	7B FFFH 20 000H
Internal SRAM		
Top Address Base Address	3F FFFH 00 000H	none none

Table 1.3 Memory Map

Four 2764 EPROM located at the top memory area allowing: 32 Kbytes of EPROM, 256 Kbytes of internal SRAM and 736 Kbytes of G-96 VMA area.

Device/Field	CPU byte address	G-96 Bus word address
2 x 271001 installed on U24 and U26 sockets (UCS)		
EPROM Top EPROM Base	FF FFFH C0 000H	none none
VMA Top address VMA Base address	BF FFFH 80 000H	5F FFFH 40 000H
2 x 128 K x 8 SRAM installed on U23 and U25 sockets		
Mid-Range Top address Mid-Range Base address	7F FFFH 40 000H	none none
Internal SRAM		
Top Address Base Address	3F FFFH 00 000H	none none

Table 1.4 Memory Map

512 Kbytes of SRAM located at the bottom memory area and 256 Kbytes of EPROM located at the top memory area plus, 256 Kbytes of G-96 VMA area.

Device/Field	CPU byte address	G-96 Bus word address
2 x 271001 installed on U24 and U26 sockets (UCS)		
EPROM Top EPROM Base	FF FFFH C0 000H	none none
2 x 271001 installed on U23 and U25 sockets		
Mid-Range Top address Mid-Range Base address	BF FFFH 80 000H	none none
VMA Top address VMA Base address	7F FFFH 40 000H	3F FFFH 20 000H
Internal SRAM (LCS)		
Top Address Base Address	3F FFFH 00 000H	none none

Table 1.5 Memory Map

512 Kbytes of contiguous EPROM located at the top of the memory area, 256Kbytesof internal SRAM plus 256 Kbytes of G-96 VMA area.

1.4 1/0 MAP

The 8OC186 CPU supports both 8- and 16-bit I/O devices. The CPU reserves a 64 Kbyte segment for 1/0. Four special 1/0 instructions are available for these communications. The GESSBS-8 module uses this special scheme for addressing the on-board peripheral devices and generating the VPA signal when accessing peripheral devices on the G-96 Bus.

1.4.1 INTERNAL 1/0 ADDRESSES

The GESSBS-8 includes seven internal 1/0 devices: 8530 SCC, two 82C59 Interrupt Controllers, 82C54 Timer, 8OC1 87 Coprocessor, 7170 Real-Time Clock/Calendar, and the 82C55 parallel 1/0 controller. All these devices are connected on data lines DO-07 of the 8OC186 CPU, with only even addresses allowed. The 8OC1 86 generates chip selections for up to seven peripheral devices. The GESSBS-8 module uses the first five chip selection lines (Peripheral Chip Selects PCSO to PCS4) to decode the internal 1/0. These chip selections are active for five contiguous blocks of 128 bytes, above a programmable base address. This base address is located in 1/0 space and must be a multiple of 1 Kbyte. PCS5 and PCS6 are programmed to provide latched address bits Al and A2. GESSBS-8 internal device base addresses are shown in Table 1.6. Refer to Section 4 for wait-state generation and base address selection.

Device	PCS	Base Address
Master Interrupt controller	PCS0	0000H 0002H
Slave Interrupt controller	PCS0	0004H 0006H
Timer	PCS1	0080H 0086H
SCC	PCS2	0100H 0106H
Parallel I/O (82C55)	PCS3	0180H 0186H
Real Time Clock/Calendar	PCS4	0200H 0222H
Coprocessor	Hardware wired	00F8H 00FFH

Table 1.6 Internal 1/0 Map

1.4.2 EXTERNAL I/0 - VPA FIELD

The external I/O field is divided in two banks of 2 Kbytes each, allowing interfacing of the GESSBS-8 with synchronous and asynchronous I/0 modules. The external 1/0 field is characterized on the G-96 Bus by the VPA signal and the AO-A9 address lines (corresponding to Al -Al O of the 8OC186's physical address lines). If the 1/0 module is an 8-bit module, it is connected on DO-D7 lines of the G-96 Bus (corresponding to D8-DI 5 of the 80CI 86's data lines) and is always addressed with ODD addresses.

Due to the redundancy of the two fields, only two Kbytes are available for connecting 1/0 devices. This means that if an asynchronous device is placed at address FOOOH, it is not possible to have a synchronous module connected at address F800H. These CPU addresses relate to the same physical address on the bus. Mapping of the VPA field is shown in Table 1.7.

EXTERNAL I/O VPA FIELD	I/O MAPPED CPU PHYSICAL BYTE ADDRESS	I/O MAPPED G-96 BUS PHYSICAL WORD ADDRESS
Synchronous Field	FFFFH F800H	7FFFH 7D00H
Asynchronous Field	F7FFH F000H	7BFFH 7800H

WARNING: Do not attempt to reference other 1/0 addresses due to the risk of stopping the system indefinitely

Table 1.7 VPA field addresses

1.5 82C59 INTERRUPT CONTROLLERS

The GESSBS-8 includes two 82C59 Priority Interrupt controller chips. The Master device handles interrupts from internal peripherals, and manages the cascade mode for the slave interrupt controller and the 8OC186 integrated interrupt controller. This Master Interrupt Controller must be programmed to operate in the edge sensitive interrupt mode. The Slave interrupt controller receives only the five G-96 interrupts lines. These external interrupts must be programmed as slave devices to allow the auto-vectored mode on the G-96 bus. The 82C59 device must be programmed as a slave and operates in the level interrupt mode. Tables 1.8 and 1.9 show the assignment of 82C59 interrupt inputs.

Level	Priority	Issued from	Input type*
7	Lowest	RTC	non-slave
6		82C59 Slave	slave
5		82C55 / Not used	non-slave
4		80C186 Int. Cont.	slave
3		SCC	slave/non-slave
2		Not used	-
1		82C55 / Not used	non-slave
0	Highest	TIMER	non-slave

* Slave input means the device connected on this input generates its own vector during INTA cycle.
Non-Slave input means the device connected on this input cannot generate vectors.

Table 1.8 Master device interrupt structure

Level	Priority	G-96 Interrupt	Input type**
7	Lowest	not used	-
6		not used	-
5		IRQ5	non-slave
4		IRQ4	"
3		IRQ3	"
2		IRQ2	"
1		IRQ1	"
0	Highest	not used	-

All G-96 Interrupt lines work in the auto-vectored mode. The Slave controller must be programmed to generate the vector during an INTA cycle.

Table 1.9 Slave device interrupt structure

1.6 TIMER

The 82C54 has three independent programmable 16-bit counters, each capable of handling clock input frequencies of up to 10 Mhz. All I/0 signals of the three timers are available on a connector allowing the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, along with many other applications. The OUT0, OUT1 or OUT2 outputs can be routed to the master interrupt line IRQ0 via a jumper. For more information about programming, refer to the *Intel Data Book.* Table 1. IO shows the Timer register addresses.

Base Address	Access	Register Name
0080H	R/W	Counter 0
0082H	R/W	Counter 1
0084H	R/W	Counter 2
0086H	W	Control Word Reg.

Tablel.10 Timer 82C54 register map

1.7 REAL-TIME CLOCK/CALENDAR - ICM 7170

The ICM 7170 chip gives the GESSBS-8 board a real-time clock/calendar functioning from 1/100s to years, and two interrupt functions. First is the periodic interrupt (i.e., 100HZ, 10Hz, etc.) which can be programmed by the internal interrupt control register to provide seven different output signals. Second type is the alarm interrupt. The alarm time is set by loading a 51-bit RAM that activates an interrupt output through a comparator. This 51-bit RAM can otherwise be used to save the system configuration during power shut-down. Tables 1.1 1 through 1.1 5 show the ICM 7170 register map.

Physical Address	Function	Data Value
200H	counter 1/100s	0 to 99
202H	counter hours	0 to 23
	12 hour mode	0 to 12
204H	counters minutes	0 to 59
206H	counter seconds	0 to 59
208H	counter month	1 to 12
20AH	counter date	1 to 31
20CH	counter year	0 to 99
20EH	counter day of week	0 to 6
210H	RAM 1/100s	0 to 99
212H	RAM hours	0 to 23
	12 hour mode	1 to 12
214H	RAM minutes	0 to 59
216H	RAM seconds	0 to 59
218H	RAM month	1 to 12
21AH	RAM date	1 to 31
21CH	RAM year	0 to 99
21EH	RAM day of week	0 to 6
220H	Interrupt status and mask register	
222H	Command register	

Table l.11 Address codes and functions

D7	D6	D5	D4	D3	D2	D1	D0
N.U.	Day	Hour	Min	Sec	1/10s	1/100s	Alarm

Table l.12 lnterrupt Mask Register (write only)

D7	D6	D5	D4	D3	D2	D1	D0
Global int	Day	Hour	Min	Sec	1/10s	1/100s	Alarm

Tablel.13 lnterrupt Status Register(read only)

D7	D6	D5	D4	D3	D2	D1	D0
N.U.	N.U.	Test	Int	Run	12/24	Freq	Freq

Table l.14 Command Register Format

BIT	FUNCTION	VALUE
D0	Crystal Frequency	0
D1	32.768Khz	0
D2	12 hour mode	0
	24 hour mode	1
D3	Stop	0
	Run	1
D4	Int. disable	0
	Int. enable	1
D5	Normal mode	0
	Test mode	1

Tablel.15 Command Register Bit Assignment

1.8 80187 NUMERIC PROCESSOR EXTENSION

The 8OC187 numeric processor extension is optional and supported by the GESBS-8 hardware. Updating the system is accomplished by installing the 8OC187 in its socket and removing a jumper. When the 8OC186 executes an ESC instruction, the CPU automatically generates one or more I/0 operations to the 8OC187's reserved I/0 addresses (F8H, FAH, FCH). These I/0 operations take place independently of the 8OC186's current I/0 privilege level. Reserved I/0 addresses are generated automatically by the processor. These I/0 addresses should not be referenced explicitly, due to the risk of corrupting data within the SOC187.

1.9 SERIALCOMMUNICATIONSCONTROLLER

1.9.1 GENERAL DESCRIPTION

The 8530 SCC Serial Communications Controller is designed for multi-f unction support in order to handling the large variety of serial communication protocols available. The 8530 can be programmed to satisfy special serial communications requirements as well as to follow standard formats such as byte-oriented synchronous, bit-oriented synchronous and asynchronous. The features of the 8530 SCC are listed in Table 1. 1 6.

Two independent full-duplex channels
Receiver data registers qua-duplex buffered Transmitter data registers double buffered Baud Rate generator in each channel Digital Phase-Locked Loop for clock recovery NRZ, NRZI and FM encoding/decoding
Asynchronous capabilities 5, 6, 7 or 8 bits per character 1, 1-1 /2 or 2 stop bit Odd or Even Parity Times 1, 16, 32 or 64 clock modes Break generation and detection Parity, Overrun and framing error detection
Byte-oriented synchronous capabilities Internal character synchronization 1 or 2 sync. characters in separate registers Automatic synchronous character insertion and deletion Cyclic redundancy check (CRC) generation/detection 6 or 8-bit synchronous character
SDLC/H DLC capabilities Abort sequence generation and checking Automatic zero insertion and deletion Automatic flag insertion between messages Address field recognition 1-field residue handling CRC generation/deletion SDLC loop mode with EOP recognition/loop Entry and exit

Tablel.16 8530 SCC features

1.9.2 8530 REGISTERS

The 8530 SCC contains 13 registers per channel allowing configuration of that channel's functional characteristic. Six registers are directly accessible by the CPU allowing access of the other 8530 registers as shown in Table 1. 1 7.

Physical	Access	Register name address
0100H	R	Channel B Control Register
0100H	W	Channel B Status Register
0102H	R/W	Channel B Data Register
0104H	W	Channel A Control Register
0104H	R	Channel A Status Register
0106H	R/W	Channel A Data Register

Tablel.17 8530 SCC direct access register map

Notes:
- Control Register is the WRO 8530 register
- Status Register is the RRO 8530 register
- Data Register, in write access, is the WR8 8530 register
- Data Register, in read access, is the RR8 8530 register - Baud rate generator has a 4.9152 Mhz input frequency

For more information about programming the 8530 SCC, refer to the *Ziloq Data Book.*

1.9.3 8530 INTERRUPT

The 8530 SCC can generate a vectored interrupt when one of the following conditions occurs:

- Channel A transmitter empty
- Channel A receiver full
- Channel A external/status condition
- Channel B transmitter empty
- Channel B receiver full
- Channel B external/status condition

Channel A interrupts have a higher priority than Channel B interrupts, with the receiver, transmitter and external/status interrupts prioritized in that order, within each channel. The 8530 SCC can generate multiple vectors during INTA cycles, and the Master 82C59 Interrupt level can be programmed in a slave mode.

1.10 PARALLEL I/O CONTROLLER

The 82C55 is a programmable peripheral interface (PPI) device. It is a general purpose I/0 component used to inter- face peripheral equipment to the microcomputer system. The 82C55 device contains three 8-bit ports (A, B and C). All can be configured by the system software with a variety of functional characteristics.

Port A — One 8-bit data latch/buffer and one 8-bit data input latch.

Port B — One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C — One 8-bitdataoutputiatch/bufferand one 8-bitdata input buffer (no latch for input). This port can be divided into two 4-bit ports under mode control. Each 4-bit port contains a 4-bit latch and can be used for control signal outputs and status signal inputs, in conjunction with ports A and S.

For more information about programming, refer to the *Intel Data Book.* Table 1.1 8 82C55 device address register.

Base Address	Access	Operation or Register
80H	Read/Write	Read/Write PORT A
82H	Read/Write	Read/Write PORT B
84H	Read/Write	Read/Write PORT C
86H	Write	Write Control Register

Table 1.18 82C55 register map

1.11 RESET OPERATION

The RESET signal is an output to the G-96 bus generated by the GESSBS-8 module during power-on or when an external reset button is pressed. The reset circuitry includes the MAX 691 device which automatically generates a reset during a power-on or power-off (V typ 4.75 V). It is very important to have an appropriate +5 Volts power supply.

2. PREPARATION FOR USE, INTERCONNECTIONS

2.1 CONNECTOR AND JUMPER IDENTIFICATION

Table 2.1 identifies the jumpers and connectors of the GESSBS-8 module. Figure 2.1 shows their locations on the printed circuit.

Designation	Function
Pi	G-96 Bus interface connector
P2	External I/0 connector (Serials and Parallel I/0)
P3	Timer I/0 interface connector
P4	External reset connector
J1	Modem/Terminal selector channel A
J2	Clock selector for serial port A
J3	Modem/Terminal selector channel B
J4	Clock selector for serial port B
J5	External I/0 interrupt selection
J6	Timer: CLKI input clock selection
J7	U23 socket EPROM/RAM selection
J8, J9	Timer: CLK2 input clock selection
J10	Master IRQO Interrupt selection
J11	Timer: CLKO input clock selection
J12	U25 socket EPROM/RAM selection
J13	Numeric Processor Extension
J14 / Jl5	U23/U25 EPROM/RAM size selection
J16 / Jl7	U24/U26 EPROM size selection
Jl8, J21	8OC186 NMI source selection
J20,J22-J25	U23/U25 base address selection
J19,J26	U23/U25 wait states selection
J27	E, SYSCLK Tri-State selection

Table 2.1 Connectors and jumpers identification

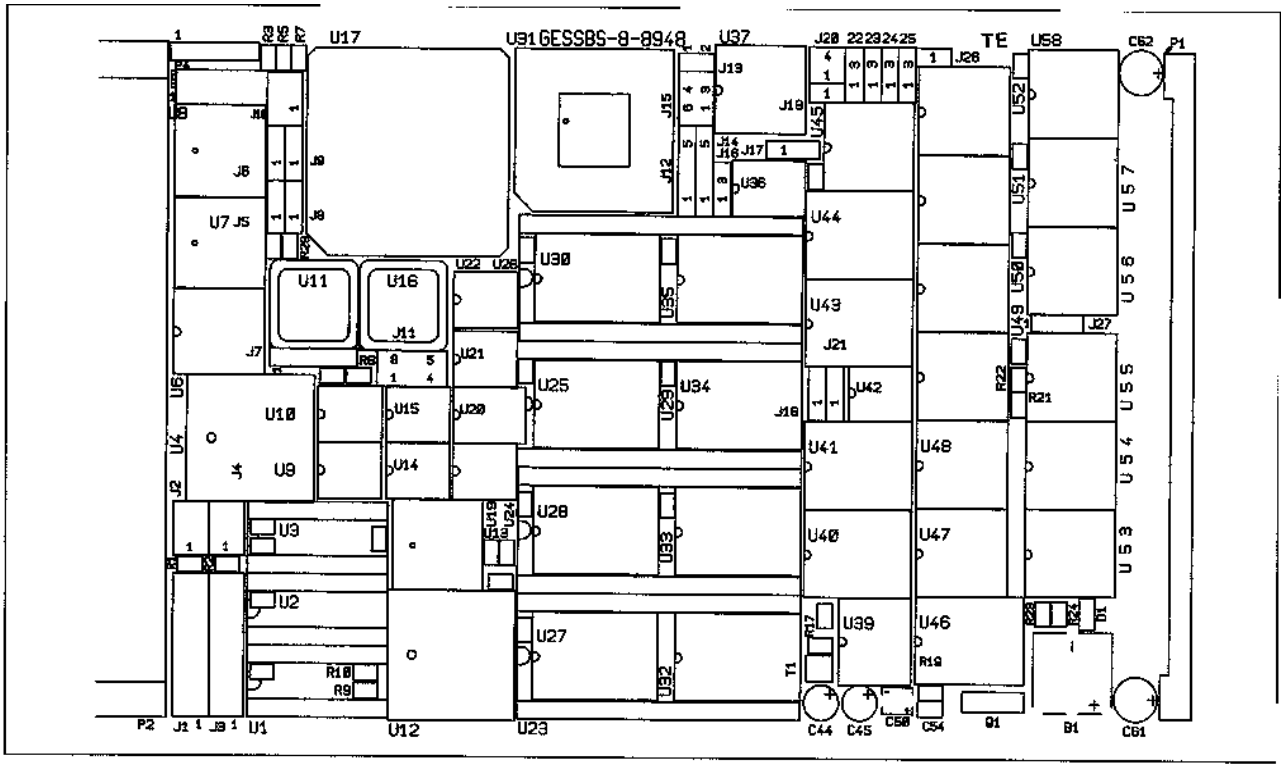


Figure 2.1a Implementation

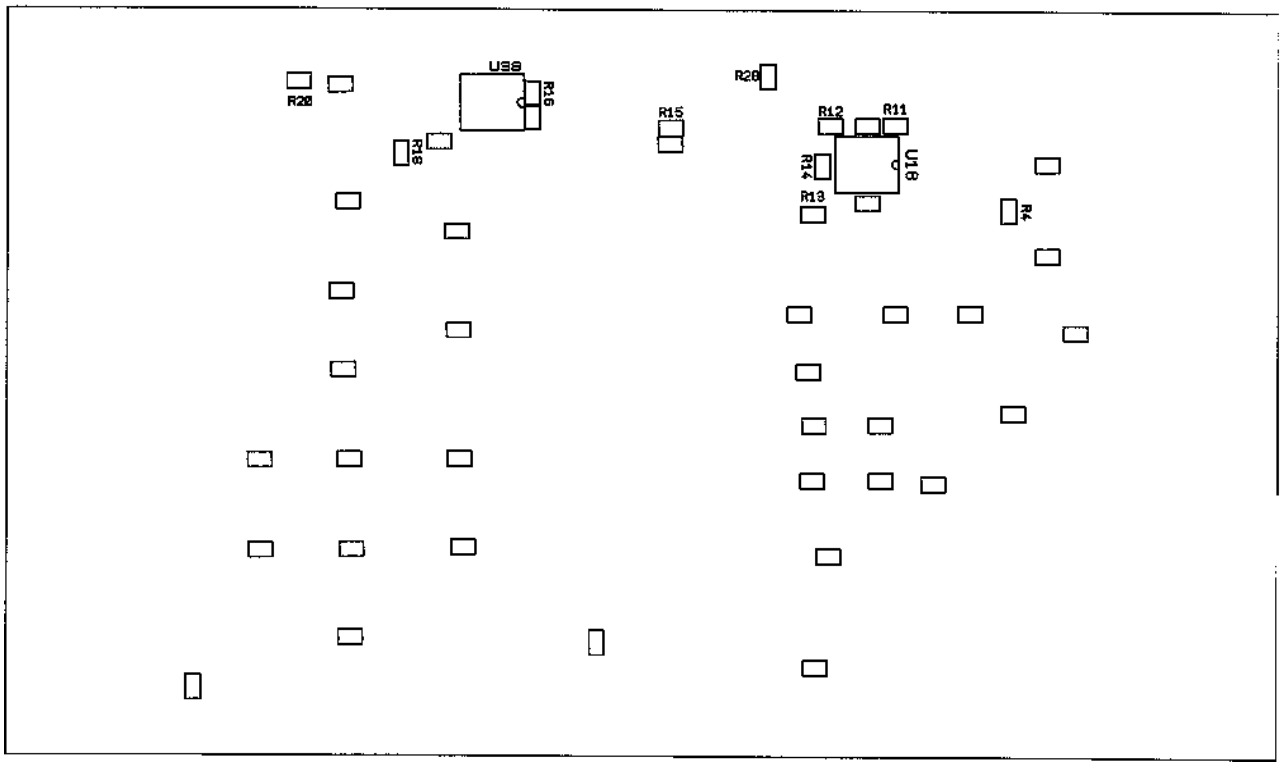


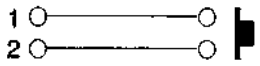
Figure2.lb Implementation solder side

2.2 RESTART OPERATION

An external switch for system resetting can be connected to the P4 connector as illustrated in Figure 2.2.

1	RESET
2	0 V
3	not used
4	not used
5	+5 V

P4 pin assignment



P4 external connection

Figure **2.2** External Reset connector

2.3 SERIAL COMMUNICATION INTERFACE

2.3.1 GENERAL INFORMATION

The GESSBS-8 provides two serial interfaces driven by the 85C30 SCC device. These two serial interfaces allow asynchronous and synchronous communications, and provide signals for modem connections. Interconnections on J1 and J3 provide the configuration of channels A and B as DCE (Data Communication Equipment) or DTE (Data Terminal Equipment) mode.

External I/0 is available through the P2 connector. A 60-wire flat cable is needed to provide the two serial channel and the parallel I/0 interfaces. This flat cable can be connected to a general purpose dispatcher or proprietary design (e.g., opto-coupled I/0, etc.). The GESSBS-8 module uses the GESPAC standard 10-pin RS-232-C pinout for each channel. Standard signals for the RS-232-C serial interface and the serial channel pin assignments of P2 are shown in Table 2.2.

P2 60-pin Channel A	P2 60-pin Channel B	Signal Name	25-pin delta RS 232-C pin	RS 232-C Signal
1	11	GND	7	not used
3	13	TxD	2	TxD
5	15	RxD	3	RxD
7	17	RTS	4	RTS
9	19	CTS	5	CTS
2	12	DSR	6	DSR
4	14	TxC	15	TxC
6	16	DTR	20	DTR
8	18	DCD	8	DCD
10	20	RxC	17	RxC

Table 2.2 Serial channels P2 connector pin assignment

2.3.2 DCE/DTECONFIGURATION

Signals defined in Table 2.2 are connected to P2 through the J1 and J3 jumpers as illustrated in Figure 2.3. Figures 2.4 and 2.5 show the configuration of J1/J3 for two standard applications. For special configurations, refer to Table 2.2 for signal definitions and Figure 2.3 for their interconnection.

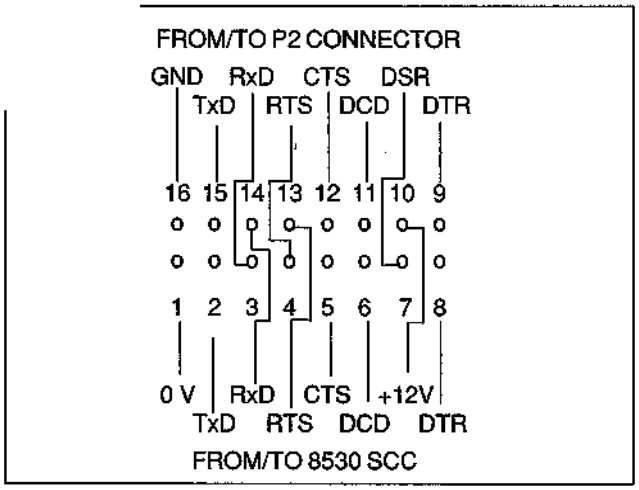


Figure 2.3 J1/J3 pin assignment

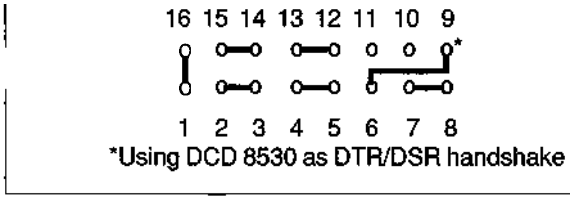


Figure 2.4 DCE configuration (J1 example)

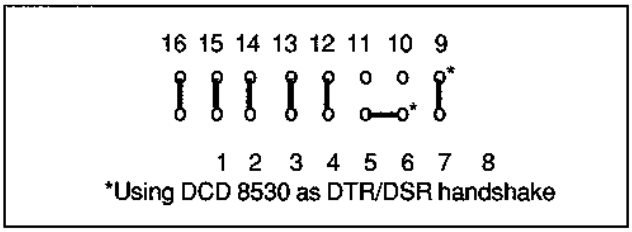


Figure 2.5 DTE configuration (J1 example)

2.3.3 Tx AND Rx CLOCK SELECTION

The transmit and receive clock for channels A and B can be selected to be internal or external for synchronous transfer. When internal, the clocks are provided by the on-chip baud rate generator. Clock selection for channels A and B is done with jumper J2/J4 as shown in Figure 2.6.

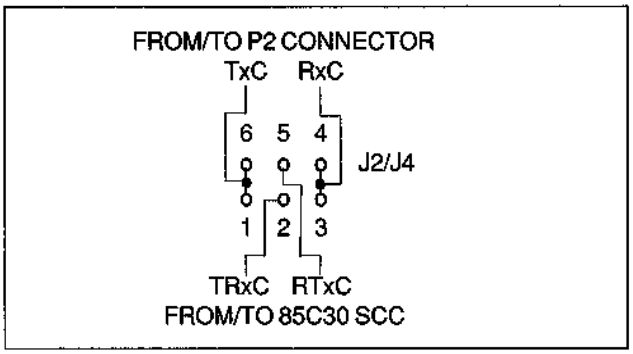


Figure 2.6 J2/J4 pin assignment: Tx C and Rx C clock selection for channel A and B

2.4 82C54-TIMER CLOCK SELECTION

Input clocks of counters O, land 2 can be selected by jumper J11 to provide a basic clock of 1, 2, 4 or 8 Mhz. Other combinations between J11, CLK, OUT, GATE and the external P3 connector are selectable with jumpers J6, J8 and J9. Figure 2.7 shows the basic clock provided by jumper J11 and Figures 2.8 and 2.9 show the different connection possibilities between CLK, OUT, GATE. Figure 2.10 shows the pin configuration of connector P3.

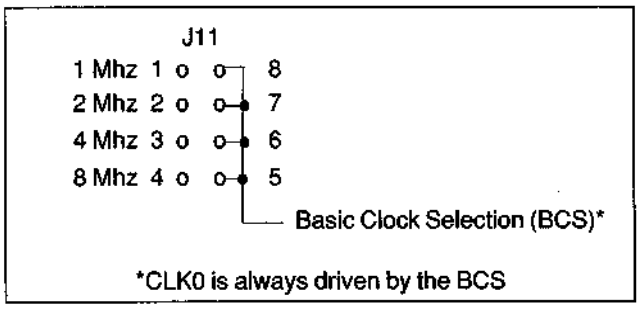


Figure 2.7 Basic clock selection

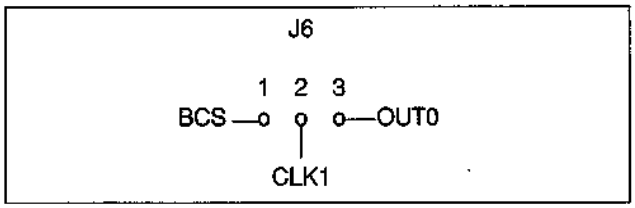


Figure 2.8 CLK1 clock input selection

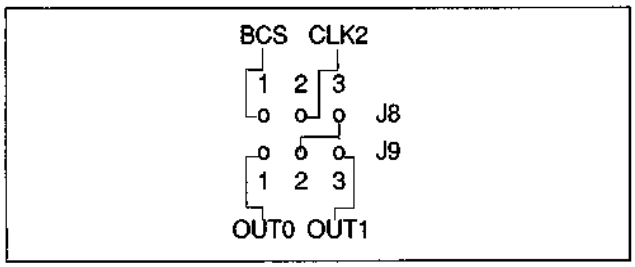


Figure 2.9 CLK2 clock input selection

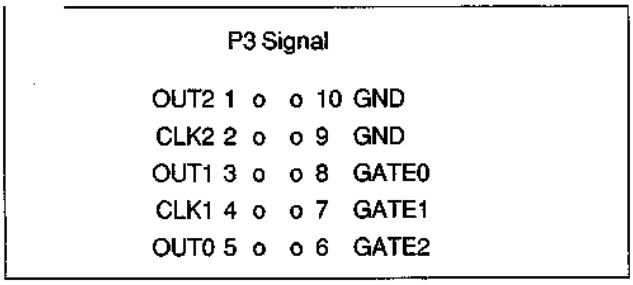


Figure 2.10 P3 pin assignment

2.5 TOP EPROM TYPE SELECTION

U24 and U26 sockets can be equipped with either 28 or 32-pin JEDEC compatible devices. These sockets can support EPROM devices from 8 Kbytes up to 128 Kbytes (2764, 27128, 27256, 27512, 271001). A28-pin device must be inserted at the bottom of the 32-pin socket provided on the GESSBS-8 module. The U24 socket is connected to upper data (D8-D15) and socket U26 to lower data (DO-D7). Device type selection is made with J16 and J17 jumpers as illustrated in Table 2.3.

EPROM TYPE	J16	J17
2764	o o—o 1 2 3	o 1 o 2 o 3
27128	o o—o 1 2 3	o 1 o 2 o 3
27256	o—o o 1 2 3	o 1 o 2 o 3
27512	o—o o 1 2 3	o 1 o 2 o 3
271001	o—o o 1 2 3	o 1 o 2 o 3

Table 2.3 EPROM size selection

2.5.1 TOP EPROM ACCESS TIME

Since EPROMs are decoded with the UCS chip selection, the EPROM size and number of wait-states needed to access these EPROMs are software programmable, via the 80CI 86 UMCS Register. Table 2.4 gives the corresponding EPROM access time and number of wait-states to program in the UMCS Register. Note that external ready is ignored during UMCS activity must always be specified. Refer to the *8OC186 Data Sheet* or the *Intel AP-186* for more information on programming.

Number of Wait-states	Minimum** Access Time	Ready Bits* R2 R1 R0	EPROM type
0	115 ns	1 0 0	100 ns
1	177 ns	1 0 1	150 ns
2	240 ns	1 1 0	200 ns
3	302 ns	1 1 1	300 ns

All other combinations are not allowed
**Time from address= 2xCLK + 0.5xCLK - TDVCL - TCHLL - PD374 + (NXCLK)
where:
CLK = Clock period of processor
TDVCL = 186 data valid setup time
TCHLL = ALE inactive delay
PD374 = 74 ACT374 propagation delay CP to On
N = Number of wait-states inserted

Table 2.4 Top EPROM ready bits

2.6 LOW RAM ACCESS TIME

The GESSBS-8 module is factory equipped with 256 Kbytes of SRAM, with an access time of 100 ns maximum for the TTL version and 150 ns maximum for the CMOS version. The 8OC1 86 provides a chip selection for low memory called LCS. The lower memory limit defined by this chip selection is always OH, while the upper limit is programmable. The size of this memory block is defined by programming the RAM upper limit in the LMCS Register. The corresponding upper limit of 256 Kbytes is 3F FFFH. The LMCS Register bits 0 - 2 are used to specify the READY mode for the RAM area. Refer to the *Intel 8OC186DataSheetorthe IntelAP-186for* more information on programming. Refer to Table 2.5 when programming the LMCS Ready bits with 0 wait-state for the TTL version and 1 wait-state for the CMOS version.

Number of Wait state	Minimum** Access Time	Ready Bits* R2 R1 R0	EPROM type
0	115 ns	1 0 0	100 ns
1	177 ns	1 0 1	150 ns

* All other combinations are forbidden
**Time from address= 2xCLK + 0.5xCLK - TDVCL - TCHLL - PD374 + (NXCLK)
where:
CLK = Clock period of processor
TDVCL = 186 data valid setup time
TCHLL = ALE inactive delay
PD374 = 74 ACT374 propagation delay CP to On
N = Number of wait-states inserted

Table 2.5 Low SRAM ready bits

2.7 MID-RANGE MEMORY

U23 and U25 sockets can be equipped with 28- or 32-pin JEDEC compatible devices. These sockets support EPROM or SRAM devices from 8 Kbytes up to 128 Kbytes. A 28-pin device must be inserted at the bottom of the 32-pin socket provided on the GESSBS-8 module. The U23 socket is connected to upper data (D8-Dl 5) and socket U25 to lower data (DO-D7).

2.7.1 MID-RANGE MEMORY BASE ADDRESS AND SIZE SELECTION

The Mid-Range Block address is always located inside one of the three available 256 Kbyte banks, selectable with jumper J20 as shown in Table 2.6. The Mid-Range Memory base address and block size are selectable with jumpers J22, J23, J24 and J25 as shown in Table 2.7.

J20	Selected Block	J20	Selected Block
1 o—o 4 2 o o 3	40 000H to 7F FFFH	1 o o 4 2 o o 3	C0 000H to FF FFFH
1 o o 4 2 o—o 3	80 000H to BF FFFH	1 o—o 4 2 o—o 3	SRAM area Forbidden

Table 2.6 Mid-range memory block area selection

Mid-Range memory can be placed in the free area between the 256K of low SRAM rnernory and the top EPROM memory. The base address for Mid-Range memory must be a multiple of its block size.

J22 A17 selection		
1 2 3 o—o o A17=0	1 2 3 o o o A17=1	1 2 3 o o—o A17 Not used
J23 A16 selection		
1 2 3 o—o o A16=0	1 2 3 o o o A16=1	1 2 3 o o—o A16 Not used
J24 A15 selection		
1 2 3 o—o o A15=0	1 2 3 o o o A15=1	1 2 3 o o—o A15 Not used
J25 A14 selection		
1 2 3 o—o o A14=0	1 2 3 o o o A14=1	1 2 3 o o—o A14 Not used

Note: Not used means this address is not used in the decoded area (i.e., 27001 EPROMs do not need bits Al 4, Al 5, Al 6 and Al 7 in the decode logic).

Table 2.7 Mid-range memory base address selection

J7	J12	J14	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o o o o—o	1 2 3 4 5 o—o o o o	6 5 4 o—o o o o o 1 2 3	2 x 2764 EPROM 16 Kbytes
J7	J12	J14	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o o o o—o	1 2 3 4 5 o—o o o o	6 5 4 o o—o o o o 1 2 3	2 x 27128 EPROM 32 Kbytes
J7	J12	J14	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o—o o o o	1 2 3 4 5 o—o o o o	6 5 4 o o—o o o o 1 2 3	2 x 27256 EPROM 64 Kbytes
J7	J12	J14	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o—o o o o	1 2 3 4 5 o o o o—o	6 5 4 o o—o o o o 1 2 3	2 x 27512 EPROM 128 Kbytes
J7	J12	J14	J15	Device Type
1 o 2 o o o o	1 2 3 4 5 o—o o o o	1 2 3 4 5 o o—o o o	6 5 4 o o o o—o o 1 2 3	2 x 271001 EPROM 256 Kbytes

Table 2.8 Mid-range memory equipped with EPROM

2.7.2 MID-RANGE MEMORY TYPE SELECTION

Mid-range memory can be equipped with EPROM or with static RAM. The size and type of memory used is selectable with jumpers J7, J12, J14 and J15 as shown in Table 2.8 for EPROMS, and Table 2.9 for SRAM.

J7	J12	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o o o—o o J14 o—o o o o 1 2 3 4 5	6 5 4 o—o o o o o 1 2 3	2 x 8 K x 8 SRAM 16 Kbytes
J7	J12	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o o o—o o J14 o o o o—o 1 2 3 4 5	6 5 4 o o—o o o o 1 2 3	2 x 32 K x 8 SRAM 64 Kbytes
J7	J12	J15	Device Type
1 o 2 o 3 o 4 o 5 o	1 2 3 4 5 o o o—o o J14 o o o o—o 1 2 3 4 5	6 5 4 o o—o o o—o 1 2 3	2 x 128 K x 8 SRAM 256 Kbytes

Table 2.9 Mid-range memory equipped with SRAM

2.7.3 MID-RANGE MEMORY ACCESS TIME

The Mid-Range memory is hardware decoded and an external wait-state generator provides the READY signal to the CPLJ to terminating the access. From 0 to 3 wait-states for Mid-Range memory can be selected via jumpers J 1 9 and J26 as shown in table 2.1 0.

J19	J26	Wait states	J19	J26	Wait states
1o 2o	1 o 2 o	0 Wait state inserted	1 o 2 o	1 o 2 o	1 Wait state inserted
1o 2o	1 o 2 o	2 wait states inserted	1 o 2 o	1 o 2 o	3 wait states inserted

Table 2.1 0 Mid-range memory wait-states selection

2.8 CONFIGURABLEINTERRUPTS

2.6.1 MASTER 8259 IRD SELECTION

The IRQ input of the master interrupt controller can be driven by one of three timer outputs: OUTO, OUT1 or OUT2. This interrupt can be selected with jumper J1 0 as shown in Table 2.11.

J10	IR0	J10	IR0	J10	IR0
6 5 4 o o o o o o 1 2 3	OUT0	6 5 4 o o o o o o 1 2 3	OUT1	6 5 4 o o o o o o 1 2 3	OUT2

WARNING: If this interrupt line is not used in the application, this interrupt source must be disabled during initialization of the interrupt controller.

Table2.11 Master IRQ interrupt selection

An external interrupt coming from the P2 connector can be routed to the slave interrupt controller on IR1 or IR5. This interrupt can be selected with jumper J5 as shown on Figure 2.11.

J5	J5
o—o o 1 2 3	o o—o 1 2 3
External interrupt routed to IR1	External interrupt routed to IR5

WARNING. If these interrupt lines (slave interrupts IR1 and IR5) are not used in the application, these interrupt sources must be disabled during initialization of the interrupt controller.

External interrupt selection

The CPU NMI signal can be provided by one of the following sources: G-96 bus NMI or the G-96 bus power-failure signal (PWF). Time-out circuitry is activated when the CPU attempts to access anon-existent asynchronous area on the G-96 Bus. One of these signals can be routed on the NMI CPU input through jumper Jl 8 and J21 as shown in Table 2.12.

J18 1 2 3 o o—o J21 1 2 3 o o—o	G-96 NMI line	J18 1 2 3 o—o o J21 1 2 3 o o o	Time-out logic
J18 1 2 3 o o—o J21 1 2 3 o—o o	G-96 PWF line	J18 1 2 3 o o o J21 1 2 3 o o o	not used

Table 2.12 NMI CPU selection

2.9 ENABLE AND SYCLK CONTROL

The Enable and SYCLK bus signals can be selected with jumper J27 to be tri-state (or not) during G-96 DMA operation as shown in Table 2.13. These signals are in a high impedance state if the tri-state mode is selected.

J27	Function
1 o 2 o 3 o	Enable and SYCLK signals are free running on the bus during G-96 DMA operation
1 o 2 o 3 o	Enable and SYCLK signals are in a high impedance state during G-96 DMA operation

Table 2.13 Enable and SYCLK tri-state control

2.10 8OC187CO-PROCESSOR INSTALLATION

Upgrading the GESSBS-8 module is accomplished by installing the 8OC187-16 in its socket, then removing the J 13 jumper as shown in Figure 2.12.

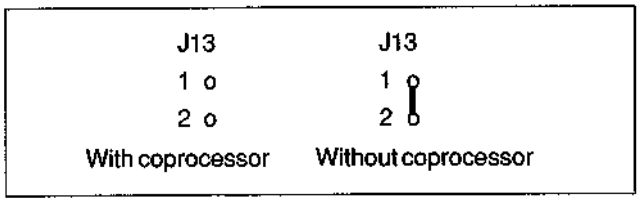


Figure 2.12 GESSBS-8 module coprocessor installation

2.11 PARTICULAR EXTENSION

The GESSBS-8 module provides system signals on the P2 connector. An external interrupt can be generated and routed on the master interrupt controller via the J5 jumper as explained in Section 2.8.2. The buffered signals RD, WR, AI, A2, sysCLK, 8255 chip selection and DROO are available for system design extension and testing options.

2.12 P2 CONNECTOR

The GESSBS-8 module provides a unique interface connector which includes two serial channels , three 8-bit 1/0 ports and buffered system signals. Table 2.14 shows the pin configuration of the P2 connector.

P2 pin	Signal name	P2 pin	Signal name
1	GND	2	DSRA
3	TxDA	4	TxCA
5	RxDA	6	DTRA
7	RTSA	8	DCDA
9	CTSA	10	RxCA
11	GND	12	DSRB
13	TxDB	14	TxCB
15	RxDB	16	DTRB
17	RTSB	18	DCDB
19	CTSB	20	RxCB
21	VCC	22	VCC
23	VCC	24	PA0
25	PA1	26	PA2
27	PA3	28	PA4
29	PA5	30	PA6
31	PA7	32	PB0
33	PB1	34	PB2
35	PB3	36	PB4
37	PB5	38	PB6
39	PB7	40	PC0
41	PC1	42	PC2
43	PC3	44	PC4
45	PC5	46	PC6
47	PC7	48	D4
49	/CS8255	50	RD
51	WR	52	LA1
53	LA2	54	/CLKOUT
55	Reserved	56	Ext. Interrupt
57	/DRQ0	58	GND
59	GND	60	GND

Table 2.14 P2 connector pin assignment

2.13 GESINT-2A MODULE

To make external connections easier, GESPAC proposes a dispatcher module named GESINT-2A.This module provides two 25-pin Delta connectors and a 26-pin general purpose 1!0 connector. Fig. 2.13 illustrates the different part of the GESINT-2A module and the table 2.15 and 2.16 shows the pin-configuration of the connectors.

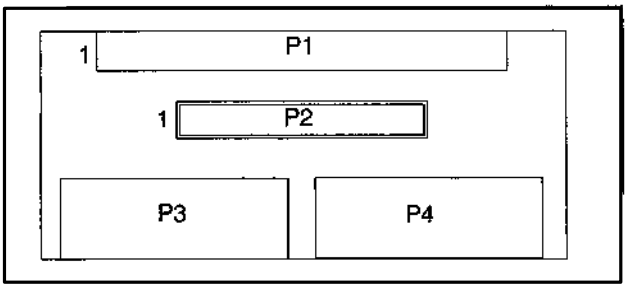


Figure 2.13 GESINT-2A implementation

P3 pin	Signal name	P4 pin	Signal name
2	TxDA	2	TxDB
3	RxDA	3	RxDB
4	RTSA	4	RTSB
5	CTSA	5	CTSB
6	DSRA	6	DSRB
7	GND	7	GND
8	DCDA	8	DCDB
15	TxCA	15	TxCB
17	RxCA	17	RxCB
20	DTRA	20	DTRB

Table 2.15 GESINT-2A P3/P4 connectors pin assignment

P2 pin	Signal name	P2 pin	Signal name
1	PA0	2	PA1
3	PA2	4	PA3
5	PA4	6	PA5
7	PA6	8	PA7
9	PB0	10	PB1
11	PB2	12	PB3
13	PB4	14	PB5
15	PB6	16	PB7
17	PC0	18	PC1
19	PC2	20	PC3
21	PC4	22	PC5
23	PC6	24	PC7
25	VCC	26	GND

Table 2.16 GESINT-2A P2 connector pin assignment

2.14 INTERFACE WITH THE G-96 BUS

The GESSBS-8 module interconnects directly on the G-96 bus. Signals used by the module are identified in Table 2.14. For more information on the bus, refer to the *G-64IG-96 Bus Specifications manual.*

ROW C	ROW B	ROWA		Definition
GND	GND	GND	1	Power
A16	A8	A0	2	
A17	A9	A1	3	
A18	A10	A2	4	Address
A19*	A11	A3	5	Lines
A20*	A12	A4	6	A0 to A23
A21*	A13	A5	7	
A22*	A14	A6	8	
A23*	A15	A7	9	
Reserved	BRQ	BGRT	10	
Reserved	DS1	DS0	11	
Reserved	BBUSY	HALT *	12	
GND	Enable	SYCLK	13	Control and
Reserved	Reset	VPA	14	Interrupt
Reserved	NMI	DTACK	15	Lines
IRQ3	IRQ1	VMA	16	
IRQ5	IRQ2	R/W	17	
VED *	IACK	IRQ4	18	
GND	D12	D8	19	
P5 *	D13	D9	20	
P4 *	D14	D10	21	Data Lines
P3 *	D15	D11	22	D0 to D15
P2 *	D4	D0	23	and
P1 *	D5	D1	24	Arbitration
P0 *	D6	D2	25	Lines
Reserved	D7	D3	26	
SYSFAIL *	BERR *	Page *	27	
A-1**	Chain in	Chain out	28	Misc.
Reserved	+ 5 V bat.*	PWF	29	
Reserved	–12 V	+12 V	30	Power
+ 5 V	+ 5 V	+ 5 V	31	
GND	GND	GND	32	

Note: * Not used in the GESSBS-8 module.
** Special feature of the GESSBS-8 module
(the 8OC1 86's AO CPU line is connected on A-1)

Table 2.17 Pl connector, G-96 bus.

3. DYNAMIC CHARACTERISTICS FOR SYNCHRONOUS AND ASYNCHRONOUS OPERATIONS

All transfers on the G-96 bus correspond to G-96 bus specifications. For more information on timing generated by the GESSBS-8 refer to the *G-64IG-968usSpecificationsmanuaL*

4. GETTING STARTED

4.1 UPPER MEMORY CHIP SELECT

The 80186 provides a chip selection called /UCS, for the top of memory. The upper memory limit defined by this chip selection is always OFFFFFH; the lower limit is programmable through the UMCS register. UMCS bits R2-RO are used to specify READY mode for the memory area defined by this chip selection register. With the GESSBS-8 module, the 80186 must generate a READY signal internally for the UCS and ignoring the external RDY line. The UMCS register R2 bit must be set to 1. Rl and RO define the number of wait-states to be inserted depending on the EPROM access time (Refer to Section 2.5.1 for access time selection). Table 4.1 shows the UMOS register bit assignment.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
19	18	17	16	15	14	13	12	11	10	1	1	1	1	X	X
A19									A10						

Table 4.1 UMCS register

4.2 LOWER MEMORY CHIP SELECT

The 80186 provides a chip selection for low memory called / LCS. The lower memory limit defined by this chip selection is always OH; the upper limit is programmable. The upper limit of this memory block is defined in the LMCS register. LMCS register bits R2-RO are used to specify READY mode for the memory area defined by this register. The GESSBS-8 module is factory equipped with 256 Kbytes of SRAM running without wait-states. Table 4.2 gives the LMCS register value for this memory block.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
A19									A10						

Table 4.2 LMCS register

4.3 MID-RANGE MEMORY CHIP SELECTS

Since GESSBS-8 can be equipped with a coprocessor, the Mid-Range Memory chip selections are not used in this module. The MMCS register must not be programmed.

4.4 PERIPHERAL CHIP SELECTS

The 80186 can generate chip selections for up to seven peripheral devices. PCSO - PCS4 are used in the GESSBS-3 to select internal peripherals. PCS5 and PCS6 must be programmed to provide latched address bits Al and A2. Three wait-states must be inserted for PCSO - PCS3 without external ready, and three wait states plus external ready must be programmed for PCS4 chip selection. The starting address of the peripheral chip-select block is defined by the PACS register, and must be set to 800H to avoid conflict with the VPA area and the internal 80186 peripherals. Tables 4.3 and 4.4 show the MPCS and PACS registers initialization.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0
1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

EX: 5 PCS lines used, Al and A2 provided
MS: Peripherals mapped into 1/0 space
PCS4 = 3 wait states with external ready

Table 4.3 MPCS register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1

A19 A10 Peripheral base address = 800H
PCSO -3 = 3 wait states without external ready

Table 4.4 PACS register

4.5 RELOCATION REGISTER

All the 80186 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. The base address of the control block must be set to 4000H in the relocation register as shown in table 4.5.

15	14	13	12	11 0
ET	Slave/master	X	M/IO	Relocation address bits A19-8
U	Slave = 1	X	U	Base address = 4000H

U: User defined
X: Insignificant

Table 4.5 Relocation register

For more information about programming, refer to the *Intel Data Book.*

4.6 DEVICE LOCATIONS

Table 4.6 shows the 28-pin devices implementation and Table4.7shows the EPROM/RAM locations for Top memory and Mid-range memory.

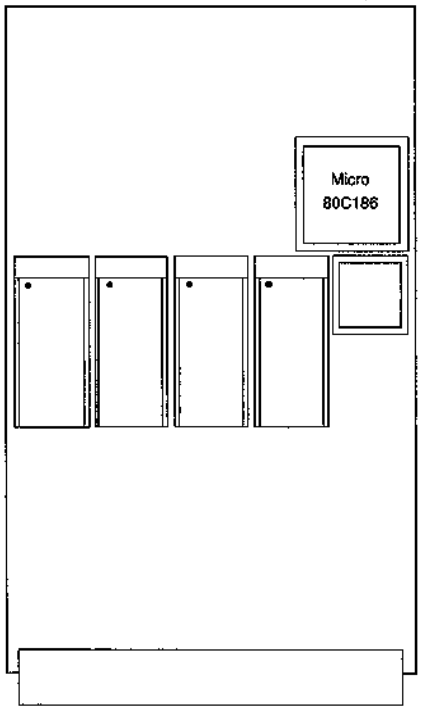


Table 4.6 28-pin device implementation

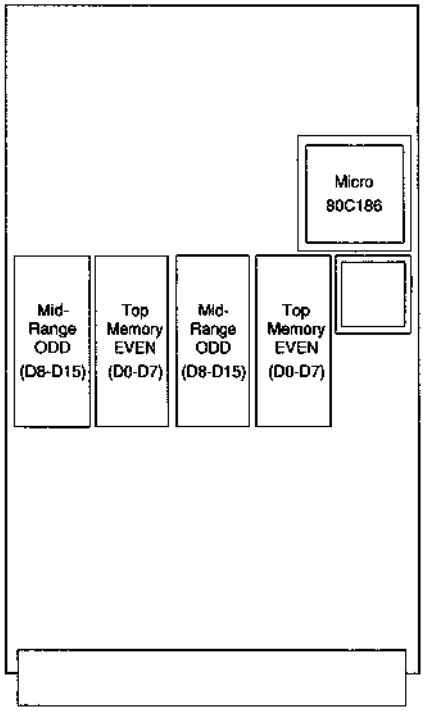
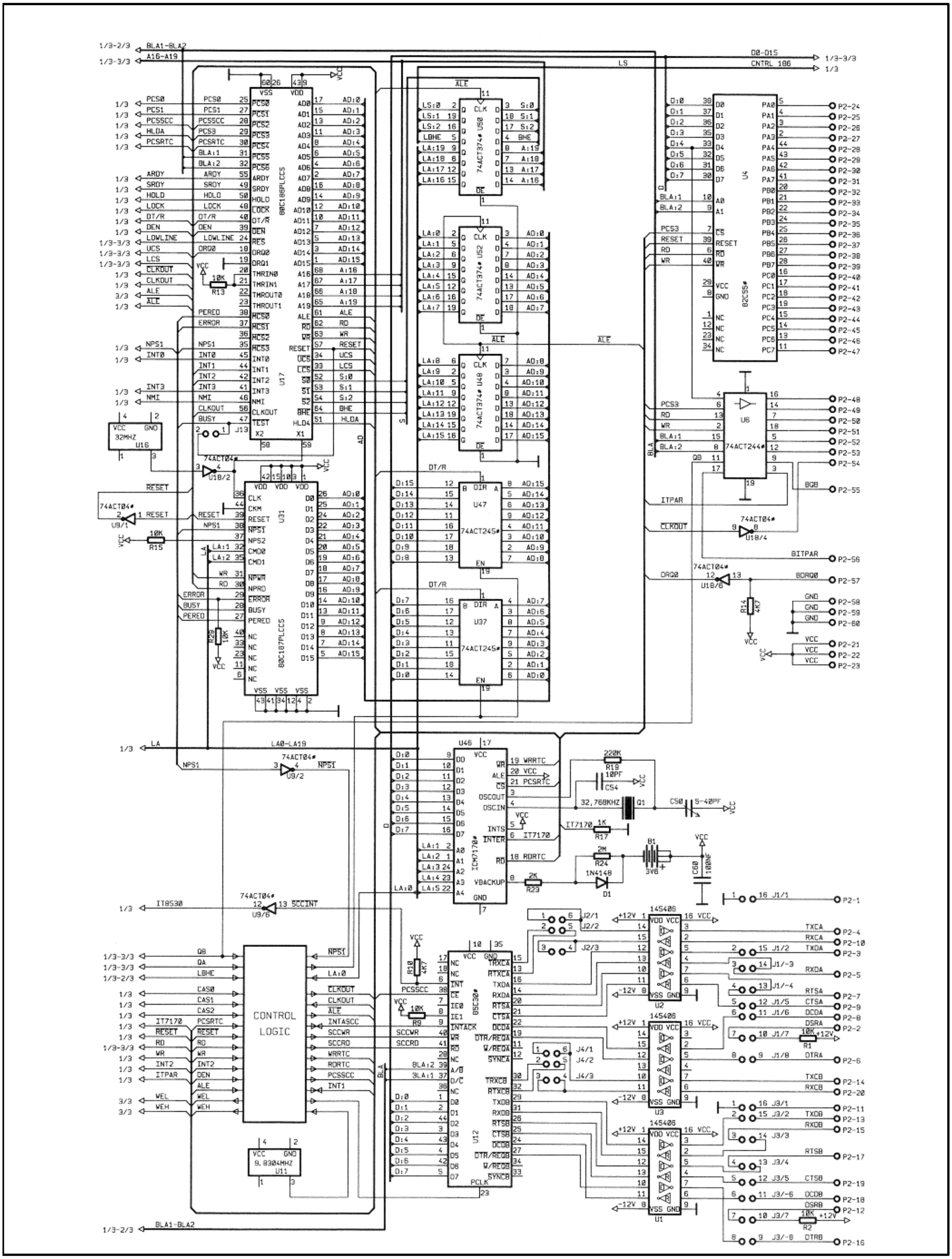
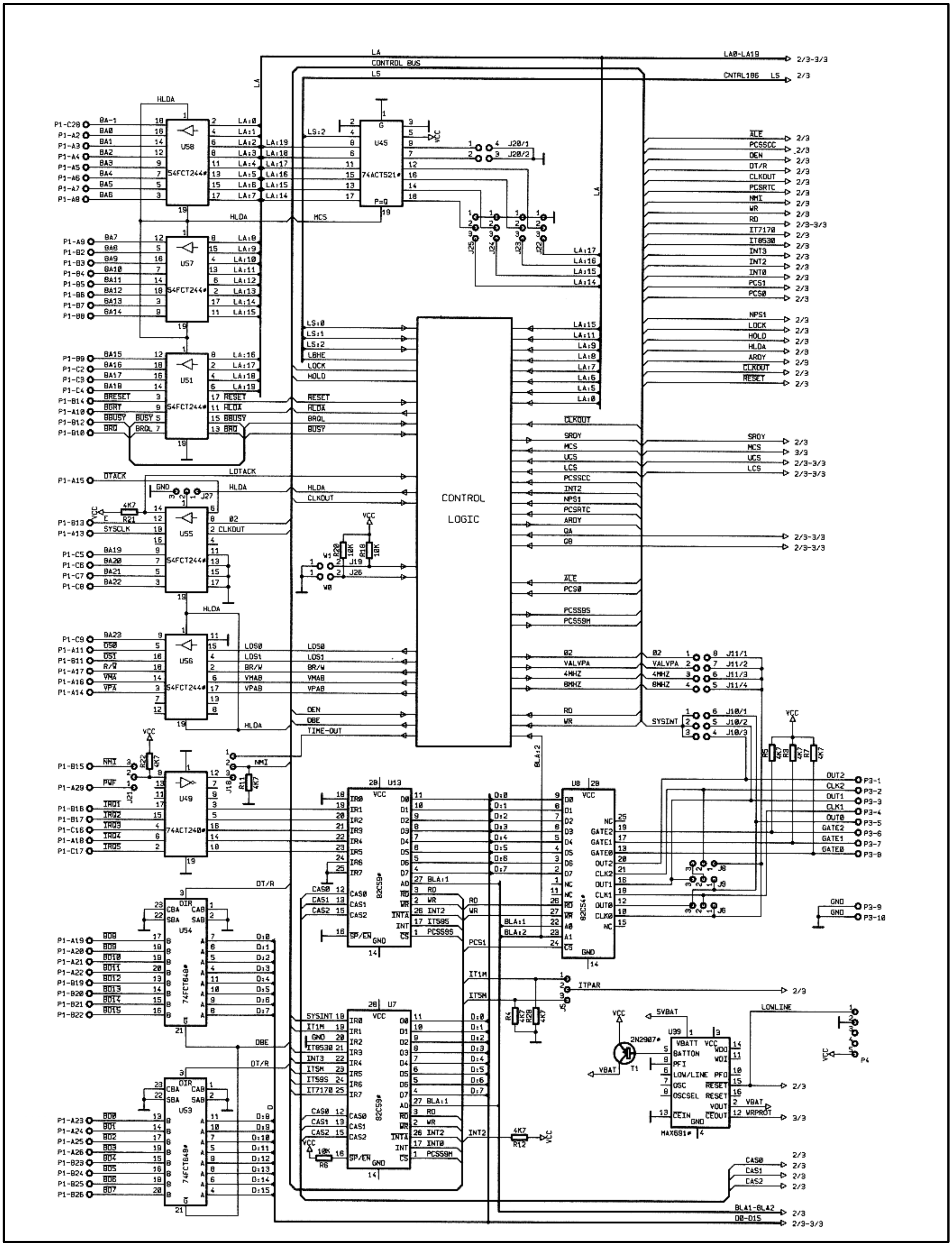
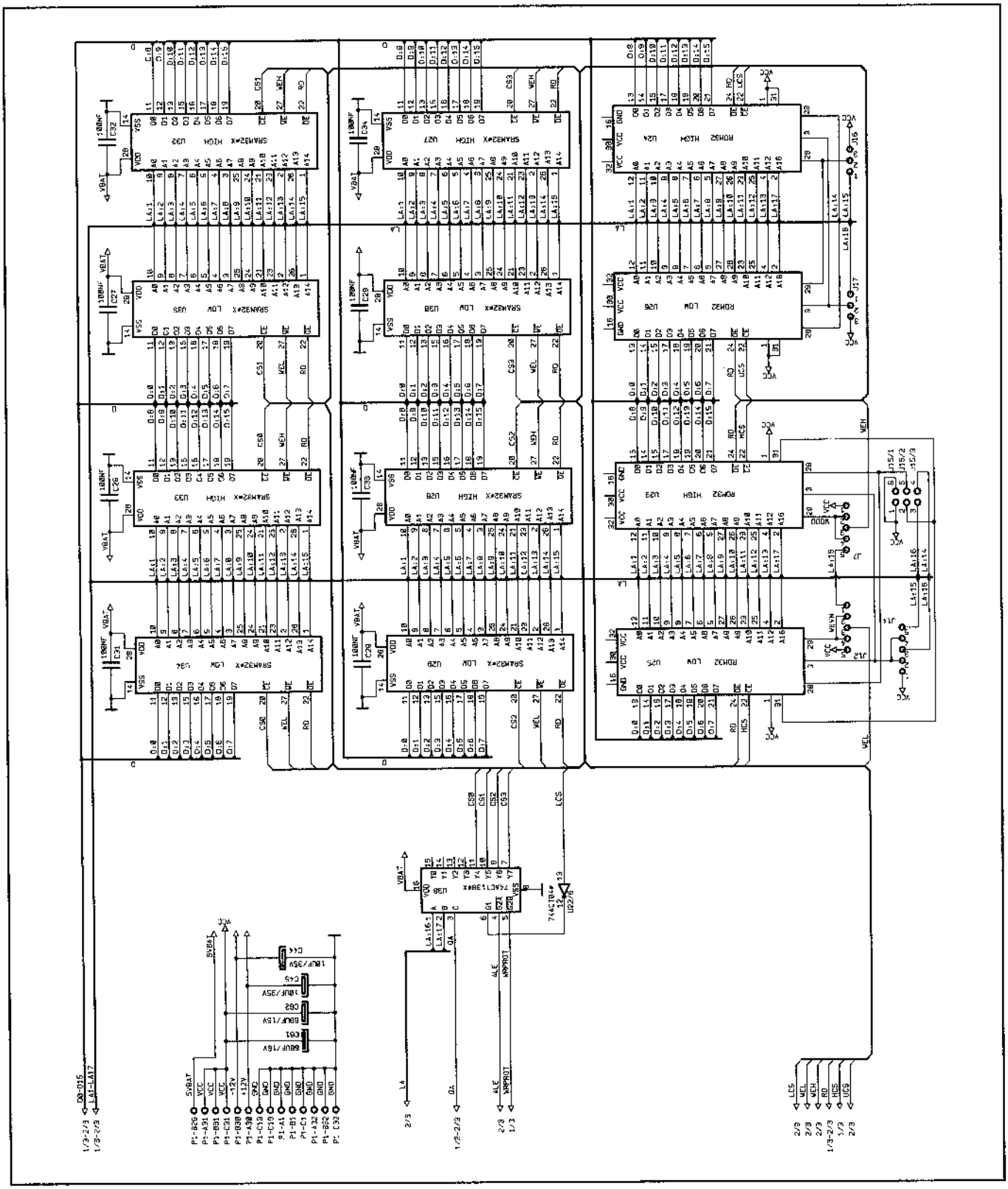


Table 4.7 EPROM / RAM locations


BLA1-BLA2
A16-A19
D0-D15
CNTRL 186
LS
80C186PLCC5
U17
74ACT374#
U50
U52
U48
82C55#
U4
74ACT244#
U6
32MHZ
U16
80C187PLCC5
U31
74ACT245#
U47
U37
LA0-LA19
ICM7170#
U46
32,768KHZ
Q1
CONTROL
LOGIC
9,8304MHZ
U11
85C30#
U12
145406
U2
U3
U1
74ACT04#


LA
CONTROL BUS
LS
LA0-LA19
CNTRL186 LS
HLDA
U58
54FCT244
U57
54FCT244
U51
54FCT244
U45
74ACT521
P=Q
J20/1
J20/2
J25
J24
J23
J22
MCS
ALE
PCSSCC
DEN
DT/R
CLKOUT
PCSRTC
NMI
WR
RD
IT7170
IT8530
INT3
INT2
INT0
PCS1
PCS0
NPS1
LOCK
HOLD
ARDY
RESET
CONTROL
LOGIC
LS:0
LS:1
LS:2
LBHE
BRESET
BGRT
BBUSY
BRQ
BRQL
BUSY
DTACK
LDTACK
SYSCLK
U55
54FCT244
J27
J19
J26
W0
W1
SRDY
UCS
LCS
QA
QB
PCS59S
PCS59M
U56
54FCT244
LDS0
LDS1
BR/W
VMAB
VPAB
DBE
TIME-OUT
VALVPA
4MHZ
8MHZ
J11/1
J11/2
J11/3
J11/4
SYSINT
J10/1
J10/2
J10/3
U49
74ACT240
NMI
PWF
J21
J18
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
U13
82C59
U8
82C54
OUT2
CLK2
OUT1
CLK1
OUT0
GATE2
GATE1
GATE0
CLK0
J8
J9
J6
GND
U54
74FCT640
U53
74FCT640
U7
82C59
BLA:1
BLA:2
IT1M
ITSM
ITPAR
J5
SVBAT
VBAT
2N2907
T1
U39
MAX691
LOWLINE
WRPROT
P4
CAS0
CAS1
CAS2
BLA1-BLA2
D0-D15
2/3
2/3-3/3
3/3



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