VMIVME-2511
48-bit Digital Parallel Input/Output Board

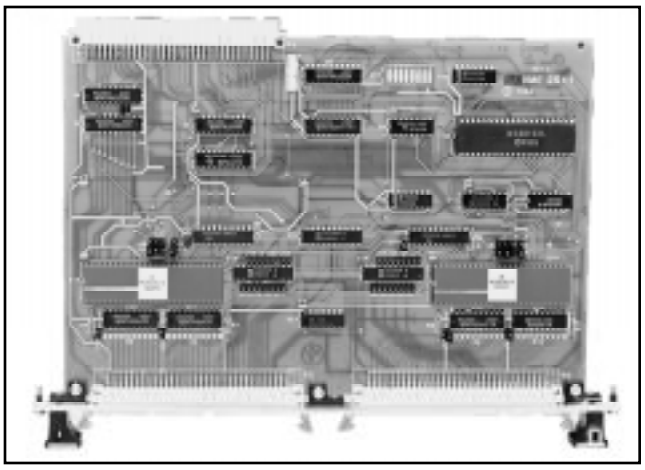
- 48 bit of TTL I/O
- Programmable modes
  - — Unidirectional 8- and 16-bit
  - — Bidirectional 8- and 16-bit
  - — Double-buffered I/O modes
  - — Programmable handshake options (interlocked or pulsed)
  - — Status/interrupt inputs
- Two 24-bit programmable timers
  - — Periodic interrupt generator
- I/O options
  - — 64 mA sink capability
  - — Square wave generator
  - — Interrupt after timeout
  - — Elapsed time measurement
  - — External clock
  - — Device watchdog
- Utilizes two MC68230 parallel interface/timers

GENERAL DESCRIPTION — The VMIVME-2511 is designed utilizing two Motorola MC68230 Parallel Interface/Timers (PI/Ts) and one MC68153 Bus Interrupter Module (BIM) to support all board functions as shown in Figure 1.

The VMIVME-2511 is capable of handling four interrupt requests. Each PI/T module is capable of two requests: a port interrupt request and a timer interrupt request. The four interrupt request signals (two from PI/T No. 1 and two from PI/T No. 2) are connected to the BIM giving full interrupt support for both PI/T modules. Each PI/T module has two on-board Interrupt Vector Registers programmable by the user. Table 1 provides a summary of operational modes for the PI/T.

The MC68230 Parallel Interface/Timer provides a versatile, double-buffered, parallel interface, and an operating system-oriented timer to VMEbus systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8- or 16-bit wide. In the unidirectional mode, an associated Data Direction Register determines whether the port pins are inputs or outputs. In the bidirectional mode, the Data Direction Registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high-speed peripherals or the other computer systems. The PI/T ports allow use of vectored or autovectored interrupts. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement, or as a device watchdog. MC68230 I/O pins available to the user are shown in Figure 3.

PA0 TO PA7 AND PB0 TO PB7 (Port "A" and Port "B") — Ports "A" and "B" are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1 to H4. For stabilization during system power up, Ports "A" and "B" have internal pull-up resistors to V_{CC}. All port pins are active high.



H1 TO H4 — Handshake Pins (I/O depending on the mode and submode). Handshake pins H1 to H4 are multipurpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power up, H2 and H4 have internal pull-up resistors to V_{CC}. Their sense (active high or low) may be programmed in the port general Control Register bits 3 to 0. The instantaneous level of the handshake pins can be read from the port Status Register independent of the mode.

Port C — (PC0 to PC7/Alternate Function). This port can be used as eight general-purpose I/O pins (PC0 to PC7), or any combination of six special function pins and two general-purpose I/O pins (PC0 to PC1). (Each dual function pin can be standard I/O or a special function independent of the other Port "C" pins.) The dual function pins are defined in the following paragraphs. When used as Port "C" pin, these pins are active high. They may be individually programmed as inputs or outputs by the Port "C" Data Direction Register.

Ordering Options

March 11, 1998 800-022511-000 D	A	B	C	–	D	E	F
VMIVME-2511 –		0	0	–			

A = Input/Output Type; Low/High Current
2 = TTL/TTL; Low Current
4 = TTL/TTL; High Current
6 = TTL/OC; Low Current
8 = TTL/OC; High Current
BC = 00 (Options reserved for future use)

Connector Data

Compatible Cable Connector	Panduit No. 120-964-435
Strain Relief	Panduit No. 100-000-032
PC Board Connector	Panduit No. 120-964-033A

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
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The alternate functions (TIN, TOUT, AND TIACK) are timer I/O pins, TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square wave output, initially high. TIACK is an active low/high impedance input used for timer interrupt acknowledge.

Ports "A" and "B" functions have an independent pair of active low interrupt request (PIRQ) and interrupt acknowledge (PIACK) pins.

PORT CONTROL STRUCTURE — The primary focus of most applications will be on Ports "A" and "B," the handshake pins, and the port interrupt pins. They are controlled in the following way: the port general Control Register contains a 2-bit field that specifies a set of four operation modes. These modes govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's Control Register to further define its operation. In each port Control Register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and the behavior of two of the handshake pins. This structure is summarized in Table 2 and Figure 4.

FUNCTIONAL CHARACTERISTICS

Compliance: This product complies with the VMEbus specification Rev. C. 1 with the following mnemonics:

A16: D16, D08 (O) :29, 2D: Slave
Interrupt levels: I(1) - I (7):ROAK
Interrupt vector: D08 (O)
6U form factor

I/O Connector Type: 64-pin connector - DIN 41612

I/O Organization: The VMIVME-2511 board utilizes two Motorola MC68230 Parallel Interface/Timers that provide a wide variety of programmable I/O features, including unidirectional 8- and 16-bit I/O, bidirectional 8- and 16-bit I/O, selectable handshake options, and a 24-bit programmable timer. The VMIVME-2511 may be ordered with a buffered I/O option that provides up to 64 mA sink capability; however, the bidirectional modes are not supported with this option.

Addressing Scheme: One eight-position DIP switch is provided to select the board's base address. The VMIVME-2511 is configured at the factory to respond to short supervisory I/O access; however, the user may change the jumper to enable short nonprivileged access. The VMIVME-2511 registers are accessed at ODD addresses.

ELECTRICAL SPECIFICATIONS

I/O Buffers Low Current Option:
VIH = 2 V minimum
VIL = 0.8 V maximum
IOH = -15 mA
IOL = 24 mA

I/O Buffers (5.25 V ≤ VCC ≥ 4.75 V)
High Current Option:
VIH = 2 V minimum
VIL = 0.8 maximum
IOH = -15 mA
IOL = 64 mA

PHYSICAL/ENVIRONMENTAL

Temperature: 0 to 55 °C, operating
-20 to 85 °C, storage

Humidity: 20 to 80 percent, noncondensing

Cooling: Convection

Power Requirements: +5 V at 2.51 A

MTBF: 82,200 hours (stress)

TRADEMARKS

Table 1. PI/T I/O Channel Definitions

(PB0 to PB7)	All eight bits, input or output depending on jumper configuration chosen
(PC4 to PC7)	All four bits, input or output depending on jumper configuration chosen
H1	Input only
H2	Configured as input or output
H3	Input only
H4	Configured as input or output
PC0	Configured as input or output
PC1	Configured as input or output
PC2/TIN	Input only
PC3/TOUT	Output only

Table 2. Port Mode Control Summary

Mode 0 (Unidirectional 8-bit Mode)

Port A		
Submode	00	Double-buffered input
	H1	Latches input data
	H2	Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed input handshake protocols
Submode	01	Double-buffered output
	H1	Indicates data received by peripheral
	H2	Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed output handshake protocols
Submode	1X	bit I/O*
	H1	Status/interrupt generating input
	H2	Status/interrupt generating input or general-purpose output
Port B, H3, and H4		Identical to Port “A”, H1, and H2

*This mode of operation is not supported by the VMIVME-2511.

Mode 1 (Unidirectional 16-bit Mode)

Port A		Double-buffered data (Most Significant)
Submode	XX	(not used)
	H1	Status/interrupt generating input
	H2	Status/interrupt generating input or general-purpose output
Port B		Double-buffered data (Least Significant)
Submode	X0	Unidirectional 16-bit input
	H3	Latches input data
	H4	Status/interrupt generating input, general-purpose output or operation with H43 in the interlocked or pulsed input handshake protocols
Submode	X1	Unidirectional 16-bit output
	H3	Indicates data received by peripheral
	H4	Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed output handshake protocol

Mode 2 (Bidirectional 8-bit Mode)

Port A	bit I/O	(with no handshaking pins)
Submode	XX	(not used)

Port B	Bidirectional 8-bit data (double buffered)	
Submode	XX	(not used)
	H1	Indicates output data received by peripheral
	H2	Operation with H1 in the interlocked or pulsed output handshake protocols
	H3	Latches input data
	H4	Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-bit Mode)

Port A	Double-buffered data (Most Significant)	
Submode	XX	(not used)

Port B	Double-buffered data (Least Significant)	
Submode	XX	(not used)
	H1	Indicates output data received by peripheral
	H2	Operation with H1 in the interlocked or pulsed output handshake protocols
	H3	Latches input data
	H4	Operation with H3 in the interlocked or pulsed input handshake protocols

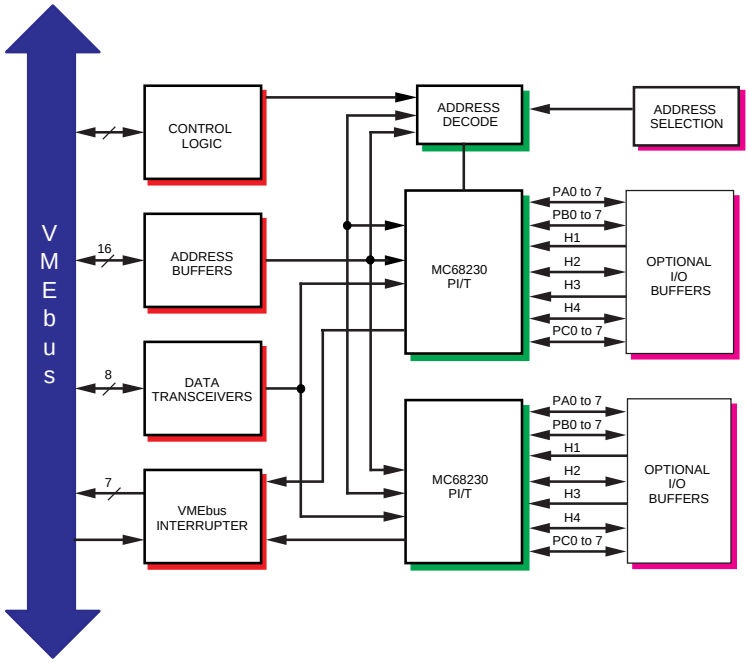


Figure 1. Functional Block Diagram

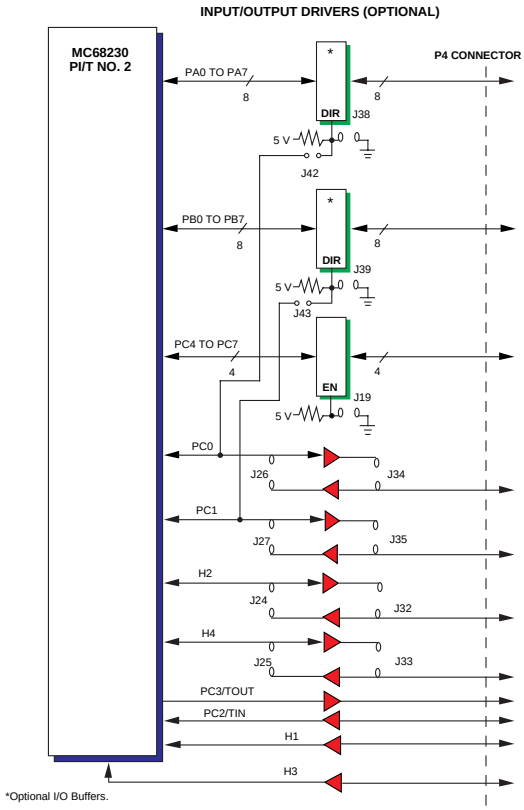
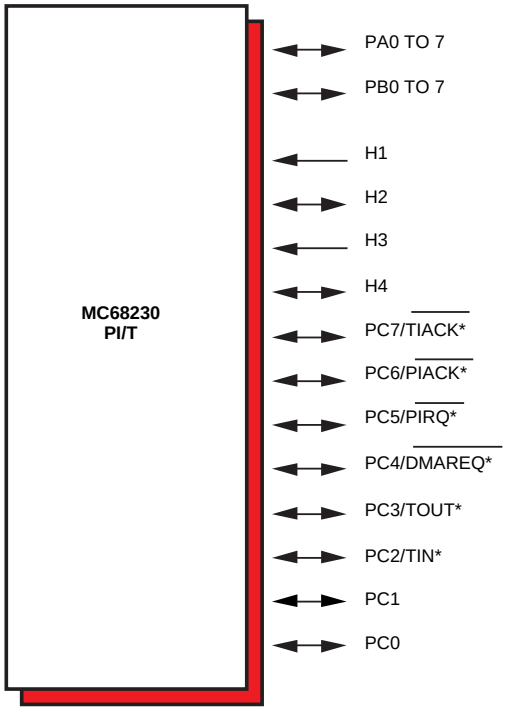


Figure 2. I/O and Jumper Block Diagram for PI/T No. 2



* Individually programmable dual function pin.

Figure 3. I/O Pin Assignments

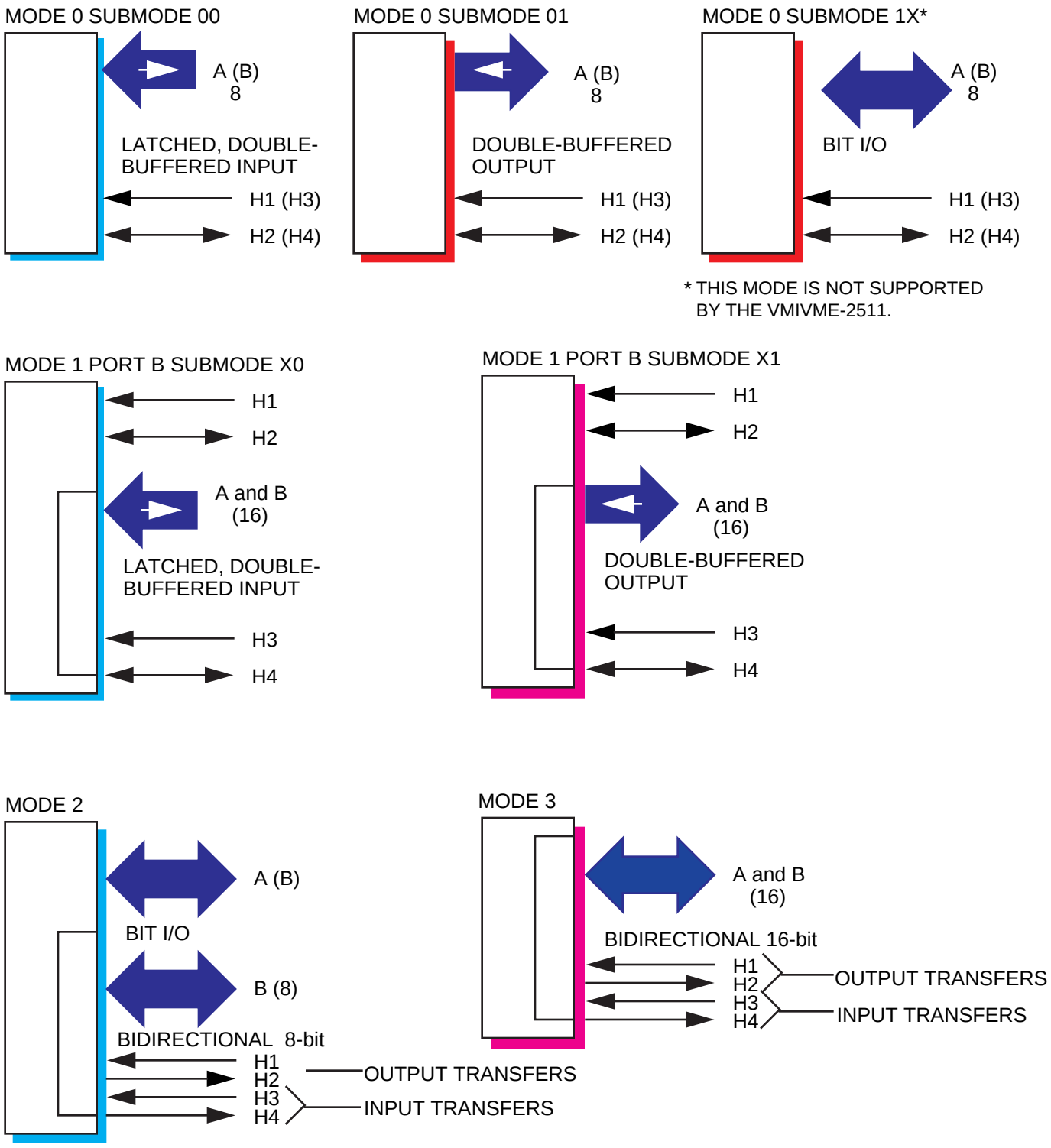


Figure 4. Port Mode Layout