DIGITAL-LOGIC

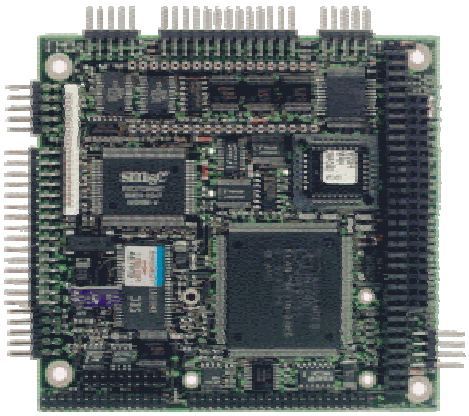
smart embedded computers

TECHNICAL USER'S MANUAL FOR:

MICROSPACE®

PC/104

MSM386SN/SV



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ATTENTION:
All information in this manual and the product are subject to change without prior notice.

REVISION HISTORY:

Prod.-Serialnumber: From: To:	Product Version	BIOS Version	Doc. Version	Date/Vis:	Modification: Remarks, News, Attention:
550xxx10000 550xxx1yyyy	***V2.2***		***V0.9***	***10.96 FK***	***Initial Version***
	V4.0		***V2.0***	***03.97 FK***	***IDE modifications, BIOS***
	V5.1		***V2.4***	***07.97 FK***	***V5.1 Mod.***
			V2.5	08.97 FK	BIOS Download
			V2.6	08.97 FK	RTC Reset IMPORTANT !
			V2.61	08.97 FK	RS485 description
			V2.62	09.97 FK	DOC2000, Virusalert
	V5.1A		***V2.63***	***10.97 FK***	***MSM104J, V5.1A Mod., Jumper***
			V2.64	11.97 FK	V3/V4 DLFFSFMT.EXE
			V2.74	03.98 SL	FFS & Down.exe revision
		V1.40B	V2.75	03.98 JM	Layout, detailed corrections
			V2.76	03.98 JM	POD-Code Table added
			V2.77	03.98 SL	FFS revision
			V2.78	05.98 SL	J35, J36 COM1 485 / TTL add descr.
			V2.79	08.98 JM	Configuration table corrected
			V2.80	11.98 FK	Timer Adr. kor. page 32
	V5.1A	***V1.41***	***V2.81b***	***01.99 JM***	***Maintenance update***
		V1.41	V2.90	02.99 FK	Y2K, BIOS-Hist, Address-MAP's
		V1.42	V2.91	03.99 FK	New Download Tools
			V2.92	03.99 JM	Thermoscan pics added
			V2.93	03.99 JM	Related APP-NOTES
			V2.94	04.99 FK	Filter applications
		V1.43	V2.95	05.99 JM	Default chipset values
			V2.96	10.99 FK	Programming WatchDOG
			V2.97	11.99 FK	Comments in Chap.6, 4.3.2.
			V2.98	01.00 STP	Com 3 to Com 1 example added
	V5.1A	V1.43	V2.99	02.00 STP	LPT- EPP sample added
	V5.1A	V1.43	V3.0	03.2000 STP	Minor corrections
	V5.1b	V1.43	V3.1	10.2000 STP	New address and logo, etc
	V5.1b	V1.44	V3.2	03.2001 STP	Minor corrections

READ CHAPTER 2.7 TO UNDERSTAND THE ELAN300 INCOMPATIBILITIES COMPARED TO THE STANDARD PC-AT DESIGN !

Product Registration:

Please register your product at:

http://www.digitallogic.com -> SUPPORT -> Product Registration

After registration, you will receive driver & software updates, errata information, customer information and news from DIGITAL-LOGIC AG products automatically.

Table of Contents

1 PREFACE

This manual is for integrators and programmers of systems based on the MICROSPACE card family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime. If errors are found, please notify DIGITAL-LOGIC AG at the address shown on the title page of this document, and we will correct them as soon as possible.

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1.2 Technical Support

1. **Contact your local DIGITAL-LOGIC Technical Support in your country first !**

2. Use the Internet Support Request form at http://www.digitallogic.com -> Support -> Support Request Form

3. Send a FAX or an E-mail to DIGITAL-LOGIC AG with a description of your problem.

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   E-Mail: support@digitallogic.com
   Internet www.digitallogic.com

➔ Support requests will only be accepted with detailed information of the product (BIOS-, Board- Version) !

1.3 Limited Warranty

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2 OVERVIEW

2.1 Standard Features

The MICROSPACE PC/104 is a miniaturized modulear device incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

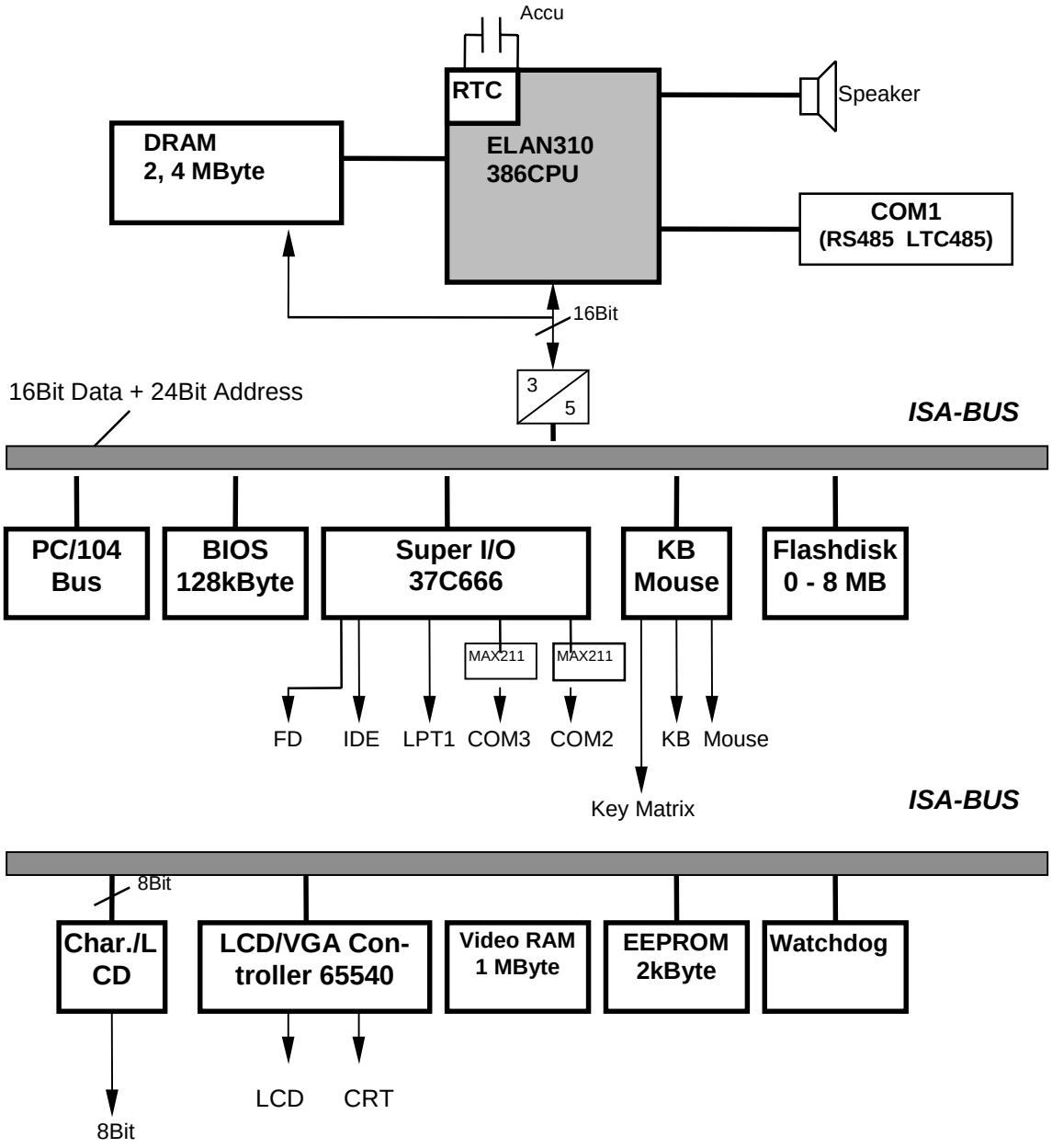
- Powerful ELAN310 CPU with 386 core
- BIOS ROM
- DRAM 2 or 4MBytes 70ns
- Timers
- DMA
- Real-time clock with CMOS-RAM and battery buffer
- LPT1 parallel port
- COM2, COM3 serial port RS232
- COM1 serial port with RS485
- Speaker interface
- AT-keyboard interface or PS/2-keyboard interface
- Keymatrix 8 x 16
- Floppy disk interface
- AT-IDE harddisk interface
- VGA/LCD video interface (only on MSM386SV boards)
- PC/104 embedded BUS
- PS/2 mouse interface

2.2 Unique Features

The MICROSPACE MSM386SV/SN includes all standard PC/AT functions plus unique DIGITAL-LOGIC AG enhancements, such as:

- Flashdisk 512k - 8MByte
- SVGA/LCD interface
- Low power, 1 watt 3.3V CPU
- Single 5 volt supply
- WatchDog with Power-fail
- EEPROM for setup and configuration
- UL approved parts
- Onboard mounting of the MSFLASH-Drive with 4 or 10MByte
- Onboard keymatrix controller

2.3 MSM386SV/SN Block Diagram



2.4 MSM386SV/SN Specifications

CPU:		
CPU 386:	AMD 310™	
Mode:	Real / Protected	
Compatibility:	8086 - 80386	
Word Size:	16 Bits	
Physical Addressing:	24 lines	
Virtual Addressing:	16 MBytes	
Clock Rates:	25, 33MHz selectable	
Socket Standard:	directly soldered onboard	
Math. Coprocessor:		
	not available on AMD-ELAN310	
Power Management:		
available	clock switching, sleep, possible controlled power-up, inactivity-auto powerdown	
DMA:		
8237A comp.	4 channels 8 Bits 3 channels 16 Bits	
Interrupts:		
8259 comp.	8 + 7 levels PC compatible	
Timers:		
8254 comp.	3 programmable counter/timers	
Memory:		
DRAM	2 or 4 MByte directly soldered	
Video only on SV boards:		
Controller:	65545 from C&T	
BUS:	ISA 16Bit	
Enhanced BIOS:	VGA / LCD BIOS	
Memory:	VRAM onboard: 1MByte	
CRT-Monitor:	VGA, SVGA up to 768 x 1024 pixels 16/256 colors	
Flatpanel:	TFT:	640 x 480 with 8/16/256 colors
	STN:	640 x 480 monochrome
	STN:	640 x 480 with 256 colors
	Plasma:	up to 1280 x 1024
	EL:	640 x 350 , 640 x 480, 768 x 1024 pixels
Controller Modes:	CRT only; Flatpanel only or simultaneous CRT and Flatpanel	
LCD-BIAS:	not available onboard	
Drivers:	Windows	
Mass Storage:		
FD:	Floppy disk interface, for max. 1 floppy with 26pin connector	
HD:	IDE interface, AT - Type, for max. 2 harddisks, 44pin connector, for 1.3, 1.8 and 2.5" harddisk with 44pin IDE	

Sockets SSD:

1st socket:	READ/WRITE/BOOTABLE Flashdiskmodule 512kByte - 8MByte
IDE:	MSFLASH-Drive 4MB or 10MB onboard mountable

Standard AT Interfaces:

Serial:

Name	FIFO	IRQs	Addr.	Standard
COM1	no	IRQ4	3F8	TTL / RS485 (ltc485)
COM2	yes	IRQ3	2F8	RS232C
COM3	yes	IRQ4/5/10	3E8	RS232C

COM3 is default on IRQ10. It may be jumpered to IRQ 4 or IRQ5.
(Baudrates: 50 - 115 KBaud programmable)

Parallel:	LPT1 printer interface mode: SPP (output only) , EPP (bidirectional)
Keyboard:	AT or PS/2 –keyboard
Keymatrix	8 x 16
Mouse:	AT or PS/2
Speaker:	0.1 W output drive
RTC:	integrated into the ELAN310, RTC with CMOS-RAM 128Byte
Backup current:	<50 µA
Battery:	3.6V 70mAh Ni-Cd or NiMh or external

Supervisory:

Watchdog:	LTC1232 with power-fail detection, strobe time max. 1sec.

BUS:

PC/104	IEEE-996 standard bus, buffered with 24mA
Clock:	8 MHz or programmable

Peripheral Extension:

with PC/104 BUS

Power Supply:

Working:	5 Volts ± 5%	
Power Rise Time:	>100µs (0V --> 4,75V)	
Current:	SV: 740mA nominal	SN: 400mA nominal
	SV: 410mA in sleep mode	SN: 210mA in sleep mode

Physical Characteristics:

Dimensions:	Length:	90 mm
	Depth:	96 mm
	Height:	20 mm
Weight:	SV: 90gr / SN: 70gr	
PCB Thickness:	1.6 mm / 0.0625 inches nominal	
PCB Layer:	8 with separate ground and VCC plane for low noise	

Operating Environment:

Relative Humidity:	5 - 90% non condensing		
Vibration:	5 to 2000 Hz		
Shock:	10 G		
Temperature:	Operating:	Standard version:	-25°C to +70°C *)
		Extended version:	-40°C to +85°C T.B.A.
	Storage:	-55°C to +85 °C *)	
	*) with onboard backupbattery, only +60°C peak are allowed.		

EMI / EMC (IEC1131-2 refer MIL 461/462):

ESD Electro Static Discharge:	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 metallic protection needed separate Ground Layer included 15 kV single peak
REF Radiated Electromagnetic Field:	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. not tested
EFT Electric Fast Transient (Burst):	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements:	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2 kV, 6 pulse/minute I/O: 500 V, 2 pulse/minute FD, CRT: none
High-frequency radiation:	EN55022

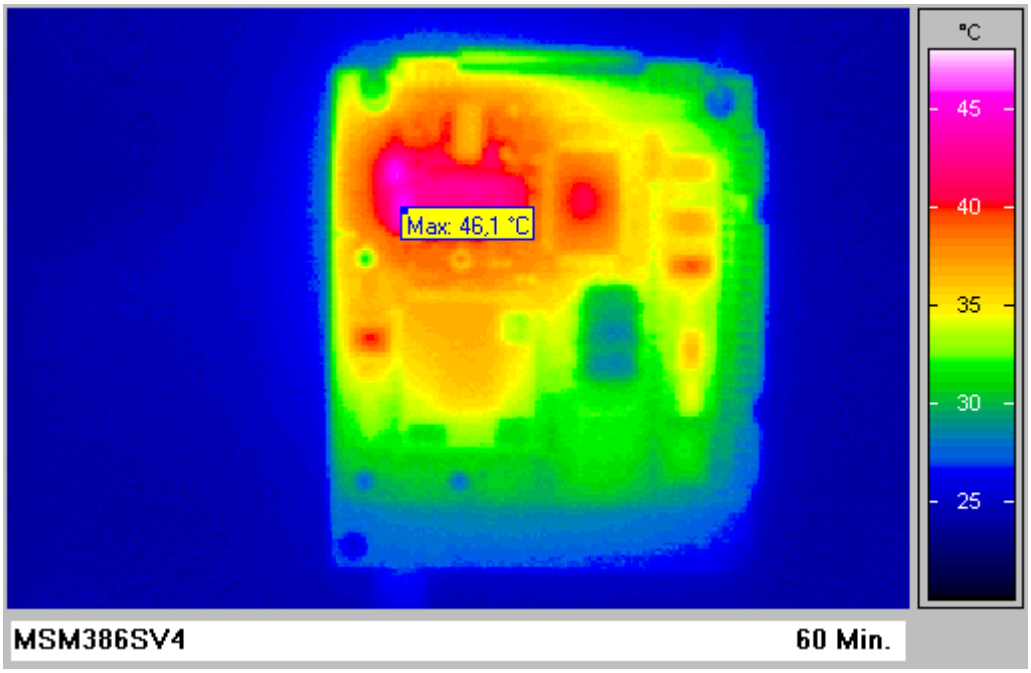
Compatibility:

MSM386SV/SN:	mechanically compatible to our MSMx86 Boards and to all other PC/104 boards

Any information is subject to change without notice.

2.5 Thermoscan

Product: MSM386SV4 Scan time: 60min.



2.6 Ordering Codes

MSM386SV2	with 2 MB DRAM, with VGA/LCD	-25°C to +70°C BurnIn proofed, 33MHz
MSM386SV4	with 4 MB DRAM, with VGA/LCD	-25°C to +70°C BurnIn proofed, 33MHz
MSM386SN2	with 2 MB DRAM, without VGA/LCD	-25°C to +70°C BurnIn proofed, 33MHz
MSM386SN4	with 4 MB DRAM, without VGA/LCD	-25°C to +70°C BurnIn proofed, 33MHz
-E48	Extended temperature range	-40°C to +85°C BurnIn proofed, 25MHz
MSFLASH4	Flashdrive 4 MB on IDE interface	
MSFLASH10	Flashdrive 10 MB on IDE interface	
MSM3/486V/-CK	Cablekit for MSM386V/486V/486DX	
MSSD-F2S0	Flashdisk Module 2 MB	
MSSD-F4S0	Flashdisk Module 4 MB	
MSSD-F6S0	Flashdisk Module 6 MB	
MSSD-F8S0	Flashdisk Module 8 MB	
MSSD-F0S1	SRAM Module 1 MB	
MSFLA-05DL	Flash Device 29F040 with 512kB DIL32	

2.7 Incompatibilities or Warnings for the ELAN300/310

1. The ELAN300 has an internal PCMCIA controller, the external must have an alternative address

The internal PCMCIA controller operates at the address 3E0h / 3E1h. Using the MSM386SV board with an MSM104J PCMCIA board needs the following modification on the MSM104J board:

J18 = 2-3 and J14 = 1-2 -> Base Address is now 3E2h

The MMCD.SYS receives the option /B:3E2h

Boot option for selecting the Index Base Addresses on the MSM104J board:

J18	**J14:**			
INTR:	SPKROUT:	Index Base:	I/O Address:	Comment:
1-2 (VCC)	1-2 (VCC)	00h	3E0h/3E1h	DEFAULT
1-2 (VCC)	2-3 (GND)	80h	3E0h/3E1h	
2-3 (GND)	1-2 (VCC)	00h	3E2h/3E3h	(needed on ELAN300/400 boards)
2-3 (GND)	2-3 (GND)	80h	3E2h/3E3h	

2.8 Related Application Notes

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38	ELAN310 with IDE
39	ELAN310 IRQ for COM-Ports
44	Akku as a backup power for the RTC data
45	COM3 to COM1
52	EPP Mode for MSM386SV/SN
54	Problem between powerdown and int COM disable
55	All you wish to know about COM on MSM386SV/SN
57	PCMCIA Controller of the ELAN or VADEM
65	MSM386SV and MSMJ104/D, SYSCLK-Loads
78	Several versions of the FFS format
80	High frequency Radiation (to meet EN55022)
84	Power consumption on Pentium / any other boards with attached drives (HDD, CD)

➔ *Application Notes are availble at http://www.digitallogic.com ->support, or on any Application CD from DIGITAL-LOGIC.*

2.9 BIOS History

Version:	Date:	Status:	Modifications:
1.40	**Juni 97**	**released**	**Basic BIOS**
1.41	Aug. 98	released	Y2K support added, FFS V6.0
1.42	Feb. 99	released	C-Segment Shadow programmable Wait Time for ALT-CTRL-S longer FFS V7.02
1.43	May 99	released	Boot with video shadow FFS 7.02 read & write, read only correction
1.44	27.10.2000	released	FFS 7.03, EEPROM support added

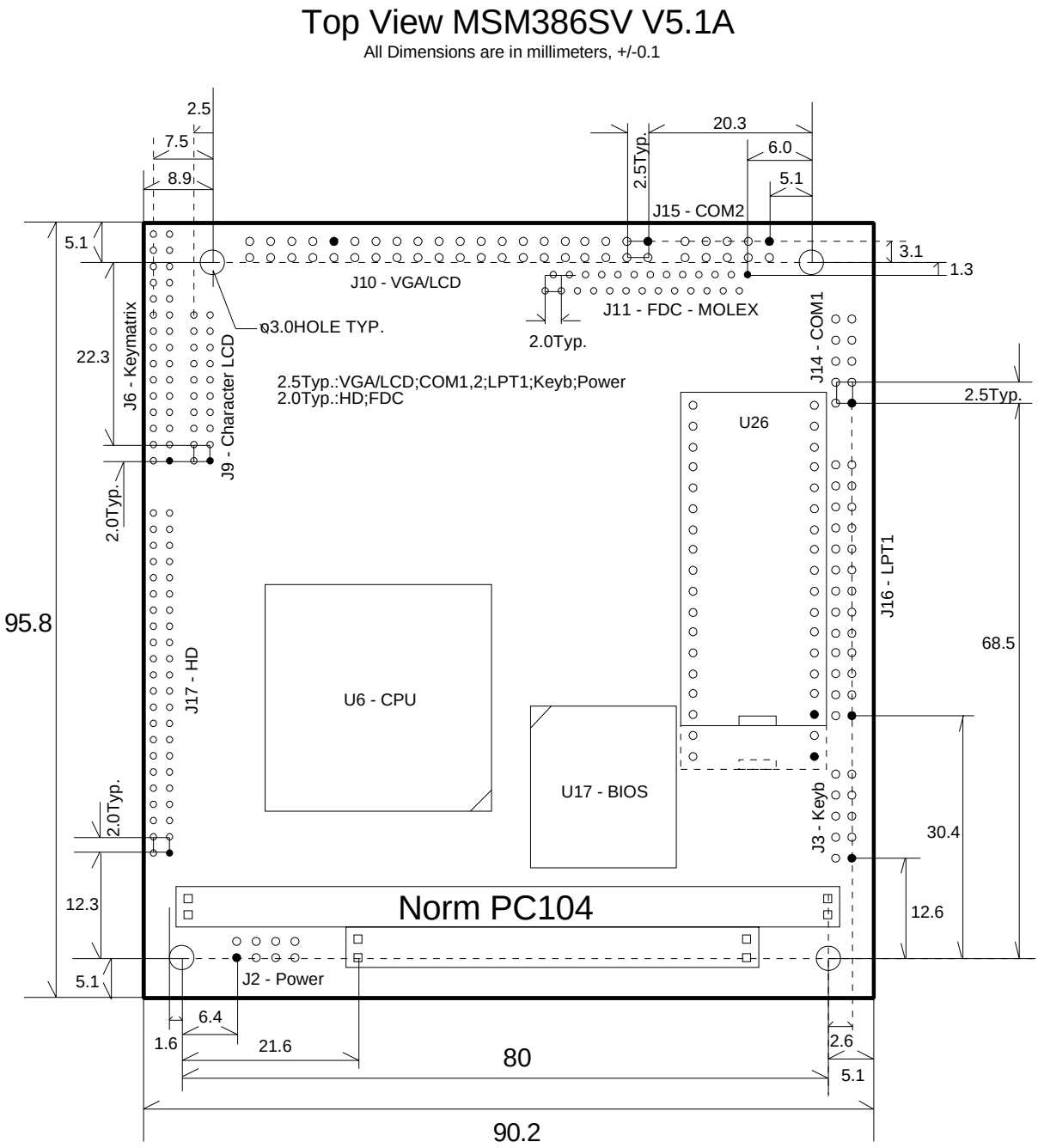
2.10 This product is "YEAR 2000 CAPABLE"

This DIGITAL-LOGIC product is "YEAR 2000 CAPABLE". This means, that upon installation, it accurately stores, displays, processes, provides and/or receives date data from, into, and between 1999 and 2000, and the 20. and 21. centuries, including leap year calculations, provided that all other technology used in combination with said product properly exchanges date data with it. DIGITAL-LOGIC makes no representation about individual components within the product should be used independently from the product as a whole. You should understand that DIGITAL-LOGIC's statement that an DIGITAL-LOGIC product is "YEAR 2000 CAPABLE" means only that DIGITAL-LOGIC has verified that the product as a whole meet this definition when tested as a stand-alone product in a test lab, but dies not mean that DIGITAL-LOGIC has verified that the product is "YEAR 2000 CAPABLE" as used in your particular situation or configuration. DIGITAL-LOGIC makes no representation about individual components, including software, within the product should they be used independently from the product as a whole.

DIGITAL-LOGIC customers use DIGITAL-LOGIC products in countless different configurations and in conjunction with many other components ans systems, and DIGITAL-LOGIC has no way to test wheter all those configurations and systems will properly handle the transition to the year 2000. DIGITAL-LOGIC encourages its customers and others to test whether their own computer systems and products will properly handle the transition to the year 2000.

The only proper method of accessing the date in systems is indirectly from the Real-Time-Clock via the BIOS. The BIOS in DIGITAL-LOGIC computerboards contain a century checking and maintenance feature the checks the laest two significant digits of the year stored in the RTC during each BIOS request (INT 1A) to read the date and, if less than '80' (i.e. 1980 is the first year supported by the PC), updates the century byte to '20'. This feature enables operating systems and applications using BIOS date/time services to reliably manipulate the year as a four-digit value.

2.11 Mechanical dimensions



2.12 RTC - Reset / Battery IMPORTANT INFORMATION

The ELAN3x0 device includes a built-in 146818A compatible realtime clock (RTC) with 114 bytes of SRAM. The RTC SRAM is designed to hold configuration data and to maintain accurate time and date when the rest of the system is powered down. This state is called the MICRO POWER OFF mode. MICRO POWER OFF mode allows the system to conserve battery power by removing all power to all system components and the ELAN300 device except for the AVCC and the VCC pins. Maintaining power on these pins allows the RTC to remain powered up, preventing the system from losing ist configuration, time and data data. This feature allows an AT-compatible system to be implemented without using an external RTC device.

REAL TIME CLOCK

The ELAN300 is designed to operate properly, while in MICRO POWER OFF mode, at voltages all the way down to 2.4V with the power consumption of around 40µA. Any source below 2.4V will not guarantee proper functionality, which could mean the loss of system configuration data, date and time.

BACKUP BATTERY

The MICRO POWER OFF mode of the ELAN300 allows the main system power source to be turned off and a backup source to be switched in to maintain power for the RTC.

IMPORTANT POINT 1:

If a RTC backup battery is installed on the system , while the main power is off, the ELAN300 will come up in an undefined state causing power consumption in the mA range which could drain the backup battery! There are also IRQ accessing errors possible.

1. Solution:

The backup battery must be installed after the system is powered with the main source, and is fully working. Therefore close jumper J5 only if the main source is already on.

IMPORTANT POINT 2:

If the RTC backup battery goes under 2.4V the MICRO POWER OFF mode will be stopped, and the system will loose all configuration from the RTC. If the system main power is switched on, the configuration data will be copied form the EEPROM to the RTC SRAM.
If the backup battery is not fully empty (in the range of 0.4V to 1.8V), the system will not come up when the main power is on, because the ELAN is in an undefined state. In this case, the backup battery must be fully interrupted for a very short time (by opening the J5 jumper). After the system has started, the jumper could be closed and the system should be powered until the backup battery is fully charged.

2.A solution:

In every design, using a backup battery for the RTC (also the onboard accu), install a reset switch with a cable to jumper J5. This switch should be placed in the rearside of the case, and should be activated only with a small pen. This prevents from accidently resetting the RTC, if the system if powered off.
Indicate in your operating manual, that the system could hang, if the RTC battery is nearly fully unloaded. Only in this case, this RTC-Reset switch must be pressed, to interrupt J5 for a short time until the main power is on. All palmtop computers have exactly the same RTC reset switch!

2.B solution:

If you do not need an RTC date and time, dismount the backup battery and start every bootup from the EEPROM configuration values. In this case, nothing must be observed.

2.13 High frequency radiation (to meet EN55022)

Since the PC/104 CPU modules are very high integrated embedded computers, no peripheral lines are protected against the radiation of high frequency spectrum. To meet a typical EN55022 requirement, all peripherals, they are going outside of the computer case, must be filtered externaly.

Typical signals, they must be filtered:

Keyboard:	KBCLK, KBDATA, VCC
Mouse:	MSCLK, MSDATA, VCC
COM1/2/3/4:	All serial signals must be filtered
LPT:	All parallel signals must be filtered
CRT:	red,blue,green, hsynch, vsynch must be filtered

Typical signals, they must not be filtered, since they are internaly used:

IDE:	connected to the harddisk
Floppy:	connected to the floppy
LCD:	connected to the internal LCD

1. For peripheral cables:

Use for all DSUB connector a filtered version. Select carefully the filter specifications. Place the filtered DSUB connector directly frontside and be sure that the shielding makes a good contact with the case.

9pin	DSUB connector from AMPHENOL:	FCC17E09P	820pF
25pin	DSUB connector from AMPHENOL:	FCC17B25P	820pF

2. For stackthrough applications:

Place on each peripheral signal line, they are going outside, a serial inductivity and after the inductivity a capacitor of 100pF to 1000pF to ground.
In this case, no filtered connectors are needed. Place the filter directly under or behind the onboard connector.

Serial Inductivity:	TDK HF50ACB321611-T	100MHz, 500mA, 1206 Case
Ground capacitor:	Ceramic Capacitor with 1000pF	

Power supply:

Use a current compensated dualinductor on the 5V supply e.g.

SIEMENS B82721-K2362-N1 with 3.6A , 0.4mH

3 PC/104 BUS SIGNALS

AEN, output
Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle , high = DMA Cycle**

BALE, output
Address Latch Enable is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17..23. The SA0..19 address lines latched internally according to this signal. BALE is forced high during DMA cycles.

/DACK[0..3, 5..7], output
DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQO through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

DRQ[0..3, 5..7], input
DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQO through DRQ3 will perform 8-Bit DMA transfers; DRQ5-7 are used for 16 accesses.

/IOCHCK, input
IOCHCK/ provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

IOCHRDY, input
I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held in the range of 125-15600nS. **low = wait, high = normal operation**

/IOCS16, input
I/O 16 Bit Chip Select signals the system board that the present data transfer is a 16-Bit, 1 wait-state, I/0 cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8 Bit I/O transfer, the default transfers a 4 wait-state cycle.

/IOR, input/output
I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is **active low**.

/IOW, input/output
I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

IRQ[3 - 7, 9 - 12, 14, 15], input
These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

/Master, input
This signal does not exist on the ELAN3xx designs.

/MEMCS16, input
MEMCS16 Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-Bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 2OmA.

/MEMR input/output
These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

/MEMW, input/output
These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low.**

OSC, output
Oscillator (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100µs after reset is inactive.

RESETDRV, output
Reset Drive is used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is active high. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

/REFRESH, input/output
This signal does not exist on ELAN3xx designs (onboard pulled up to VCC).

SAO-SA19, LA17 - LA23 input/output
Address bits 0 through 19 are used to address memory and I/0 devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SAO through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16 MBytes range. These signals are generated by the microprocessors or DMA controllers.

/SBHE, input/output
Bus High Enable (system) indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. 16Bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

SD[O..15], input/output
These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/0 devices. DO is the least-significant Bit and D15 is the most significant Bit. All 8-Bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-Bit devices will use DO through D15.

/SMEMR input/output
These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

/SMEMW, input/output
These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low.**

SYSCLK, output
This is a 8 MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

TC output
Terminal Count provides a pulse when the terminal count for any DMA channel is reached. Onboard from FD used.

/OWS, input
The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles.

12V +/- 5%
Used only for the flatpanel supply.

The Bus currents are:

Output Signals:	IOH:	IOL:
D0 - D16	12 mA	12 mA
A0 - A23	12 mA	12 mA
MR, MW, IOR, IOW, RES, ALE, AEN, C14	12 mA	12 mA
DACKx, DRQx, INTx, PSx, OPW	12 mA	12 mA

Output Signals:	Logic Family:	Voltage:
Input Signals:	ABT-Logic ViH (min.) = 2.15 V	ABT-Logic Vil (max.) = 0.85 V

4 DETAILED SYSTEM DESCRIPTION

This system has a system configuration based on the ISA architecture. Check the I/O and the Memory map in this chapter.

4.1 Power Requirements

The power is connected through the PC/104 power connector; or the separate power connector on the board. The supply uses only the +5 Volts and ground connection.

Warning: Make sure that the power plug is wired correctly before supplying power to the board!

4.1.1 Powersave Modes

	MSM386SV/SN	MSM486SV	MSM486DX	MSM486DX	PCC-P5	PCC-P5
DRAM	4	8	16	16	16	16
3.3V Gen.	linear	linear	linear	switched	linear	switched
Fullspeed	33MHz	66MHz	100MHz	100MHz	166MHz	166MHz
at 5.0V	600mA	1000mA	1800mA	1300mA	4000mA	3000mA
Power	3W	5W	9W	6.5W	20W	15W
↓ Powerdn	Ti, Sus, Sw	Ti, Sus, Sw	Ti, Sw	Ti, Sw	Ti	Ti
Low Speed	20MHz	33MHz	4MHz	4MHz	10MHz	10MHz
at 5.0V	450mA	800mA	850mA	800mA	2000mA	1800mA
Power	2W	4W	4.5W	4W	10W	9W
VGA,MAX	on	on	on	on	on	on
↓ Powerdn	Ti, Sus, Sw	Ti, Sus, Sw	Ti, Sw	Ti, Sw	Ti	Ti
↑ Powerup	Ac, Res, Sw	Ac,Res, Sw	Ac, Res	Ac, Res	Ac	Ac
Suspend	1MHz	1MHz				
at 5.0V	160mA	180mA				
Power	0.8W	0.9W				
VGA	off	off				
MAX211	off	off				
↓ Powerdn	Ti, Sus, Sw	Ti, Sus, Sw				
↑ Powerup	Ac, Res, Sw	Ac,Res, Sw				
Sleep	0MHz	0MHz	0MHz	0MHz		
at 5.0V	140mA	160mA	600mA	600mA		
VGA	off	off	off	off		
MAX211	off	off	on	on		
Keyboard	off	off	off	off		
↑ Powerup	Res	Res	Res	Res		

In all powermodes, the program is resident in the refreshed DRAM!

Others: KBD = 10mA, Floppy = 10mA, HD = 300mA/10mA, Flashdisk = 1mA, VGA = ~300mA

Remarks:	Ti	1s to 24h prog.=	Timer controlled (modifiable in the CMOS-Setup)
	Sus/Res	500ms =	Suspend / Resume signal (hardware)
	Sw	500ms =	Software controlled, by programming a register
	Ac	500ms =	Activity, Keyboard pressed, Mouse, COMx,

4.2 CPU, Board and RAMs

4.2.1 CPU of this MICROSPACE Product

Processor:	Type:	Clock:	Landmark MHz:	Landmark Units:
ELAN 310-B4	AMD	33 MHz	30 MHz	100

4.2.2 Numeric Coprocessor

Is not integrated in the ELAN 310 CPU.

4.2.3 DRAM Memory

Speed:	70ns
Size:	soldered onboard SOJ DRAMs
Bits:	16 Bit
Capacity:	2 or 4 MBytes
Bank:	1 or 2

4.3 Interface

4.3.1 Keyboard AT-compatible and PS/2 Mouse

J3

Pin	Signal
Pin 1	Speaker out
Pin 2	Resume Input
Pin 3	Reset Input. A mechanical pushbutton or an active logic signal can drive the reset input. The debounced input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or grater.
Pin 4	VCC
Pin 5	Keyb. Data
Pin 6	Keyb. Clock
Pin 7	Ground
Pin 8	Ext. Battery
Pin 9	Mouse Clock (PS/2)
Pin 10	Mouse Data (PS/2)

4.3.2 Line Printer Port LPT1

A standard bi-directional LPT port is integrated in the MICROSPACE PC.

Further information about these signals is available in numerous publications, including the IBM technical reference manuals for the PC and AT computers and from some other reference documents.

The current is: IOH = 12 mA IOL = 24mA

The SMC 37C666 may be programmed with reset strap options in the following modes:

Parallel Port Address (default LPT1)

The jumpers are available since board version 5.1.

PCF1 (RTS1) R50 / J51	PCF0 (TXD1) J22	port address	IRQ
low 1-2	low 2-3	disabled	7
low 1-2	high 1-2	PS2 3BCh	7
high 2-3	**low 2-3**	**LPT1 378h**	7
high 2-3	high 1-2	LPT2 278h	7

In order to make any changes the resistor must be wired to the other potential.

Parallel Port Mode (default normal)

The jumpers are available and the DACK7/DRQ7 are connected since board version 5.1!

ECPEN (MTR2) J53	PADCF (GAME) J52	port function
low 1-2	low 1-2	Standard Printer Port, output only
low 1-2	high 2-3	Enhanced Printer Port (EPP), bidirection
high 2-3	**low 1-2**	**Extended Capabilities Printer Port (ECP)**
high 2-3	high 2-3	ECP & EPP

ATTENTION:
If others than standard mode are used, check the BIOS-setup, that the " INTERNAL LPT PORT" is disabled. For EPP and ECP mode, the LPT port is using the DMA7 and the IRQ7.

4.3.3 Serial Ports COM1-COM2-COM3

The serial channels are fully compatible with 16C550 UARTS. COM1 is the primary serial port, and is supported by the board's ROM-BIOS as the PC-DOS 'COM1' device. The secondary serial port is COM2; it is supported as the 'COM2' device. In the BIOS Setup only COM1 is programmable. The COM2 and COM3 is hardware defined.

Standard:	COM 3/2:	37C666 (SMC):	2 x 16C550 compatible serial interfaces with RS232C
	COM1:	ELAN310:	1 x 16C450 compatible serial interface with RS485

Serial Port Connectors COM2, COM3

Pin	Signal Name	Function	in/out	DB25 Pin	DB9 Pin
1	CD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear to Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicator	in	22	9
9	GND	Signal Ground		7	5

The serial port signals are compatible with the RS232C specifications.

The COM of the ELAN (default COM1)

ELAN	port address	IRQ
register int com disabled	Disabled	
register int com enabled	**COM1 3F8h**	4

To make any changes the BIOS must be modified.

The internal UART is hardwired on the address of the COM1 and of the IRQ4. No other modification to other addresses or IRQ numbers are possible.

The SMC 37C666 may be programmed with reset strap options in the following modes:
The first serial channel is in the ELAN controller (if enabled in the BIOS-Setup, always on COM1).

J14 = Second serial channel (default COM3)

S1CF1 (IDELO line) R45	S1CF0 (IDEHI line) R46	port address	IRQ
low	low	Disabled	4, 5, 10
low (COM3)	**high**	**COM3 3E8h**	**4, 5, 10**
high	low	COM2 2F8h	4, 5, 10
high (COM1)	high	COM1 3F8h	4, 5, 10

In order to make any changes the resistor must be wired to the other potential. If the internal UART from the ELAN300 is disabled (BIOS-Setup), J14 may be configured as COM1 (by setting wiring the R45 to Vcc instead to GND).
In the future, the settings will be done by the CMOS- setup, and the new board version (V5.1) will use J54 instead of wiring the R45 (see also chapter 6).

J15 = Third serial channel (default COM2)

S2CF1 (DTR1 line) R53	S2CF0 (RTS2 line) R51 or J50	port address	IRQ
low	low	Disabled	3
low	high	COM4 2E8h	3
high	low	COM1 3F8h	3
high	**high**	**COM2 2F8h**	3

In order to make any changes the resistor must be wired to the other potential.

4.3.4 Serial Ports RS485 on COM1

The RS485 interface is controlled by the RTS/DTS outputs. The application must be able to control the RS485 port correctly.

Function:	Output: RS485	Input: RS485	RTS-Output = DE of the LTC485 (3FCh Bit1)	DTS-Output = RE/ of the LTC485 (3FCh Bit0)	Remarks:
RS485	Enabled	Disabled	0	0	Transmit Data
RS485	Enabled	Enabled	0	1	TxD & RxD, Loopback
RS485	Disabled	Disabled	1	0	No Bus Access
RS485	Disabled	Enabled	1	1	Receive only Data

4.3.5 Floppy Disk Interface

The onboard floppy disk controller and ROM-BIOS support one or two floppy disk drives in any of the standard PC-DOS and MS-DOS formats shown in the table.

Supported Floppy Formats

Capacity	Drive size	Tracks	Data rate	DOS version
1.2 MB	5-1/4"	80	500 KHz	3.0 - 6.22
720 K	3-1/2"	80	250 KHz	3.2 - 6.22
1.44 M	3-1/2"	80	500 KHz	3.3 - 6.22

Floppy Interface Configuration

The desired configuration of floppy drives (number and type) must be properly initialized in the board's CMOS - configuration memory. This is generally done by using CTRL + ALT + 'S' at bootup time.

Floppy Interface Connector

The table shows the pinout and signal definitions of the board's floppy disk interface connector. It is identical in pinout to the floppy connector of a standard AT. Note that, as in a standard PC or AT, both floppy drives are jumpered to the same drive select: as the 'second' drive. The drives are uniquely selected as a result of a swapping of a group of seven wires (conductors 10-16) that must be in the cable between the two drives. The seven-wire swap goes between the computer board and drive 'A'; the wires to drive 'B' are unswapped (or swapped a second time). The 26 pin high density (1mm pitch FCC) connector has only one drive and motor select. The onboard jumper defines the drive A: or B:. Default is always A:.

Floppy Disk Interface Technology

We only support CMOS drives. That means that the termination resistors are 1 Kohm. 5 1/4“-drives are not recommended (TTL interface).

The 26 pin connector: FFC/FPC 0.3mm thick 1.0mm (0.039") pitch (MOLEX 52030 Serie)

Floppy Disk Interface connector

FD26: Pin	Signal Name	Function	in/out
1	VCC	+5 volts	
2	IDX	Index Pulse	in
3	VCC	+5 volts	
4	DS2	Drive Select 2	out
5	VCC	+5 volts	
6	DCHG	Disk Change	in
10	M02	Motor On 2	out
12	DIRC	Direction Select	out
14	STEP	Step	out
16	WD	Write Data	out
17	GND	Signal grounds	
18	WE	Write Enable	out
19	GND	Signal grounds	
20	TRKO	Track 0	in
21	GND	Signal grounds	
22	WP	Write Protect	in
23	GND	Signal grounds	
24	RDD	Read Data	in
25	GND	Signal grounds	
26	HS	Head Select	out

4.3.6 Speaker Interface

One of the board's CPU device provides the logic for a PC compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides approximately 0.1 watt of audio power to an external 8 ohm speaker. Connect the speaker between VCC and speaker output to have no quiescient current.

4.4 Controllers

4.4.1 Interrupt Controllers

An 8259A compatible interrupt controller, within the chipset device, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt:	Sources:	onboard used:
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2 serial port	yes
IRQ4	COM1 + COM3 remappable to IRQ5, IRQ10	yes
IRQ5	Free for user Remappable to COM3	no
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Alarm function of the RTC	yes
IRQ9	Free for user	no
IRQ10	Free for user Remappable to COM3	no
IRQ11	Free for user	no
IRQ12	PS/2 mouse	yes
IRQ13	Math. coprocessor	not available
IRQ14	Harddisk IDE	yes
IRQ15	Free for user	no

4.5 Timers and Counters

4.5.1 Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190 MHz clock, derived from a 14.318 MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Timer Assignment

Timer	Function
0	ROM-BIOS clock tick (18.2 Hz)
1	DRAM refresh request timing (15 µS)
2	Speaker tone generation time base

4.5.2 Battery Backed Clock (RTC)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

One unique feature of the board's battery-backed clock device is that it contains the backup battery directly on the board. The battery is rated for a minimum of 100 days of clock and internal CMOS RAM backup under conditions of no power to the board.

The battery is a DIGITAL-LOGIC AG replacement part. The battery-backed clock can be set by using the DIGITAL-LOGIC AG SETUP at boot-time.

Addresses:	70h	=	Index register
	71h	=	Data transfer register
RTC-Address MAP:	00 - 0F		Real time clock
	10 - 3F		BIOS setup (Standard)
	40 - 7F		Extended BIOS

The onboard NiCd or NiMH+ battery has a capacity of 70mAh. The chipset consumes the following currents:

Typical battery current at 25°C : <50 µA

The J5 jumper must be closed, if the main power supply +5V is applied to the board. Otherwise the battery standby current will be increased !

4.5.3 Watchdog

The watchdog timer is not tested in the current product version.
To activate the watchdog, install jumper J28. Use the special function in INT15h to strobe the watchdog periodically.

D7 = '1' : Watchdog not strobed
D7 = '0' : Watchdog is strobed with 32kHz

4.5.4 Watchdog Programming example

The watchdog may be initiated also directly from an applicationsoftware.
Attention: J28 must be closed, if any WDOG function should work.

Enable Watchdog (reset after 0.5sec, staying enabled)

```
mov  dx, 2B0h
mov al,078h
out  dx,al
```

Disable Watchdog (no reset)

```
mov  dx, 2B0h
mov al,0F9h
out  dx,al
```

We recommend to use the INT15 function to handle the WatchDog. Only for special and rare cases (ex. RTC systems) , the above programming of the hardware level should be used.
Refers also to chapter 9.2.

4.6 BIOS

4.6.1 ROM-BIOS Sockets

An EPROM socket with 8 Bit wide data access normally contains the board's AT compatible ROM-BIOS. The socket takes any of a 27C010 to 27C040 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this socket. The ROM-BIOS sockets occupies the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules. Consult the appropriate address map for the MICROSPACE MSM386SV/SN ROM-BIOS sockets.

4.6.1.1 Standard BIOS ROM

DEVICE: PLCC32 90ns

Map:	27/28F020:	29F040:	PC-Adress:	Function / BIOS-Extensions:
	00000-07FFF	40000-47FFF	C0000-C7FFF	VGA BIOS from Chips & Technology
	08000-0FFFF	60000-67FFF	E0000-E7FFF	BIOS-Extensions, FFS, BurnIn
	20000-3FFFF	68000-7FFFF	E8000-FFFFF	Chipset BIOS

4.6.2 EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2048 Bytes.

Organisation of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Keymatrix-Setup valid (01=valid)**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Booterrors (Autoincremented if any booterror occurs)
0123h-0125h	Setup Entries (Autoincremented on every Setup entry)
0126h-0128h	Low Battery (Autoincremented everytime the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Autoincremented on every poweron start)
0130h	Number of 512k SRAM
0131h	Number of 512k Flash
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom)
0137h	CPU TYPE (01h=ELAN300/310, 02h=ELAN400, 03h=486SLC, 04h=486DX, 05h=P5).
0200h-03FFh	**Keymatrix-Setup data**
0200h-027Fh	Keymatrix Table
0400h-07FFh	**Free for Customer’s use**

4.6.3 BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM with the CMOS-RESET jumper. If the battery is down, it is always possible to start the system with the default values from the BIOS.

The following entries may be made:

Date: The current Real Date of the RTC

Time: The current Real Time of the RTC

Drive: A or B

none	=	no drive present, SSD / ROM-Disk enabled (if device is loaded)
360k	=	5,25" low density drive, SSD enabled
1,2 MB	=	5,25" high density drive
720 K	=	3,5" low density drive
1,44 MB	=	3,5" high density drive (Default for A:)

The A: Drive is the bootable drive.

Display type:

CRT:	for Mono CRTs, no LCD operating possible.
40 x 25:	for Color CGA or LCD
80 x 25:	for Color CGA or LCD (Default)
VGA:	for VGA

Harddisk type: defines which drive is connected
Type = 0 means no drive is present (Default)!
Drive type 48 and 49 enable you to define a custom harddisk parameter.

WARNING:

On the next setup pages (switched with PgDn and PgUp) the values for special parameters are modifiable. Normally the parameters are set correctly by DIGITAL-LOGIC AG. Be very careful in modifying any parameter since the system could crash. Some parameters are dependent on the CPU type. The cache parameter is always available, for example. So, if you select too few wait states, the system will not start until you reset the CMOS-RAM using the RAM-Reset jumper, but the default values are reloaded. If you are not familiar with these parameters, do not change anything.

4.6.4 CMOS Setup Harddisk List

Use type 48 and type 49 for user defined harddisk entries. Enter the sectors, cylinders and the number of heads. Use the AUTODETECT mode for identifing the harddisk automatically after power-up.

If the used harddisk is larger than 508Mbyte, you must ENABLE the option HD1/2 TRANSLATE PARAMETER to switch on the LBA-Mode for capacities up to 8GByte.

4.6.5 CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64 bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

SystemSoft's BIOS supports 128 bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain System BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of Day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of Day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power

Continued...

CMOS Map Continued...

Location	Description
0Eh	CMOS Location for Bad CMOS and Checksum Flags bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code
10h	Diskette Drives bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 K 0010 = Drive A = 1.2 MB 0011 = Drive A = 720 K 0100 = Drive A = 1.44 MB 0101 = Drive A = 2.88 MB bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 K 0010 = Drive B = 1.2 MB 0011 = Drive B = 720 K 0100 = Drive B = 1.44 MB 0101 = Drive B = 2.88 MB
11h	Reserved
12h	Fixed (Hard) Drives bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 19h. bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 2Ah. See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
13h	Reserved

Continued...

CMOS Map Continued...

Location	Description
14h	Equipment bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome bits 3-2 = Reserved bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in KB) - Low Byte
16h	Base Memory Size (in KB) - High Byte
17h	Extended Memory Size in (KB) - Low Byte
18h	Extended Memory Size (in KB) - High Byte
19h	Extended Drive Type - Hard Drive 0 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Ah	Extended Drive Type - Hard Drive 1 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Bh	Custom and Fixed (Hard) Drive Flags bits 7-6 = Reserved bit 5 = Internal Floppy Diskette Controller 0 = Disabled 1 = Enabled bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled bit 3 = Hard Drive 0 Custom Flag 0 = Disable 1 = Enabled bit 2 = Hard Drive 0 IDE Flag 0 = Disable 1 = Enabled bit 1 = Hard Drive 1 Custom Flag 0 = Disable 1 = Enabled bit 0 = Hard Drive 1 IDE Flag 0 = Disable 1 = Enabled

Continued...

CMOS Map Continued...

Location	Description
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 bytes (48 bits) contain the following data: Cylinders Landing Zone 10 bits Write Precomp 10 bits Heads Sectors/Track 8 bits
1Fh	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
20h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
21h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone
22h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
23h	Byte 4 bits 7-0 = Number of Heads
24h	Byte 5 bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 bytes (48 bits) contain the following data: Cylinders Landing Zone 10 bits Write Precomp 10 bits Heads Sectors/Track 8 bits
25h	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
26h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
27h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone

Continued...

CMOS Map Continued...

Location	Description
28h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
29h	Byte 4 bits 7-0 = Number of Heads
2Ah	Byte 5 bits 7-0 = Sectors Per Track
2Bh	Boot Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Ch	SCU Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (KB) detected by POST - Low Byte
31h	Extended RAM (KB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed bit 7 = Flag for Memory Size 0 = 640KB 1 = 512KB bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage bits 7-6 = Reserved bit 5 = Semaphore for Completed POST bit 4 = Semaphore for 0 Volt POST (not currently used) bit 3 = Semaphore for already in SCU menu bit 2 = Semaphore for already in PM menu bit 1 = Semaphore for SCU menu call pending bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

4.6.6 Default chipset values

HEX dump of MSM386SV BIOS V1.43:

Idx	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	00	00	00	00	00	00	00	00	00	10	00	00	1F	00	00	FF
10	00	00	00	00	00	00	00	00	20	20	20	20	20	20	20	20
20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
30	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
40	00	00	0A	00	FF	24	00	FF	20	20	20	20	20	20	20	20
50	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
60	52	52	52	52	2A	6B	52	00	00	00	52	52	00	40	00	00
70	60	00	00	00	06	00	00	10	00	FF	FF	FF	FF	FF	FF	FF
80	40	44	06	00	00	00	00	00	20	20	20	20	20	20	20	20
90	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
A0	B4	7F	B7	0F	08	00	00	32	00	C0	28	E7	01	13	00	00
B0	00	10	60	00	40	FF	FF	FF	10	04	00	00	10	04	00	00
C0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
D0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
E0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
F0	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20

4.6.7 Harddisk PIO Modes

Block Mode Transfer:
(Multi-Sector)

Block mode boots IDE drive performance by increasing the amount of data transferred.

No Block Mode: 512 Byte per interrupt
Block Mode: up to 64 kByte per interrupt

LBA Mode:

LBA (logical block addressing) is a new method of addressing data on a disk drive. In the standard ST506 (MFM) ISA hard disk, data is accessed via a cylinder - head - sector format.

LBA Mode disabled: max. 528 MByte per Disk

LBA Mode enabled: max. 8 GByte per Disk

Enable/Disable LBA-Mode: Enter the BIOS-Setup. Select the option HD1/2 TRANSLATE PARAMETER and switch this option ON or OFF.

4.6.8 EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing the keymatrix definitions, if the hardware supports a keymatrix (MSM386SV, MSM386SN, MSM486SV).
- Storing system informations like: version, production date, customisation of the board, CPU type.
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting up, the CMOS is automatically updated with the EEPROM values.

Press the Esc-key while powering on the system until the video shows the BIOS message and the CMOS will **not** be updated.

This would be helpful, if wrong parameters are stored in the EEPROM and the setup of the BIOS does not start.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (use the jumper to reset or disconnect the battery for at least 10 minutes).
2. Press Esc until the system starts up.
3. Enter the BIOS Setup:
   a) load DEFAULT values
   b) enter the settings for the environment
   c) exit the setup
4. Restart the system.

- The user may access the EEPROM through the INT15 special functions. Refer to the chapter SFI functions.
- The keymatrix is defined with special EDITMATR.EXE and SAVEMATR.EXE tools.
- The system information are read only information. To read, use the SFI functions.

4.7 Download the VGA-BIOS and the CORE-BIOS

Before downloading a BIOS, please check as follows:

- Select the SHADOW option in the BIOS, for a BIOS and VGA (if this option is available).
- Disable the EMM386 or other memory managers in the CONFIG.SYS of your bootdisk.
- Make sure, that the DOWN_xxx.EXE programm and the BIOS to download are on the same path and directory!
- Boot the DOS without config.sys & autoexec.bat -> press “F5” while starting DOS boot.
- Is the empty diskspace, where the down.exe is located, larger than 64kB (for safe storage)
- Is the floppydisk not write-protected

Start the DOWNLOADING Tool with:

- Start the corresponding download tool. Refer to the table to see which tool fits in, each productgroup has its own download tool. Do never use the wrong one!

Product:	BIOS-Core download	VGA-BIOS download	BIOS-Ext. download
File-Extension:	*.COR	*.V40 , *.V45 *.V48 depending on the product	*.BIN
BIOS Size:	128k	32k	32k
Addressrange:	E0000 - FFFFFh	C0000 – C7FFFh	C8000 - CFFFFh
MSM386SN	DOWN_3SN.EXE	-	-
MSM386SV	DOWN_3SV.EXE	DOWN_3SV.EXE	DOWN_3SV.EXE
MSM486SL	DOWN_4SN.EXE	-	-
MSM486SN	DOWN_4SN.EXE	-	-
MSM486SV	DOWN_4SV.EXE	DOWN_4SV.EXE	DOWN_4SV.EXE
MSM486SE / SEV	DOWN_4SE.EXE	DOWN_4SE.EXE	-
MSM486DN	DOWN_4DX.EXE	-	-
MSM486DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
SM-486PC / EK	DOWN_SM4.EXE	On the –EK : DOWN_SM4.EXE	-
SM-486PCX / EK	DOWN_S4X.EXE	DOWN_S4X.EXE	DOWN_S4X.EXE
MSM5x86DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
MSM586SEN / SEV	To be defined	To be defined	
MSM-P5	- AMI82602.EXE or - FLASHAMI.COM (AMIBOOT.ROM)**	DOWN_000.EXE	-
PCC-P5L / PCC-PII AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
PCC-P5L / PCC-PII PCC-P5S / PCC-P3S PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5S MSM-P5SV / SEV AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
MSM-P5SN / SEN AMI- BIOS	AMI82602.EXE	-	-
MSM-P5S MSM-P5SV / SEV PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5SN / SEN PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	-	-
MSEBX	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	
SMP5PC / 3PC / DK	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	
MAS-P5 / P3	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	

Remarks:
** Core- file has to be renamed as written in brackets

4.7.1 VGA- BIOS Download Function

The BIOS for the VGA must be downloaded, before a LCD is connected. This could be also a new LCD- display, which needs a corresponding VGA- BIOS.

How to download a VGA- BIOS:

1. Restart the system with the SHADOW enabled (if available) and no EMM386 loaded.
2. Check, if you find the DOWN_xxx.EXE and the *.V40 / *.000 files on your disk, to get downloaded.
3. Refer to the VGABIOS.DOC for more information about the VGABIOS files.
4. Insert the floppydisk with the program DOWN_xxx.EXE and all VGA-Drivers.
5. Start DOWN_xxx.EXE.
6. Check, if the DOWN program has identified the product and the shadow correctly.
7. Select the function PROGRAMM VGA- BIOS.
8. Select the VGA- BIOS out of the proposed file list (UP/DOWN arrows) and press ENTER.
9. Check, if the new VGA- header is displayed on the VGA- INFO- screen.
10. After proceeding, switch off the power and restart the board (cold start).

What is the filename of the BIOS-Files:

Operation:	Filename:	Size:
Download COREBIOS	*.COR	128k
Read the COREBIOS	READ_3SV.COR	128k
DOWNLOAD VGA	*.540, *.V40	32k
Read the VGABIOS	READ_VGA.540	32k
DOWNLOAD BIOSEXT	*.BIN	32k
Read the BIOSEXT	READC8CF.BIN	32k

If the download does not work:
- Check, if no EMM386 is loaded.
- Check, if no peripheral card is in the system, which occupies the same memory range. Disconnect this card.
- If the download is stopped or not completed, make only a warm boot and repeat the steps or download another file. As the video is may shadowed, everything is visible and a cold boot would clear the screen and nothing would be visible afterwards.

If the screen flickers or is misaligned after reboot:
- The previously loaded VGA- BIOS is not corresponding 100% or works only on the LCD properly.

If the screen is dark after the reboot of the system:
- A new system BIOS must be programmed. Ask DIGITAL-LOGIC AG for the binary file.

If the previous version is still programmed:
- Switch off the board and do not make a warm boot due to the fact that the data may are still stored in the memory shadow.

4.8 Memory / I/O Map

The AMD ELAN310™ CPU used as central processing unit on the MICROSPACE PC has a memory address space which is defined by 26 address bits. Therefore, it can address 64 MByte of memory. The memory address MAP is as follows:

CPU AMD ELAN310

Address:	Size:	Function / Comments:
0000000 - 009FFFFh	640 KBytes	Onboard DRAM for DOS applications
00A0000 - 00BFFFFh	128 KBytes	CGA, EGA, LCD Video RAM 128kB
00C0000 - 00C7FFFh 00C8000 - 00CFFFFh	32 KBytes 32 KBytes	VGA BIOS BIOS Extension
00D0000 - 00D4000h 00D4000 - 00DBFFFFh 00DC000 - 00DFFFFh	16 KBytes 32 KBytes 16 KBytes	No FFS: free for user With FFS: 64k used by the flashdisk With DOC2000: 16k used / 48k free With PCMCIA: additional 16k used
00E0000 - 00EFFFFh	64 KBytes	BIOS
00F0000 - 00FFFFFh	64 KBytes	BIOS
0100000 - 01FFFFFh	1 MByte	DRAM for extended onboard memory
0200000 - 03FFFFFh	2 MBytes	DRAM for extended onboard memory

Address:	Size:	Function / Comments:
1000000 - 1FFFFFF	16 MBytes	Flashdisk Window
2000000 - 2FFFFFF	16 MBytes	Reserved for PCMCIA Socket 1*
3000000 - 3FFFFFF	16 MBytes	Reserved for PCMCIA Socket 2*

- not available on MSM386SN/SV products!

4.8.1 System I/O map

The following table shows the detailed listing of the I/O port assignments used in the MICROSPACE board:

I/O Address	Read/Write Status	Description
0000h	R / W	DMA channel 0 address byte 0 (low), then byte 1
0001h	R / W	DMA channel 0 word count byte 0 (low), then byte 1
0002h	R / W	DMA channel 1 address byte 0 (low), then byte 1
0003h	R / W	DMA channel 1 word count byte 0 (low), then byte 1
0004h	R / W	DMA channel 2 address byte 0 (low), then byte 1
0005h	R / W	DMA channel 2 word count byte 0 (low), then byte 1
0006h	R / W	DMA channel 3 address byte 0 (low), then byte 1
0007h	R / W	DMA channel 3 word count byte 0 (low), then byte 1
0008h	R	DMA channel 0-3 status register bit 7 = 1 Channel 3 request bit 6 = 1 Channel 2 request bit 5 = 1 Channel 1 request bit 4 = 1 Channel 0 request bit 3 = 1 Terminal count on channel 3 bit 2 = 1 Terminal count on channel 2 bit 1 = 1 Terminal count on channel 1 bit 0 = 1 Terminal count on channel 0

Continued...

I/O Address	Read/Write Status	Description
0008h	W	DMA channel 0-3 command register bit 7 = DACK sense active high/low 0 low 1 high bit 6 = DREQ sense active high/low 0 low 1 high bit 5 = Write selection 0 Late write selection 1 Extended write selection bit 4 = Priority 0 Fixed 1 Rotating bit 3 = Timing 0 Normal 1 Rotating bit 2 = Controller enable/disable 0 Enable 1 Disable bit 1 = Memory-to-memory enable/disable 0 Disable 1 Enable bit 0 = Reserved
0009h	W	DMA write request register
000Ah	R / W	DMA channel 0-3 mask register bits 7-3 = Reserved bit 2 = 0 Clear bit 1 Set bit bits 1-0 = Channel Select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
00Bh	W	DMA channel 0-3 mode register bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

Continued..■

I/O Address	Read/Write Status	Description
000Ch	W	DMA clear byte pointer flip/flop
000Dh	R	DMA read temporary register
000Dh	W	DMA master clear
000Eh	W	DMA clear mask register
000Fh	W	DMA write mask register
0020h	W	Programmable Interrupt Controller - Initialization Command Word 1 (ICW1) provided bit 4 = 1 bits 7-5 = 000 Used only in 8080 or 8085 mode bit 4 = 1 ICW1 is used bit 3 = 0 Edge triggered mode 1 Level triggered mode bit 2 = 0 Successive interrupt vectors separated by 8 bytes 1 Successive interrupt vectors separated by 4 bytes bit 1 = 0 Cascade mode 1 Single mode bit 0 = 0 ICW4 not needed 1 ICW4 needed
0021h	W	Used for ICW2, ICW3, or ICW4 in sequential order afterICW1 is written to port 0020h **ICW2** bits 7-3 = Address A0-A3 of base vector address for interrupt controller bits 2-0 = Reserved (should be 000) **ICW3** (for slave controller 00A1h) bits 7-3 = Reserved (should be 0000) bits 2-0 = 1 Slave ID **ICW4** bits 7-5 = Reserved (should be 000) bit 4 = 0 No special fully nested mode 1 Special fully nested mode bits 3-2 = Mode 00 Non buffered mode 01 Non buffered mode 10 Buffered mode/slave 11 Buffered mode/master bit 1 = 0 Normal EOI 1 Auto EOI bit 0 = 0 8085 mode 1 8080 / 8088 mode

Continued...

I/O Address	Read/Write Status	Description
0021h	R / W	PIC master interrupt mask register (OCW1) bit 7 = 0 Enable parallel printer interrupt bit 6 = 0 Enable diskette interrupt bit 5 = 0 Enable hard disk interrupt bit 4 = 0 Enable serial port 1 interrupt bit 3 = 0 Enable serial port 2 interrupt bit 2 = 0 Enable video interrupt bit 1 = 0 Enable kybd/pointing device/RTC interrupt bit 0 = 0 Enable interrupt timer
0021h	W	PIC OWC2 (if bits 4-3 = 0) bit 7 = Reserved bits 6-5 = 000 Rotate in automatic EOI mode (clear) 001 Nonspecific EOI 010 No operation 011 Specific EOI 100 Rotate in automatic EOI mode (set) 101 Rotate on nonspecific EOI command 110 Set priority command 111 Rotate on specific EOI command bits 4-3 = Reserved (should be 00) bits 2-0 = Interrupt request to which the command applies
0020h	R	PIC interrupt request and in-service registers programmed by OCW3 **Interrupt request register** bits 7-0 = 0 No active request for the corresponding interrupt line 1 Active request for the corresponding interrupt line **Interrupt in-service register** bits 7-0 = 0 Corresponding interrupt line not currently being serviced 1 Corresponding interrupt line is currently being serviced
0021h	W	PIC OCW3 (if bit 4 = 0, bit 3 = 1) bit 7 = Reserved (should 0) bits 6-5 = 00 No operation 01 No operation 10 Reset special mask 11 Set special mask bit 4 = Reserved (should be 0) bit = Reserved (should be 1) bit 2 = 0 No poll command 1 Poll command bits 1-0 = 00 No operation 01 Operation 10 Read interrupt request register on next read at port 0020 h 11 Read interrupt in-service register on next read at port 0020h

Continued...

I/O Address	Read/Write Status	Description
0022h	R / W	Chipsset Register Adress
0023h	R / W	Chipsset Register Data
0040h	R / W	Programmable Interrupt Time read/write counter 0, keyboard controller channel 0
0041h	R / W	Programmer Interrupt Timer channel 1
0042h	R / W	Programmable Interrupt Timer miscellaneous register channel 2
0043h	W	Programmable Interrupt Timer mode port - control word register for counters 0 and 2 bits 7-0 = Counter select 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select bits 5-4 = 00 Counter latch command 01 R / W counter, bits 0-7 only 10 R / W counter, bits 8-15 only 11 R / W counter, bits 0-7 first, then bits 8-15 bits 3-1 = Select mode 000 Mode 0 001 Mode 1 programmable one shot x10 Mode 2 rate generator x11 Mode 3 square wave generator 100 Mode 4 software-triggered strobe 101 Mode 5 hardware-triggered strobe bit 0 = 0 Binary counter is 16 bits 1 Binary counter decimal (BCD) counter
0048h	R / W	Programmable interrupt timer
0060h	R	Keyboard controller data port or keyboard input buffer
0060h	W	Keyboard or keyboard controller data output buffer

Continued...

I/O Address	Read/Write Status	Description
0064h	R	Keyboard controller read status bit 7 = 0 No parity error 1 Parity error on keyboard transmission bit 6 = 0 No timeout 1 Received timeout bit 5 = 0 No timeout 1 Keyboard transmission timeout bit 4 = 0 Keyboard inhibited 1 Keyboard not inhibited bit 3 = 0 Data 1 Command bit 2 = System flag status bit 1 = 0 Input buffer empty 1 Input buffer full bit 0 = 0 Output buffer empty 1 Output buffer full
0064h	W	Keyboard controller input buffer
0070h	R	CMOS RAM index register port and NMI mask bit 7 = 1 NMI disabled bits 6-0 = 0 CMOS RAM index
0071h	R / W	CMOS RAM data register port
0080h	R / W	Temporary storage for additional page register
0080h	R	Manufacturing diagnostic port (this port can access POST checkpoints)
0081h	R / W	DMA channel 2 address byte 2
0082h	R / W	DMA channel 2 address byte 2
0083h	R / W	DMA channel 1 address byte 2
0084h	R / W	Extra DMA page register
0085h	R / W	Extra DMA page register
0086h	R / W	Extra DMA page register
0087h	R / W	DMA channel 0 address byte 2
0088h	R / W	Extra DMA page register
0089h	R / W	DMA channel 6 address byte 2
008Ah	R / W	DMA channel 7 address byte 2
008Bh	R / W	DMA channel 5 address byte 2
008Ch	R / W	Extra DMA page register
008Dh	R / W	Extra DMA page register
008Eh	R / W	Extra DMA page register
008Fh	R / W	DMA refresh page register

Continued...

I/O Address	Read/Write Status	Description
00A0h - 00A1h are reserved for the slave programmable interrupt controller. The bit definitions are identical to those of addresses 0020h - 0021h except where indicated.		
00A0h	R / W	Programmable interrupt controller 2
00A1h	R / W	Programmable interrupt controller 2 mask bit 7 = 0 Reserved bit 6 = 0 Enable hard disk interrupt bit 5 = 0 Enable coprocessor execution interrupt bit 4 = 0 Enable mouse interrupt bits 3-2 = 0 Reserved bit 1 = 0 Enable redirect cascade bit 0 = 0 Enable real time clock interrupt
00C0h	R / W	DMA channel 4 memory address bytes 1 and 0 (low)
00C2h	R / W	DMA channel 4 transfer count bytes 1 and 0 (low)
00C4h	R / W	DMA channel 5 memory address bytes 1 and 0 (low)
00C6h	R / W	DMA channel 5 transfer count bytes 1 and 0 (low)
00C8h	R / W	DMA channel 6 memory address bytes 1 and 0 (low)
00CAh	R / W	DMA channel 6 transfer count bytes 1 and 0 (low)
00CCh	R / W	DMA channel 7 memory address bytes 1 and 0 (low)
00CEh	R / W	DMA channel 7 transfer count bytes 1 and 0 (low)
00D0h	R	Status register for DMA channels 4-7 bit 7 = 1 Channel 7 request bit 6 = 1 Channel 6 request bit 5 = 1 Channel 5 request bit 4 = 1 Channel 4 request bit 3 = 1 Terminal count on channel 7 bit 2 = 1 Terminal count on channel 6 bit 1 = 1 Terminal count on channel 5 bit 0 = 1 Terminal count on channel 4
00D0h	W	Command register for DMA channels 4-7 bit 7 = 0 DACK sense active low 1 DACK sense active high bit 6 = 0 DREQ sense active low 1 DREQ sense active high bit 5 = 0 Late write selection 1 Extended write selection bit 4 = 0 Fixed Priority 1 Rotating Priority bit 3 = 0 Normal Timing 1 Rotating Timing bit 2 = 0 Enable controller 1 Disable controller bit 1 = 0 Disable memory-to-memory transfer 1 Enable memory-to-memory transfer bit 0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
00D2h	W	Write request register for DMA channels 4-7
00D4h	W	Write single mask register bit for DMA channels 4-7 bits 7-3 = 0 Reserved bit 2 = 0 Clear mask bit, 1 Set mask bit bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D6h	W	Mode register for DMA channels 4-7 bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	W	Clear byte pointer flip/flop for DMA channels 4-7
00DAh	R	Read Temporary Register for DMA channels 4-7
00DAh	W	Master Clear for DMA channels 4-7
00DCh	W	Clear mask register for DMA channels 4-7
00DEh	W	Write mask register for DMA channels 4-7
00F0h	W	Math coprocessor clear busy latch
00F1h	W	Math coprocessor reset
00F2h - 00FFh	R / W	Math coprocessor
I/O addresses 0170h - 0177h are reserved for use with a secondary hard drive. See addresses 01F0h - 01F7h for bit definitions.		
0170h	R / W	Data register for hard drive 1
0171h	R	Error register for hard drive 1
0171h	W	Precomposition register for hard drive 1
0172h	R / W	Sector count - hard drive 1

Continued...

I/O Address	Read/Write Status	Description
0173h	R / W	Sector number for hard disk 1
0174h	R / W	Number of cylinders (low byte) for hard drive 1
0175h	R / W	Number of cylinders (high byte) for hard drive 1
0716h	R / W	Drive/head register for hard drive 1
0177h	R	Status register for hard drive 1
0177h	W	Command register for hard drive 1
01F0h	R / W	Data register base port for hard drive 0
01F1h	R	Error register for hard drive 0 **Diagnostic mode** bits 7-3 = Reserved bits 2-0 = Errors 0001 No errors 0010 Controller error 0011 Sector buffer error 0100 ECC device error 0101 Control processor error **Operation mode** bit 7 = Block 0 Bad block 1 Block not bad bit 6 = Error 0 No error 1 Uncorrectable ECC error bit 5 = Reserved bit 4 = ID 0 ID located 1 ID not located bit 3 = Reserved bit 2 = Command 0 Completed 1 Not completed bit 1 = Track 000 0 Not found 1 Found bit 0 = DRAM 0 Not found 1 Found (CP-3022 always 0)
01F1h	W	Write precomposition register for hard drive 0
01F2h	R / W	Sector count for hard disk 0
01F3h	R / W	Sector number for hard drive 0
01F4h	R / W	Number of cylinders (low byte) for hard drive 0
01F5h	R / W	Number of cylinders (high byte) for hard drive 0

Continued...

I/O Address	Read/Write Status	Description
01F6h	R / W	Drive/Head register for hard drive 0 bit 7 = 1 bit 6 = 0 bit 5 = 1 bit 4 = Drive select 0 First hard drive 1 Second hard drive bits 3-0 = Head select bits
01F7h	R	Status register for hard drive 0 bit 7 = 1 Controller is executing a command bit 6 = 1 Drive is ready bit 5 = 1 Write fault bit 4 = 1 Seek operation complete bit 3 = 1 Sector buffer requires servicing bit 2 = 1 Disk data read completed successfully bit 1 = Index (is set to 1 at each disk revolution) bit 0 = 1 Previous command ended with error
01F7h	W	Command register for hard drive 0
0200h - 020Fh	R / W	Game controller ports
0201h	R / W	I/O data - game port
0220h – 022Fh	R / W	Soundport AD1816 reserved
I/O addresses 0278h - 027Ah are reserved for use with parallel port 2. See the bit definitions for addresses 0378h - 037Ah.		
0278h	R / W	Data port for parallel port 2
0279h	R	Status port for parallel port 2
0279h	W	PnP Adress register (only for PnP devices)
027Ah	R / W	Control port for parallel port 2
02B0h	R / W	Digital I/O reserved
I/O addresses 02E8h - 02EFh are reserved for use with serial port 4. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02E8h	W	Transmitter holding register for serial port 4
02E8h	R	Receive buffer register for serial port 4
02E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02E9h	R / W	Interrupt enable register when DLAB = 0
02EAh	R	Interrupt identification register for serial port 4
02EBh	R / W	Line control register for serial port 4
02ECh	R / W	Modem control register for serial port 4
02EDh	R	Line status register for serial port 4
02EEh	R	Modem status register for serial port 4
02EFh	R / W	Scratch register for serial port 4 (used for diagnostics)

Continued...

I/O Address	Read/Write Status	Description
I/O addresses 02F8h - 02FFh are reserved for use with serial port 2. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02F8h	W	Transmitter holding register for serial port 2
02F8h	R	Receive buffer register for serial port 2
02F8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02F9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02F9h	R / W	Interrupt enable register when DLAB = 0
02FAh	R	Interrupt identification register for serial port 2
02FBh	R / W	Line control register for serial port 2
02FCh	R / W	Modem control register for serial port 2
02FDh	R	Line status register for serial port 2
02FEh	R	Modem status register for serial port 2
02FFh	R / W	Scratch register for serial port 2 (used for diagnostics)
0300h – 031Fh	R / W	LAN controller reserved
I/O addresses 0372h - 0377h are reserved for use with a secondary diskette controller. See the bit definitions for 03F2h - 03F7h.		
0372h	W	Digital output register for secondary diskette drive controller
0374h	R	Status register for secondary diskette drive controller
0375h	R / W	Data register for secondary diskette drive controller
0376h	R / W	Control register for secondary diskette drive controller
0377h	R	Digital input register for secondary diskette drive controller
0377h	W	Select register for secondary diskette data transfer rate
0378h	R / W	Data port for parallel port 1
0379h	R	Status port for parallel port 1 bit 7 = 0 Busy bit 6 = 0 Acknowledge bit 5 = 1 Out of paper bit 4 = 1 Printer is selected bit 3 = 0 Error bit 2 = 0 IRQ has occurred bit 1-0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
037Ah	R / W	Control port for parallel port 1 bits 7-5 = Reserved bit 4 = 1 Enable IRQ bit 3 = 1 Select printer bit 2 = 0 Initialize printer bit 1 = 1 Automatic line feed bit 0 = 1 Strobe
03B0h - 03B8h	R / W	Various video registers
I/O addresses 03BCh - 03BEh are reserved for use with parallel port 3. See the bit definitions for addresses 0378h - 037Ah.		
03BCh	R / W	Data port - parallel port 3
03BDh	R / W	Status port - parallel port 3
03BEh	R / W	Control port - parallel port 3
03C0h - 03CFh	R / W	Video subsystem (EGA/VGA)
03C2h - 03D9h	R / W	Various CGA and CRTC registers
03E0h	R / W	PCCARD Adress select
03E1h	R / W	PCCARD Data transfer with 365SL controller
I/O addresses 03E8h - 03EFh are reserved for use with serial port 3. See the bit definitions for I/O addresses 03F8h - 03FFh.		
03E8h	W	Transmitter holding register for serial port 3
03E8h	R	Receive buffer register for serial port 3
03E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
03E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
03E9h	R / W	Interrupt enable register when DLAB = 0
03EAh	R	Interrupt identification register for serial port 3
03EBh	R / W	Line control register for serial port 3
03ECh	R / W	Modem control register for serial port 3
03EDh	R	Line status register for serial port 3
03EEh	R	Modem status register for serial port 3
03EFh	R / W	Scratch register for serial port 3 (used for diagnostics)
03F2h	W	Digital output register for primary diskette drive controller bits 7-6 = 0 Reserved bit 5 = 1 Enable drive 1 motor bit 4 = 1 Enable drive 0 motor bit 3 = 1 Enable diskette DMA bit 2 = 0 Reset controller bit 1 = 0 Reserved bit 0 = 0 Select drive 0 1 Select drive 1

Continued...

I/O Address	Read/Write Status	Description
03F4h	R	Status register for primary diskette drive controller bit 7 = 1 Data register is ready bit 6 = 0 Transfer from system to controller 1 Transfer from controller to system bit 5 = 1 Non-DMA mode bit 4 = 1 Diskette drive controller is busy bits 3-2 = Reserved bit 1 = 1 Drive 1 is busy bit 0 = 1 Drive 0 is busy
03F5h	R / W	Data register for primary diskette drive controller
03F6h	R	Control port for primary diskette drive controller bits 7-4 = Reserved bit 3 = 0 Reduce write current 1 Head select enable bit 2 = 0 Disable diskette drive reset 1 Enable diskette drive reset bit 1 = 0 Disable diskette drive initialization 1 Enable diskette drive initialization bit 0 = Reserved
03F7h	R	Digital input register for primary diskette drive controller bit 7 = 1 Diskette drive line change bit 6 = 1 Write gate bit 5 = Head select 3 / reduced write current bit 4 = Head select 2 bit 3 = Head select 1 bit 2 = Head select 0 bit 1 = Drive 1 select bit 0 = Drive 0 select
03F7h	W	Select register for primary diskette data transfer rate bits 7-2 = Reserved bits 1-0 = 00 500 Kbs mode 01 300 Kbs mode 10 250 Kbs mode 11 Reserved
I/O addresses 03F8h - 03FFh are reserved for use with serial port 1. The bit definitions for these addresses also apply to serial ports 2, 3, and 4.		
03F8h	W	Transmitter holding register for serial port 1 - Contains the character to be sent. Bit 0, the least significant bit, is the first bit sent. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0
03F8h	R	Receive buffer register for serial port 1 - Contains the character to be received. Bit 0, the least significant bit, is the first bit received. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0

Continued...

I/O Address	Read/Write Status	Description
03F8h	R / W	Baud rate divisor (low byte) - This byte along with the high byte (03F9h) store the data transmission rate divisor. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 1
03F9h	R / W	Baud rate divisor (high byte) - This byte along with the low byte (03F8h) store the data transmission rate divisor. bits 7-0 = Bits 8-15 when DLAB = 1
03F9h	R / W	Interrupt enable register bits 7-4 = Reserved bit 3 = 1 Modem status interrupt enable bit 2 = 1 Receiver line status interrupt enable bit 1 = 1 Transmitter holding register empty interrupt enable bit 0 = 1 Received data available interrupt enable when DLAB = 0
03FAh	R	Interrupt identification register - serial port 1 bits 7-3 = Reserved bits 2-1 = Identify interrupt with highest priority 00 Modem status interrupt (4th priority) 01 Transmitter holding register empty (3rd priority) 10 Received data available (2nd priority) 11 Receiver line status interrupt (1st priority) bit 0 = 0 Interrupt pending (register contents can be used as a pointer to interrupt service routine) 1 No interrupt pending
03FBh	R / W	Line control register - serial port 1 bit 7 = Divisor Latch Access (DLAB) 0 Access receiver buffer, transmitter holding register, and interrupt enable register 1 Access divisor latch bit 6 = 1 Set break enable. Forces serial output to spacing state and remains there bit 5 = Stick parity bit 4 = Even parity select bit 3 = Parity enable bit 2 = Number of stop bits bit 1 = Word length 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	R / W	Modem control register - serial port 1 bits 7-5 = Reserved bit 4 = 1 Loopback mode for diagnostic testing of serial port. bit 3 = 1 User-defined output 2 bit 2 = 1 User-defined output 1 bit 1 = Force Request To Send active bit 0 = Force Data Terminal Ready active

Continued...

I/O Address	Read/Write Status	Description
03FDh	R	Line status register - serial port 1 bit 7 = Reserved bit 6 = 1 Transmitting shift and holding registers empty bit 5 = 1 Transmitter shift register empty bit 4 = 1 Break interrupt bit 3 = 1 Framing error bit 2 = 1 Overrun error bit 0 = 1 Data ready
03FEh	R	Modem status register - serial port 1 bit 7 = 1 Data Carrier Detect bit 6 = 1 Ring Indicator bit 5 = 1 Data Set Ready bit 4 = 1 Clear To Send bit 3 = 1 Delta Data Carrier bit 2 = 1 Trailing Edge Ring Indicator bit 1 = 1 Delta Data Set Ready bit 0 = 1 Delta Clear To Send
03FFh	R / W	Scratch register - serial port 1 (used for diagnostics)
0A79h	W	PnP Data write register (only for PnP devices)

4.8.2 BIOS-Variable-Segment

The BIOS Data Area is an area within system RAM that contains information about the system environment. System environment information includes definitions associated with hard disks, diskette drives, keyboard, video, as well as other BIOS functions. This area is created when the system is first powered on. It occupies a 256-byte area from 0400h - 04FFh. The following table lists the contents of the BIOS data area locations in offset order starting from segment address 40:00h.

BIOS Data Area Definitions

Location	Description
00h - 07h	I/O addresses for up to 4 serial ports
08h - 0Dh	I/O addresses for up to 3 parallel ports
0Eh - 0Fh	Segment address of extended data address
10h - 11h	Equipment list bits 15-14 = Number of parallel printer adapters 00 = Not installed 01 = One 10 = Two 11 = Three bits 13-12 = Reserved bits 11-9 = Number of serial adapters 00 = Not installed 001 = One 010 = Two 011 = Three 100 = Four bit 8 = Reserved bits 7-6 = Number of diskette drives 00 = One drive 01 = Two drives bits 5-4 = Initial video mode 00 = EGA or PGA 01 = 40 x 25 color 10 = 80 x 25 color 11 = 80 x 25 monochrome bit 3 = Reserved bit 2 = (1) Pointing device present bit 1 = (1) Math coprocessor present bit 0 = (1) Diskette drive present
12h	Reserved for port testing by manufacturer bits 7-1 = Reserved bit 0 = (0) Non-test mode (1) Test mode
13h	Memory size in kilobytes - low byte
14h	Memory size in kilobytes - high byte

Continued...

BIOS Data Area Definitions Continued...

Location	Description
15h - 16h	Reserved
17h	Keyboard Shift Qualifier States bit 7 = Insert mode bit 6 = CAPS lock bit 5 = Numlock bit 4 = Scroll Lock bit 3 = Either Alt key bit 2 = Either control key bit 1 = Left Shift key bit 0 = Right shift key 0 = not set / 1 = set
18h	Keyboard Toggle Key States bit 7 = (1) Insert held down bit 6 = (1) CAPS lock held down bit 5 = (1) Num Lock held down bit 4 = (1) Scroll Lock held down bit 3 = (1) Control+Num Lock held down bit 2 = (1) Sys Re held down bit 1 = (1) Left Alt held down bit 0 = (1) Left Control held down
19h	Scratch area for input from Alt key and numeric keypad
1Ah - 1Bh	Pointer to next character in keyboard buffer
1Ch - 1Dh	Pointer to last character in keyboard buffer
1Eh - 3Dh	Keyboard Buffer. Consists of 16 word entries.
3Eh	Diskette Drive Recalibration Flag bit 7 = (1) Diskette hardware interrupt occurred bits 6-4 = Not used bits 3-2 = Reserved bit 1 = (0) Recalibrate drive B bit 0 = (0) Recalibrate drive A

Continued...

BIOS Data Area Definitions Continued...

Location	Description
3Fh	Diskette Drive Motor Status bit 7 = Current operation 0 = Write or Format 1 = Read or Verify bit 6 = Reserved bits 5-4 = Drive Select 00 = Drive A 01 = Drive B bits 3-2 = Reserved 0 = Disable 1 = Enabled bit 1 = Drive B Motor Status 0 = Off 1 = On bit 1 = Drive A Motor Status 0 = Off 1 = On
40h	Diskette Drive Motor Timeout Disk drive motor is powered off when the value via the INT 08h timer interrupt reaches 0.
41h	Diskette Drive Status bit 7 = Drive Ready 0 = Ready 1 = Not ready bit 6 = Seek Error 0 = No error 1= Error occurred bit 5 = Controller operation 0 = Working 1 = Failed bits 4-0 = Error Codes 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 06h = Diskette change line active (door opened) 08h = DMA overrun error 09h = Data boundary error 0Ch = Unknown media type 10h = ECC or CRC error 20h = Controller failure 40h = Seek operation failure 80h = Timeout
42h - 48h	Diskette Controller Status Bytes
49h	Video Mode Setting
4Ah - 4Bh	Number of Columns on screen
4Ch - 4Dh	Size of Current Page, in bytes
4Eh - 4Fh	Address of Current Page

Continued...

BIOS Data Area Definitions Continued...

Location	Description
50h - 5Fh	Position of cursor for each video page. Current cursor position is stored two bytes per page. First byte specifies the column, the second byte specifies the row.
60h - 61h	Start and end lines for 6845-compatible cursor type. 60h = starting scan line, 61h = ending scan line.
62h	Current Video Display Page
63h - 64h	6845-compatible I/O port address for current mode 3B4h = Monochrome 3D4h = Color
65h	Register for current mode select
66h	Current palette setting
67 - 6Ah	Address of adapter ROM
6Bh	Last interrupt the occurred
6Ch - 6Dh	Low word of timer count
6Eh - 6Fh	High word of timer count
70h	Timer count for 24-hour rollover flag
71h	Break key flag
72h - 73h	Reset flag 1243h = Soft reset. Memory test is bypassed.
74h	Status of last hard disk operation 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 05h = Reset failed 08h = DMA overrun error 09h = Data boundary error 0Ah = Bad sector flag selected 0Bh = Bad track detected 0Dh = Invalid number of sectors on format 0Eh = Control data address mark detected 0Fh = DMA arbitration level out of range 10h = ECC or CRC error 11h = Data error corrected by ECC 20h = Controller failure 40h = Seek operation failure 80h = Timeout AAh = Drive not ready BBh = Undefined error occurred CCh = Write fault on selected drive E0h = Status error or error register = 0 FFh = Sense operation failed
75h	Number of hard drives
76h - 77h	Work area for hard disk

Continued...

BIOS Data Area Definitions Continued...

Location	Description
78h - 7Bh	Default parallel port timeout values
7Dh - 7Fh	Default serial port timeout values
80h - 81h	Pointer to start of keyboard buffer
82h - 83h	Pointer to end of keyboard buffer
84h - 88h	Reserved for EGA/VGA BIOS
8Ah	Reserved
8Bh	Diskette drive data transfer rate information bits 7-5 = Data rate on last operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 5-4 = Last drive step rate selected bits 3-2 = Data transfer rate at start of operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 1-0 = Reserved
8Ch	Copy of hard status register
8Dh	Copy of hard drive error register
8Eh	Hard drive interrupt flag
8Fh	Diskette controller information bit 7 = Reserved bit 6 = (1) Drive confirmed for drive B bit 5 = (1) Drive B is multi-rate bit 4 = (1) Drive B supports line change bit 3 = Reserved bit 2 = (1) Drive determined for drive A bit 1 = (1) Drive B is multi-rate bit 0 = (1) Drive B supports line change
90h - 91h	Media type for drives bits 7-6 = Data transfer rate 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bit 5 = (1) Double stepping required when 360K diskette inserted into 1.2MB drive bit 4 = (1) Known media is in drive bit 3 = Reserved bits 2-0 = Definitions upon return to user applications 000 = Testing 360K in 360K drive 001 = Testing 360K in 1.2 MB drive 010 = Testing 1.2 MB in 1.2 MB drive 011 = Confirmed 360K in 360K drive 100 = Confirmed 360K in 1.2 MB 101 = Confirmed 1.2 MB in 1.2 MB drive 111 = 720K in 720K drive or 1.44 MB in 1.44 MB drive

Continued...

BIOS Data Area Definitions Continued...

Location	Description
92h - 93h	Scratch area for diskette media. Low byte for drive A, high byte for drive B.
94h - 95h	Current track number for both drives. Low byte for drive A, high byte for drive B.
96h	Keyboard Status bit 7 = (1) Read ID bit 6 = (1) Last code was first ID bit 5 = (1) Force to Num Lock after read ID bit 4 = (1) Enhanced keyboard installed bit 3 = (1) Right ALT key active bit 2 = (1) Right Control key active bit 1 = (1) Last code was E0h bit 0 = (1) Last code was E1h
97h	Keyboard Status bit 7 = (1) Keyboard error bit 6 = (1) Updating LEDs bit 5 = (1) Resend code received bit 4 = (1) Acknowledge received bit 3 = Reserved bit 2 = (1) Caps lock LED state bit 1 = (1) Num lock LED state bit 0 = (1) Scroll lock LED state
98h - 99h	Offset address of user wait flag
9Ah - 9Bh	Segment address of user wait flag
9Ch - 9Dh	Wait count, in microseconds (low word)
9Eh - 9Fh	Wait count, in microseconds (high word)
A0h	Wait active flag bit 7 = (1) Time has elapsed bits 6-1 = Reserved bit 0 = (1) INT 15h, AH = 86h occurred
A1h - A7h	Reserved
A8h - ABh	Pointer to video parameters and overrides
ACh - FFh	Reserved
100h	Print screen status byte

4.8.2.1 Compatibility Service Table

In order to ensure compatibility with industry-standard memory locations for interrupt service routines and miscellaneous tabular data, the BIOS maintains tables and jump vectors.

Location	Description
FE05Bh	Entry Point for POST
FE2C3h	Entry point for INT 02h (NMI service routine)
FE3FEh	Entry point for INT 13h (Diskette Drive Services)
FE401h	Hard Drive Parameters Table
FE6F1h	Entry point for INT 19h (Bootstrap Loader routine)
FE6F5h	System Configuration Table
FE739h	Entry point for INT 14h (Serial Communications)
FE82Eh	Entry point for INT 16h (Keyboard Services)
FE897h	Entry point for INT 09h (Keyboard Services)
FEC59h	Entry point for INT 13h (Diskette Drive Services)
FEF57h	Entry point for INT OEh (Diskette Hardware Interrupt)
FEFC7h	Diskette Drive Parameters Table
FEFD2h	Entry point for INT 17h (Parallel Printer Services)
FF065h	Entry point for INT 10h (CGA Video Services)
FF0A4h	Video Parameter Table (6845 Data Table - CGA)
FF841h	Entry point for INT 12h (Memory Size Service)
FF84Dh	Entry point for INT 11h (Equipment List Service)
FF859h	Entry point for INT 15h (System Services)
Location	**Description**
FFA6Eh	Video graphics and text mode tables
FFE6Eh	Entry point for INT 1Ah (Time-of-Day Service)
FFEA5h	Entry Point for INT 08h (System Timer Service)
FFEF3h	Vector offset table loaded by POST
FFF53h	Dummy Interrupt routine IRET Instruction
FFF54h	Entry point for INT 05h (Print Screen Service)
FFFF0h	Entry point for Power-on
FFFF5h	BIOS Build Date (in ASCII)
FFFFEh	BIOS ID

4.8.2.2 System Configuration Parameter Table

The System Configuration Parameter Table located at F000:E6F5h contains basic configuration information about the computer. This table can be copied to system RAM by using INT 15h function C0h "Return System Configuration Parameters".

Location	Description
00h - 01h	Table Length (from next entry)
02h	System Model 0FCH = AT, Model 50, Model 60 0F8H = Model 80, Model 70 0FAH = Model 30, Model 25
03h	System Sub-Model Byte 00h = Model 80 or AT 01h = Model 80 or AT FFh = Unknown
04h	BIOS Version
05h	System Facilities bit 7 = DMA Channel 3 used by BIOS bit 6 = Slave int. PIC. available bit 5 = Real time clock available bit 4 = Keyboard scan code hook 1AH bit 3 = Wait for external event supported bit 2 = Extended data area available if set bit 1 = MicroChannel bus installed if set bit 0 = Unused
06h	Reserved (should be zeros)
07h	Reserved (should be zeros)
08h	Reserved (should be zeros)
09h	Reserved (should be zeros)

4.9 VGA (only on MSM386SV Boards)

The 65540 High Performance Flatpanel/CRT VGA controller

- High integrated design (flatpanel/CRT VGA controller, RAMDAC, clock synthesizer)
- Local Bus (32 Bit CPU)
- Flexible display memory configurations
  - One 256Kx16 DRAM (512 KB)
- Advanced frame buffer architecture uses available display memory, maximizing integration and minimizing chip count
- Integrated programmable linear address feature accelerates GUI performance
- Hardware windows acceleration (65545)
  - 32-Bit graphics engine
    - System-to-screen and screen-to-screen BitBlt
    - Color expansion
    - Optimized for Windows™ BitBlt format
  - Hardware line drawing
  - 64x64x2 hardware cursor
- Hardware pop-up icon (65545)
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- High performance resulting from zero wait-state writes (write buffer) and minimum wait-state reads (internal asynchronous FIFO design)
- Mixed 3.3 V / 5.0 V +/- 10 % Operation
- Interface to CHIPS' PC Video to display "live" video on flatpanel displays
- Supports panel resolutions up to 1280 x 1024, including 800x600 and 1024x768
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768 / 256 colors
- True-color and Hi-color display capability with flatpanels and CRT monitors up to 640x480 resolution
- Direct interface to Color and Monochrome Dual Drive (DD) and Single Drive (SS) panels (supports 8, 9, 12, 15, 16, 18 and 24-Bit data interfaces)
- Advanced power management features minimize power consumption during:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- Flexible onboard Activity Timer facilitates ordered shut-down of the display system
- Power Sequencing control outputs regulate application of Bias voltage, +5 V to the panel and +12 V to the inverter for backlight operation
- SMARTMAP™ intelligent color to gray scale conversion enhances text legibility
- Text enhancement feature improves white text contrast on flatpanel displays
- Fully Compatible with IBM™ VGA

65540/545 Display Capabilities

CRT Mode Resolution	Color [4]	Mono LCD Gray Scales [4]	DD STN LCD Colors [2, 3, 4]	9-Bit TFT LCD Colors [1, 2, 3, 4]	Video Memory	Simultaneous Display
320x200	256 /256K♦	61 / 61	256 / 226,981	256 / 185,193	512 KB	yes
640x480	16 / 256K♦	16 / 61	16 / 226,981	16 / 185,193	512 KB	yes
640x480	256 / 256K♦	61 / 61	256 / 226,981	256 / 185,193	512 KB	yes
800x600	16 / 256K♦	16 / 61	16 / 226,981	16 / 185,193	512 KB	yes with 1 MB
800x600	256 / 256K♦	61 / 61	256 / 226,981	256 / 185,193	512 KB	yes with 1 MB
1024x768	16 / 256K♦	16 / 61	16 / 226,981	16 / 185,193	512 KB	yes with 1 MB
1024x768	256 / 256K♦	61 / 61	256 / 226,981	256 / 185,193	1 MB	yes
1280x1024	16 / 256K♦	16 / 61	n/a	n/a	1 MB	n/a

Notes:

1 Larger color palettes and simultaneous colors can be displayed on 12-Bit, 18-Bit, and 24-Bit TFT panels via the 65540/545 video input port.
2 Includes dithering.
3 Includes frame rate control.
4 Colors are described as number of simultaneous on-screen colors and number of unique colors available in the color palette. 256K colors assumes DAC output mode is set to 6 bits of R, G & B. If DAC is set to 8-Bit output mode, the number of available colors is 16 M.

VGA Controller Chips

C&T	65540	16Bit local bus	1024k RAM	
C&T	65545	16Bit local bus	1024k RAM	hardware accelerator

All controllers are software and register compatible. The 65540 to 65545 are pin compatible and may be exchanged onboard.

CRT Displays

The 65540/45A supports resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. Digital monitor support is also built in.

Supported VGA Modes

Mode:	Type:	Colors:	CRT:	Text:	Graphic:	DRAM:	Monitor:	Refresh/HR:
0,1	Text	16	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
2,3	Text	16	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
4,5	Graphic	4	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
6	Graphic	2	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
7+	Text	Mono	ABC	80 x 25	720 x 350	256k	HGC	70 Hz
D	Planar	16	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
E	Planar	16	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
F	Planar	Mono	ABC	80 x 25	640 x 350	256k	EGA	70 Hz
10	Planar	16	ABC	80 x 25	640 x 350	256k	EGA	70 Hz
11	Planar	2	ABC	80 x 30	640 x 480	256k	VGA	60 Hz
12/12+	Planar	16	ABC/BC	80 x 30	640 x 480	256k	VGA	60 Hz/72Hz
13	Planar	256	ABC	40 x 25	320 x 200	256k	CGA	70 Hz (not 8 Bit Bus)
20	4 Bit Lin	16	ABC	80 x 30	640 x 480	512k	VGA	60 Hz
22	4 Bit Lin	16	BC	100 x 37	800 x 600	512k	SVGA	60 Hz
30	8 Bit Lin	256	ABC	80 x 30	640 x 480	512k	VGA	60 Hz/72 Hz
32	8 Bit Lin	256	BC	100 x 37	800 x 600	512k	SVGA	60 Hz/72 Hz
60	Text	16	ABC	132 x 25	1056 x 400	256k	MGA	68 Hz
61	Text	16	ABC	132 x 50	1056 x 400	256k	MGA	68 Hz
72	Planar	16	C	128 x 48	1024 x 768	512k	HVGA	60 Hz
79	Packed	256	ABC	80 x 30	640 x 480	512k	VGA	72 Hz
7C	Packed	256	BC	100 x 37	800 x 600	512k	SVGA	72 Hz

Supported on MSM386SV boards with 1024k Video-RAM

24	4 Bit Lin	16	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz
26	4 Bit Lin	16	BC	128 x 48	1024 x 768	1024k	HiVGA	43 Hz
34	8 Bit Lin	256	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz
36	8 Bit Lin	256	BC	128 x 48	1024 x 768	1024k	HiVGA	43 Hz
40	15 Bit Lin	32k	ABC	80 x 30	640 x 480	1024k	VGA	60 Hz
41	16 Bit Lin	64k	ABC	80 x 30	640 x 480	1024k	VGA	60 Hz
7E	Packed	256	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz

A = PS/2 fixed frequency analog monitor;
B = Multifrequency CRT monitor like NEC Multisynch 3D or eq.
C = Nanao/EIZO 9070, NEC Multisynch 5D, or eq.

4.9.1 VGA/LCD BIOS Support

Each LCD display needs a specific adapted VGA BIOS.
This product is standardly equipped with the CRT standard VGA BIOS.

To connect an LCD Display to this product, you have to follow these steps:

1. Check the VGABIOS.DOC if the LCD BIOS is available.
   To receive the latest VGA BIOS refer to our webpage www.digitallogic.com .

If the LCD is available:

2. In the FLATPANEL-SUPPORT documentation will describe the connection between the LCD and this product.

3. DOWNLOAD the corresponding LCD BIOS with the utility DOWN.EXE.
   Go to the section **Fehler! Verweisquelle konnte nicht gefunden werden.**

4. Restart the system and check the VGA BIOS header message. The LCD name must be visible for only a short time. The VGA BIOS message appears as first info page on the screen.

5. Stop the system, connect the LCD to the system and restart again.

6. If on the LCD no image appears as soon as the monitor begins to show the first text, stop the system immediately, otherways the LCD will be damaged!

7. Check the LCD connection again.

For a new LCD type, not yet available:

If the LCD BIOS for your LCD is not available, DIGITAL-LOGIC AG will adapt the LCD and provide you with one working cable. To initialize this, we will need the following parts from you:

1. An order to adapt the LCD (for charges ask your sales contact)
2. Send the LCD panel, a datasheet, a connector to the LCD and the inverter for the backlight.

ATTENTION:

DIGITAL-LOGIC AG cannot be held responsible for a damaged LCD display. Even if there is a mistake in the BIOS or in any documentation of the LCD.

4.9.2 Driver Resolutions and File names

Application:	Resolution:	Colors:	65535/65540:	Acce.: 65545/48
Windows 3.1	640 x 480	16	LINEAR4.DRV	VIDGX4.DRV
	800 x 600	16	LINEAR4.DRV	VIDGX4.DRV
	1024 x 768	16	LINEAR4.DRV	VIDGX4.DRV
	1280 x 1024	16	LINEAR4.DRV	VIDGX4.DRV
	640 x 480	256	LINEAR8:DRV	VIDGX8.DRV
	800 x 600	256	LINEAR8.DRV	VIDGX8.DRV
	1024 x 768	256	LINEAR8.DRV	VIDGX8.DRV
	480 x 640 Portrait	16	R12.DRV	
	640 x 480	64K	LINEAR16.DRV	VIDGX16.DRV
	640 x 480	16M	LINEAR24.DRV	VIDGX24.DRV
Windows NT 3.5x	640 x 480	16	chips.dll	
	800 x 600	16		
	1024 x 768	16		
	640 x 480	256		
	800 x 600	256		
Windows NT4.x	640 x 480 - 1024 x 768	16	miniport.dll	
	640 x 480 - 800 x 600	256		
Windows 95	640 x 480 - 1024 x 768	16	chips.dll	
	640 x 480 - 800 x 600	256		
OS/2	640 x 480	256	SV480256.DLL	WV480256.DLL
	800 x 600	256	PD600256.DLL	WV600256.DLL
	1024x768	256	PD768256.DLL	WV768256.DLL
VESA SuperVGA	640 x 480	16 - 64K	VESA.COM	
	800 x 600	16, 256	VESA.COM	
	1024x768	16, 256	VESA.COM	

On the homepage of DIGITAL-LOGIC AG, on www.digitallogic.com you will find the latest VGA drivers.

- 655XXDRI.ZIP

4.9.2.1 Windows

1. Install Windows as you normally would for a VGA display.
2. Place the display driver disk 1 in drive A: and type A: <ENTER > to make this the default drive. Type SETUP, <ENTER> key.
3. Change to the directory where you installed Windows.
4. If you are using Windows V3.0, type MIXFILES <Enter> to add the new drivers to the Windows setup menu.
5. Type SETUP, <Enter> to run the Windows setup program. It will show the current Windows configuration.
6. Follow the directions on the screen to complete the setup.

4.10 Keymatrix

4.10.1 Define a Keymatrix

Start the **EDITMATR.EXE** tool from the tooldisk. This tool enables the assignment of the keymatrix table in the keyboard controller. Start this tool and read the help screen after pressing F1. The following steps must be performed:

1. Press F2 to clear the whole matrix.
2. Connect the keymatrix to the appropriate connector, at the rows and columns.
3. Press on your keymatrix that key, which corresponds with the show key in the blue box.
4. For skipping a key, use the SPACE key on your standard keyboard.
5. Save the table to the key controller to a diskfile **(XXX.MTX).**
6. Exit the program.

Now you should test the operation of the connected keymatrix. Press every key and observe the shown character on the screen.

4.10.2 Store the Keymatrix into the EEPROM

To be sure, that the boot sequence takes the correct values into the key controller, you must store the key controller table after every modification into the EEPROM device.

To do this, use the **SAVEMATR.EXE** toolfile from the tooldisk.

The usage is very simple:

1. Start the SAVEMATR.EXE program.
2. Wait until the program is performed. No parameters are used.

4.10.3 Read DISK-File and store to the EEPROM-Matrix

A previously generated file XXX.MTX (with the aid of EDITMATR.EXE) the EEPROM may be used to reload the EEPROM keymatrix table from the disk. The EEPROM keymatrixtable will be transfered to the 8242PD Keymatrixcontroller while the next booting sequence.

To do this, use the **EDITMATR.EXE** tool from the tooldisk.The usage is very simple:

1. Start the EDITMATR.EXE program and load the XXX.MTX file, e.g. from a diskette
2. Exit from this program
3. Start the **SAVEMATR.EXE** program to store the values into the EEPROM
4. Reboot the system.
5. Alternatively use **EDITMATR.EXE XXX.MTX** to do this action in one rush

4.10.4 Old step by step version for storing the values to another board

Write the EEPROM-Keymatrix to Disk

The keymatrix stored in the EEPROM (with the SAVEMATR.EXE– tool) may be backuped to a diskfile for documentation or reproduction to other boards.

The tool WRMATRIX.EXE writes the contents of the EEPROM Keymatrixtable to the file XMATRIX.DAT.

To do this, use the WRMATRIX.EXE tool from the tooldisk.The usage is very simple:

1. Start the WRMATRIX.EXE program.
2. Wait until the program is performed. No parameters are used.

Read DISK-File and store to the EEPROM-Matrix

A previously generated file XMATRIX.DAT (with the aid of WRMATRIX.EXE) the EEPROM may be used to reload the EEPROM keymatrix table from the disk. The EEPROM keymatrixtable will be transfered to the 8242PD Keymatrixcontroller while the next booting sequence.

To do this, use the RDMATRIX.EXE tool from the tooldisk.The usage is very simple:

1. Be sure that the XMATRIX.DAT file is located on the same path as the RDMATRIX.EXE
2. The XMATRIX.DAT must be prevously generated with the WRMATRIX.EXE tool
3. Start the RDMATRIX.EXE program
4. Wait until the program is performed. No parameters are used
5. Start the RESTMATR.EXE program to store the values into the EEPROM
6. Reboot the system.

4.11 Character LCD Interface

There are two different types of LCD interfaces:

1. Latched I/O LCDs
2. CPU Bus interfaced LCDs

The ELAN board may interface both types, but some jumpers must be modified.

4.11.1 Character LCDs

The command parameters define some variables:

LCD_CHAR.COM [/L] [Z/] [/C] [X/] [/Y] [/T] [/D]

/L	Number of characters per line
/Z	Number of lines per one controller
/C	Number of controller
/D	Format of databus (4 = 4 Bit, 8 = 8 Bit)
/X	First position in the line from DOS-Screen
/Y	First line from DOS-Screen
/T	Wait-Time. How many 1/18 sec cycles waits the system before refreshing the LCD

Ex: LCD_CHAR.COM /L=30 /Z=4 /C=2 /X=0 /Y=10 /T=18

This will install the LCD driver for a display with 2 controllers. Every controller has 4 lines with 30 characters per line. So the LCD-Display is 8 * 30 characters. You will see a window from DOS-screen beginning at line 10 with the first character. The display will be refreshed once per second.

These jumpers must be selected:

No.:	Close:	Function:
J31	1-2	LCDWR on Pin 3
J32	1-2	LCD Enable on Pin 5
J33	1-2	LCD Command/Data Signal on Pin 4
J34	1-2	LCD Latch enable

Address MAP:	Latch for LCD-Dataoutput	=	201h
	Latch for LCD Controllines	=	2B0h

Connector J9:	Pin 1	=	VCC	Supply	
	Pin 2	=	GND	Supply	
	Pin 3	=	LCDW	Write Data strobe line	Bit 0/2B0h
	Pin 4	=	LCDCD	Command/Data select line	Bit 1/2B0h
	Pin 5	=	LCDR	Read Data strobe line	Bit 2/2B0h
	Pin 6	=	LCD D0	Databit 0 (write only)	Bit 0/201h
	Pin 7	=	LCD D1	Databit 1 (write only)	Bit 1/201h
	Pin 8	=	LCD D2	Databit 2 (write only)	Bit 2/201h
	Pin 9	=	LCD D3	Databit 3 (write only)	Bit 3/201h
	Pin 10	=	LCD D4	Databit 4 (write only)	Bit 4/201h
	Pin 11	=	LCD D5	Databit 5 (write only)	Bit 5/201h
	Pin 12	=	LCD D6	Databit 6 (write only)	Bit 6/201h
	Pin 13	=	LCD D7	Databit 7 (write only)	Bit 7/201h

The other signals on the connector are not used by the LCD.

The protocol for the data transfer to the LCD depends on the LCD type. Please refer to the datasheet of the LCD. Ask for a driver support.

Programming example:

Write to the LCD Controllines: OUT 2B0 , al
Write to the LCD data: OUT 201 , al

Read operations are not allowed!

4.11.2 Two 4 Bit Character LCD with the HD44780 Controller

With our LCD_CHAR.COM driver (on the ELAN_UTIL Disk) may be up to two HD44780 based LCD lines controlled. With this driver, the LCD is connected as a 4bit datainterface. The upper 4 databit are used to select the line (for each line a separate HD44780 controller is used).

MSM	Signal	To LCD	Dir.	LM038
1	VCC	1 & 2	out	2
2	GND	1 & 2	out	1
3	nc			
4	nc			
5	nc			
6	LCD_RS	1 & 2	out	5
7	LCD_RW	1 & 2	out	4
8	LCD_E1	1	out	6 LCD1
9	LCD_e2	2	out	6 LCD2
10	LCD_D4	1 & 2	out	11
11	LCD_D5	1 & 2	out	12
12	LCD_D6	1 & 2	out	13
13	LCD_D7	1 & 2	out	14

4.11.3 One 8 Bit Character LCD with the HD44780 Controller

With our LCD_CHAR.COM driver (on the ELAN_UTIL Disk) there may be controlled one HD44780 based LCD line. With this driver, the LCD is connected as a 8Bit data interface.

MSM	Signal	To LCD	Dir.	LM038
1	VCC	1	out	2
2	GND	1	out	1
3	LCD_RW		out	5
4	LCD_CD		out	4
5	LCD_E		out	6
6	LCD_D0	1	out	7
7	LCD_D1	1	out	8
8	LCD_D2	1	out	9
9	LCD_D3	1	out	10
10	LCD_D4	1	out	11
11	LCD_D5	1	out	12
12	LCD_D6	1	out	13
13	LCD_D7	1	out	14

LCD_RW Read/Write (1= read from LCD, 0= write to LCD)
LCD_CD Register select of the LCD (1=Command, 0=Data)
LCD_E Enable (Data is written at the fall of E, Data can be read while E=1)

4.11.4 CPU Bus interfaced DOT-Matrix LCDs

These jumpers must be selected:

No.:	Close:	Function:
J31	2-3	-IOW on Pin 3
J32	2-3	-IOR on Pin 5
J33	2-3	System Address 0 on Pin 4
J34	2-3	LCD Latch dis/enable

Address MAP:	Latch for LCD-Data I/O	=	2B8h
	Latch for LCD Control lines	=	not used , 2B0h

Connector J9:	Pin 1	=	VCC	Supply	
	Pin 2	=	GND	Supply	
	Pin 3	=	LCDW	-IOW	CPU
	Pin 4	=	LCD A0	SA0 Address	CPU
	Pin 5	=	LCDR	-IOR	CPU
	Pin 6	=	LCD D0	Databit 0 (R/W)	Bit 0/2B8h
	Pin 7	=	LCD D1	Databit 1 (R/W)	Bit 1/2B8h
	Pin 8	=	LCD D2	Databit 2 (R/W)	Bit 2/2B8h
	Pin 9	=	LCD D3	Databit 3 (R/W)	Bit 3/2B8h
	Pin 10	=	LCD D4	Databit 4 (R/W)	Bit 4/2B8h
	Pin 11	=	LCD D5	Databit 5 (R/W)	Bit 5/2B8h
	Pin 12	=	LCD D6	Databit 6 (R/W)	Bit 6/2B8h
	Pin 13	=	LCD D7	Databit 7 (R/W)	Bit 7/2B8h
	Pin 14	=	LCD A1	SA1 Address	CPU
	Pin 15	=	LCD Reset	Reset Drive	ISA Bus Reset
	Pin 16	=	LCD Chipselect	Select Address 2B8h	CPU

The other signals on the connector are not used by the LCD.

The protocol for the data transfer to the LCD depends on the LCD type. Please refer to the datasheet of the LCD. Ask for a driver support.

Programming Example:

Write to the LCD in Assembler:	OUT	2B8h, al
Read from LCD in Assembler:	IN	al , 2B8h

4.11.5 8 Bit Dot-Matrix LCD with the HD61830 Controller

With our LCD_DOT1.COM driver (on the ELAN_UTIL Disk) there may be controlled one HD61830 based LCD line. With this driver, the LCD is connected as a 8Bit data interface.

MSM	Signal	CPU	Dir.	LM231X	LM238X	LMG640X
1	VCC		out	2	2	2
2	GND		out	1	1	1
3	LCD_RW	-IOW	out	5, 6	5, 6	5, 6
4	LCD_CD	SA0	out	4	4	4
5	LCD_E	-IOR	out	(6)	(6)	(6)
6	LCD_D0	SD0	in/out	7	7	7
7	LCD_D1	SD1	in/out	8	8	8
8	LCD_D2	SD2	in/out	9	9	9
9	LCD_D3	SD3	in/out	10	10	10
10	LCD_D4	SD4	in/out	11	11	11
11	LCD_D5	SD5	in/out	12	12	12
12	LCD_D6	SD6	in/out	13	13	13
13	LCD_D7	SD7	in/out	14	14	14
14	SA1	SA1	out			
15	LCD_RES/	RESdrv	out	16	16	16
16	LCD_CS	PGP3	out	15	15	15

The LCD_RES/ = RESDRV and must be inverted for the LCD reset input! RESDRV is active high in the reset state. Most LCDs use RESET = active low.

LCD:	**CPU:**	
LCD_RW	-IOW	Read/Write (1= read from LCD, 0= write to LCD)
LCD_CD	SA0	Register select of the LCD (1=Command, 0=Data)
LCD_E	-IOR	Enable (Data is written at the fall of E, Data can be read while E=1)
LCD_CS	PGP3	Chip select (must be on GND to select the LCD , Pin 15)
LCD_RES/		inverter from RESDRV, use a 74HCT04 or similar

4.11.6 8 Bit DOT-Matrix LCD with the T6963C Controller

With our LCD_DOT1.COM driver (on the ELAN_UTIL Disk) there may be controlled one T6963C based LCD line. With this driver, the LCD is connected as a 8Bit data interface.

MSM	Signal	CPU	Dir.	LG24011
1	VCC		out	2, 16
2	GND		out	1
3	LCD_RW	-IOW	out	6
4	LCD_CD	SA0	out	4
5	LCD_E	-IOR	out	5
6	LCD_D0	SD0	in/out	7
7	LCD_D1	SD1	in/out	8
8	LCD_D2	SD2	in/out	9
9	LCD_D3	SD3	in/out	10
10	LCD_D4	SD4	in/out	11
11	LCD_D5	SD5	in/out	12
12	LCD_D6	SD6	in/out	13
13	LCD_D7	SD7	in/out	14
14	SA1	SA1	out	
15	LCD_RES/	RESdrv	out	
16	LCD_CS	PGP3	out	15

The LCD_RES/ = RESDRV must be inverted for the LCD reset input! RESDRV is active high in the reset state. Most LCDs use RESET = active low.

LCD:	**CPU:**	
LCD_RW	-IOW	Read/Write (1= read from LCD, 0= write to LCD)
LCD_CD	SA0	Register select of the LCD (1=Command, 0=Data)
LCD_E	-IOR	Enable (Data is written at the fall of E, Data can be read while E=1)
LCD_CS	PGP3	Chip select (must be on GND to select the LCD , Pin 15)
LCD_RES/		inverter from RESDRV, use a 74HCT04 or similar

5 DESCRIPTION OF THE CONNECTORS

Flat cable

- 44pin IDE is: IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
- All others are: IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable

Connector	Texture	Pin	Remarks
J01	PC104 Bus	104	2.54mm
J02	Power , ELAN internal RS485	2x4	2.54mm
J03	Utility (Keyboard, Mouse,...)	2x5	2.54mm
J06	Keymatrix	2x15	2mm
J09	Character, 8 Bit LCD; ELAN internal COM port (TTL- RS485 as COM1)	2x10	2mm
J10H	CRT	2x10 (40)	2.54mm
J10L	LCD	2x15 (40)	2.54mm
J11	Floppy	26	FCC micro
J14	SUPER I/O Primary Port (COM3) or COM1 if J54 = 2-3	2x5	2.54mm
J15	SUPER I/O Secondary Port (COM2)	2x5	2.54mm
J16	Parallel Port (LPT1)	2x13	2.54mm
J17	Harddisk	2x22	2mm
U13	Flash IC socket / DOC2000	2x16 or 2x18	2.54mm

J14 Serial port COM3 or (COM1)

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin10		= open

J15 Serial port COM2

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= DCD
Pin 2	Pin 6	= DSR
Pin 3	Pin 2	= RxD
Pin 4	Pin 7	= RTS
Pin 5	Pin 3	= TxD
Pin 6	Pin 8	= CTS
Pin 7	Pin 4	= DTR
Pin 8	Pin 9	= RI
Pin 9	Pin 5	= GND
Pin10		= open

J11 Floppy Disk Interface connector

FD26: Pin	Signal Name	Function	in/out
1	VCC	+5 volts	
2	IDX	Index Pulse	in
3	VCC	+5 volts	
4	DS2	Drive Select *	out
5	VCC	+5 volts	
6	DCHG	Disk Change	in
10	M02	Motor on *	out
12	DIRC	Direction Select	out
14	STEP	Step	out
16	WD	Write Data	out
17	GND	Signal grounds	
18	WE	Write Enable	out
19	GND	Signal grounds	
20	TRKO	Track 0	in
21	GND	Signal grounds	
22	WP	Write Protect	in
23	GND	Signal grounds	
24	RDD	Read Data	in
25	GND	Signal grounds	
26	HS	Head Select	out

Drive A: or B: may be selected with jumpers; default is A

J17 IDE interface

Pin	Signal	Pin	Signal
Pin 1	= Reset (active low)	Pin 2	= N.C.
Pin 3	= D7	Pin 4	= D8
Pin 5	= D6	Pin 6	= D9
Pin 7	= D5	Pin 8	= D10
Pin 9	= D4	Pin 10	= D11
Pin 11	= D3	Pin 12	= D12
Pin 13	= D2	Pin 14	= D13
Pin 15	= D1	Pin 16	= D14
Pin 17	= D0	Pin 18	= D15
Pin 19	= GND	Pin 20	= N.C. (keypin)
Pin 21	= N.C.	Pin 22	= GND
Pin 23	= IOW(active low)	Pin 24	= GND
Pin 25	= IOR(active low)	Pin 26	= GND
Pin 27	= nc	Pin 28	= ALE / Master-Slave (not used)
Pin 29	= nc	Pin 30	= GND
Pin 31	= IRQ14	Pin 32	= IOCS16 (active low)
Pin 33	= ADR1	Pin 34	= N.C.
Pin 35	= ADR0	Pin 36	= ADR2
Pin 37	= CS0 (active low)	Pin 38	= CS1 (active low)
Pin 39	= LED (active low)	Pin 40	= GND
Pin 41	= VCC Logic	Pin 42	= VCC Motor
Pin 43	= GND	Pin 44	= GND

P16 Printerport (Centronics)

The printer connector provides an interface for 8 Bit centronics printers.

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	= Strobe
Pin 3	Pin 2	= Data 0
Pin 5	Pin 3	= Data 1
Pin 7	Pin 4	= Data 2
Pin 9	Pin 5	= Data 3
Pin 11	Pin 6	= Data 4
Pin 13	Pin 7	= Data 5
Pin 15	Pin 8	= Data 6
Pin 17	Pin 9	= Data 7
Pin 19	Pin 10	= Acknowledge
Pin 21	Pin 11	= Busy
Pin 23	Pin 12	= paper end
Pin 25	Pin 13	= select
Pin 2	Pin 14	= autofeed
Pin 4	Pin 15	= error
Pin 6	Pin 16	= init printer
Pin 8	Pin 17	= shift in (SI)
Pin 10,12,14,16,18	Pin 18 - 22	= left open
Pin 20,22,24	Pin 23 - 25	= GND

J2 Power Supply connector

Pin	Signal	Pin	Signal
Pin 1	= Ground	Pin 2	= VCC (+5V)
Pin 3	= AC-Sense Input	Pin 4	= +12 Volt *)
Pin 5	= RS485 Signal A	Pin 6	= RS485 Signal B
Pin 7	= Ground	Pin 8	= LT2911 (shutdown)

AC-Sense: 0=Enable Power Manager, 1=Disable Power Manager
RS485 A and B: COM1 of the ELAN310 Controller

*) for LCD-Backlight, supplies Pin 9 of J10

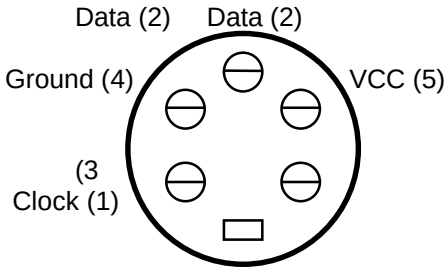
J3 Keyboard PS/2-Mouse Utility Connector

Attention: The speaker must be connected to VCC, to have a low inactive current in the speaker !

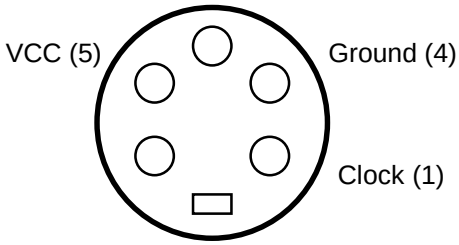
Pin	Signal	Pin	Signal
Pin 1	= Speaker Out	Pin 2	= Suspend/Resume
Pin 3	= Reset In	Pin 4	= VCC
Pin 5	= Keyboard Data	Pin 6	= Keyboard Clock
Pin 7	= Ground	Pin 8	= Ext. Accu +
Pin 9	= PS/2 Mouse Clock	Pin10	= PS/2 Mouse Data

The Utility Connector must be wired to a standard AT-female connector:

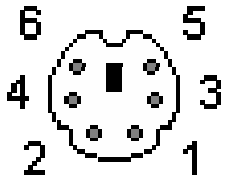
Frontside AT-Keyboard (female)



Solderside AT-Keyboard (female)



PS/2 Frontside (female)



Connector

	Mini- DIN PS/2 (6 PC)	DIN 41524 (5 PC)	Remarks
Shield	Shield	Shield	KEYBOARD
DATA	1	2	
GND	3	4	
VCC (+5V)	4	5	
CLK	5	1	
	Mini- DIN PS/2 (6 PC)		
VCC (+5V)	4		MOUSE
DATA	1		
GND	3		
CLK	5		

J10L LCD connector

VGA-LCD Interface (flatpanel signals):
Signals P20-P23 are located on the J10M connector (for higher resolution panels only)

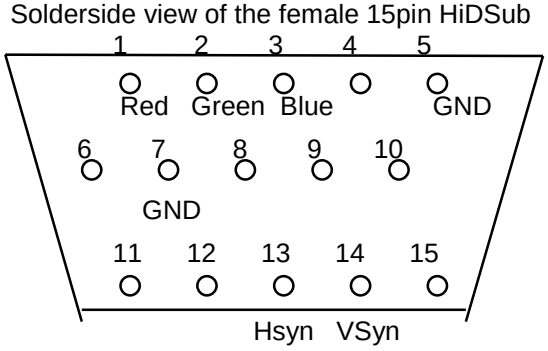
Pin	Signal	Pin	Signal
1	M-Signal (altern. DE)	2	FLM
3	P18	4	Line Pulse LP
5	VCC	6	GND
7	Enable VDD (TTL)	8	Shift Clock
9	Switched Blight (+12V/1A)	10	P3
11	P2	12	P17
13	P1	14	P16
15	P0	16	P7
17	Switched VEE (+5V/1A)	18	P6
19	open	20	P5
21	P4	22	P19
23	P8	24	P9
25	P10	26	P11
27	P12	28	P13
29	P14	30	P15

The pin 9 is supplied from the J2 pin 4 with +12V.

J10M VGA Monitor (CRT-Signals)

J10 L/M Header			15 pins HiDensity DSUB	
40 Pin -L	10 Pin -M	Signal	Pin	Signal
Pin 32	Pin 2	VGA red	Pin 1	Red
Pin 34	Pin 4	VGA green	Pin 2	Green
Pin 36	Pin 6	VGA blue	Pin 3	Blue
Pin 38	Pin 8	Horizontal Synch	Pin 13	H-Synch
Pin 39	Pin 9	Vertical Synch	Pin 14	V-Synch
			Pin 5 + 11	Bridge
Pin 31	Pin 1	Ground	Pin 5, 6, 7, 8	Ground
Pin 33	Pin 3	LCD-P20		
Pin 35	Pin 5	LCD-P21		
Pin 37	Pin 7	LCD-P22		
Pin 40	Pin 10	LCD-P23		

The VGA-CRT signals from J10 must be wired to a standard VGA HiDensity DSub connector (female):
The LCD signals must be wired panel specific.



J1 PC/104 BUS Interface

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12V)	LA18	IRQ14
8	SD1	NC	LA17	DACK0
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	Ground	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK7
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 Volt
17	SA14	DACK1	SD14	MASTER *)
18	SA13	DRQ1	SD15	Ground
19	SA12	REF *)	Ground	Ground
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

*) not available on this product

Onboard used signals (not for external use)

IRQ3, IRQ4	COM1 /2
IRQ7	LPT1
IRQ6	FD
IRQ14	HD
IRQ12	PS/2 Mouse
TC	FD
DACK2 and DRQ2	FD

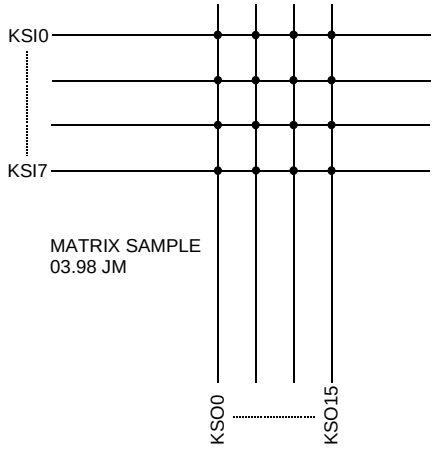
J6 Keymatrix connector

since V3.0 Keymatrix Interface:

Signals are located on the connector

Pin	Signal	Pin	Signal
1	Column 1 (KSO 0)	2	Column 2 (KSO 1)
3	Column 3 (KSO 2)	4	Column 4 (KSO 3)
5	Column 5 (KSO 4)	6	Column 6 (KSO 5)
7	Column 7 (KSO 6)	8	Column 8 (KSO 7)
9	Column 9 (KSO 8)	10	Column 10 (KSO 9)
11	Column 11 (KSO 10)	12	Column 12 (KSO 11)
13	Column 13 (KSO 12)	14	Column 14 (KSO 13)
15	Column 15 (KSO 14)	16	Column 16 (KSO 15)
17	Row 0 (KSI 0)	18	Row 1 (KSI 1)
19	Row 2 (KSI 2)	20	Row 3 (KSI 3)
21	Row 4 (KSI 4)	22	Row 5 (KSI 5)
23	Row 6 (KSI 6)	24	Row 7 (KSI 7)
25	GND	26	LED Ground
27	LED Fn-PAD (anode)	28	LED CAPs-Lock (anode)
29	LED NumLock (anode)	30	LED Scroll Lock (anode)

Each LED is connected with the cathode to the LED Ground signal Pin 26.



J9 Character-LCD and ELAN internal COM port connector

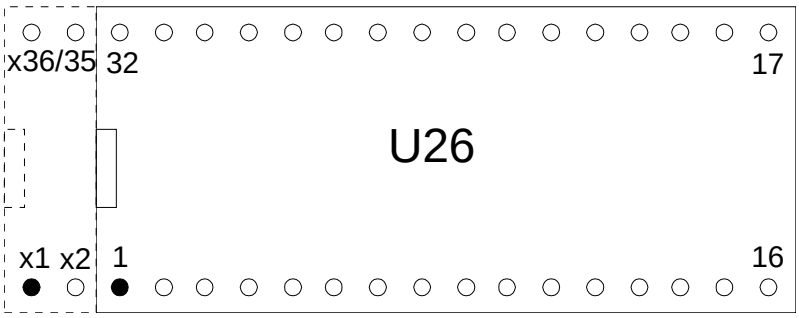
since **V3.0 Character/Graphic LCD Interface:**

Signals are located on the connector

Pin	Signal	Pin	Signal
1	VCC	2	GND
3	LCDW (-IOW)	4	LCDCD (SA0)
5	LCDE (-IOR)	6	LCD-Data 0 i/o
7	LCD-Data 1 i/o	8	LCD-Data 2 i/o
9	LCD-Data 3 i/o	10	LCD-Data 4 i/o
11	LCD-Data 5 i/o	12	LCD-Data 6 i/o
13	LCD-Data 7 i/o	14	SA1 (Adr 1)
15	RESDRV (Resetline)	16	PGP3 (Prg.I/O Line)
17	BL1 (Bat-Level Sense 1) Elan300 pin106	18	Boudout ELAN310 pin 200
19	TXD 5V (TTL)	20	RXD 5V (TTL)

U26 Flashdisk socket

Pin	Signal	Pin	Signal
1	A18	19	D5
2	A16	20	D6
3	A15	21	D7
4	A12	22	CE#
5	A7	23	A10
6	A6	24	OE#
7	A5	25	A11
8	A4	26	A9
9	A3	27	A8
10	A2	28	A13
11	A1	29	A14
12	A0	30	A17
13	D0	31	WE#
14	D1	32	VCC
15	D2	X1	A19
16	GND	X2	A20
17	D3	X35	A21
18	D4	X36	A22



6 JUMPER LOCATIONS ON THE BOARD

The figure shows the location of all jumper blocks on the MSM386SV/SN board. The numbers shown in this figure are silk screened on the board so that the pins can easily be located. This chapter refers to the individual pins for these jumpers. The default jumper settings are indicated with asterisks. Be careful when you change some jumpers. Some jumpers are soldering bridges, you need a miniature soldering station with vacuum pump.

6.1 The Jumpers on this MICROSPACE Product

RM2.54mm Jumpers on the top side

		1-2 = open	**2-3 = closed**
J5	3.6V battery charge (RTC reset)	No charging = reset	**charging = normal**
J37	LCD panel voltage	**1-2 = 5.0 V**	2-3 = 3.3 V

The jumpers on the bottom side (solder jumpers)

J7	VGA BIOS Pin 31 selection Pin 31 function:	1-2 = VCC 27C010 = VPP	**2-3 = EMEMW** **29F010/040**
J12	Floppy Drive select	1-2 = Drive B:	**2-3 = Drive A:**
J13	Floppy Motor select	1-2 = Drive B:	**2-3 = Drive A:**
J18	RS232 conversion	**1-2 = PMC4** **no sleep**	2-3 = GND sleep
J22	LPT address	1-2 = LPT2 (278h)	**2-3 = LPT1 (378h)**
J28	Watchdog	open = disabled	**close = enabled**
J29	VGA standby	1-2 = VGA enable always ON	**2-3 = PMC0** **sleep enabled**
J31	Char-LCD drive select W	**1-2 = Latch WR**	2-3 = CPU IOW
J32	Char-LCD drive select R	**1-2 = LatchRD**	2-3 = CPU IOR
J33	Char-LCD drive select A	**1-2 = LatchCD**	2-3 = CPU SA0
J34	Char-LCD drive select mode	**1-2 = Latch mode**	2-3 = CPU mode
J35	RS 485 / RS 232 RX	**1-2 = RS 485 (J2 pin 5)**	2-3 = TTL (J9 pin 20)
J36	RS 485 / RS 232 TX	**1-2 = RS 485 (J2 pin 6)**	2-3 = TTL (J9 pin 19)
J45	COM3 on IRQ4	**No IRQ4**	IRQ4
J46	COM3 on IRQ5	**No IRQ5**	IRQ5
J47	COM3 on IRQ10	No IRQ10	**IRQ10**
J48	LCD-CPU	**Open = latched**	**Closed = CPU**
J49	14MHz sleep	**PMC2**	PMC1
J50	SMC secondary COM selection	COM1	**COM2**
J51	PCF1	LOW (3BCh)	**HIGH (x78h)**
J52	PADCF	**LOW**	HIGH (ECP)
J53	ECPEN	LOW	**HIGH (ECP)**

Serial Configuration

Available since board version 5.1A!

J54	SMC primary COM selection	**1-2 = COM3**	2-3 = COM1

Settings written in bold are defaults!

COM3 to COM1, example how to make the proper settings:

BIOS- setup:	Internal com port	disabled
	Super I/O	enabled
	Internal LPT	disabled
Jumpersettings:		
J54	2-3	COM 3 to COM 1
J45	closed	IRQ 4 on COM 1 (3)
J46	open	no IRQ 5
J47	open	no IRQ10

Parallel Port Address (default LPT1)

The jumpers are available since board version 5.1, in V2.97 corrected manual!

PCF1 (RTS1) R50 / J51	PCF0 (TXD1) J22	port address	IRQ
low 1-2	low 2-3	disabled	7
low 1-2	High 1-2	PS2 3BCh	7
high 2-3	**low 2-3**	**LPT1 378h**	7
high 2-3	High 1-2	LPT2 278h	7
ECPEN (MTR2) R47 / J53	**PADCF (GAME) R54 / J52**	**port mode**	
low 1-2	low 1-2	normal	
low 1-2	high 2-3	EPP	
high 2-3	**low 1-2**	**ECP**	
high 2-3	high 2-3	ECP & EPP	

Settings written in bold are defaults!

EPP and ECP- mode enabling:

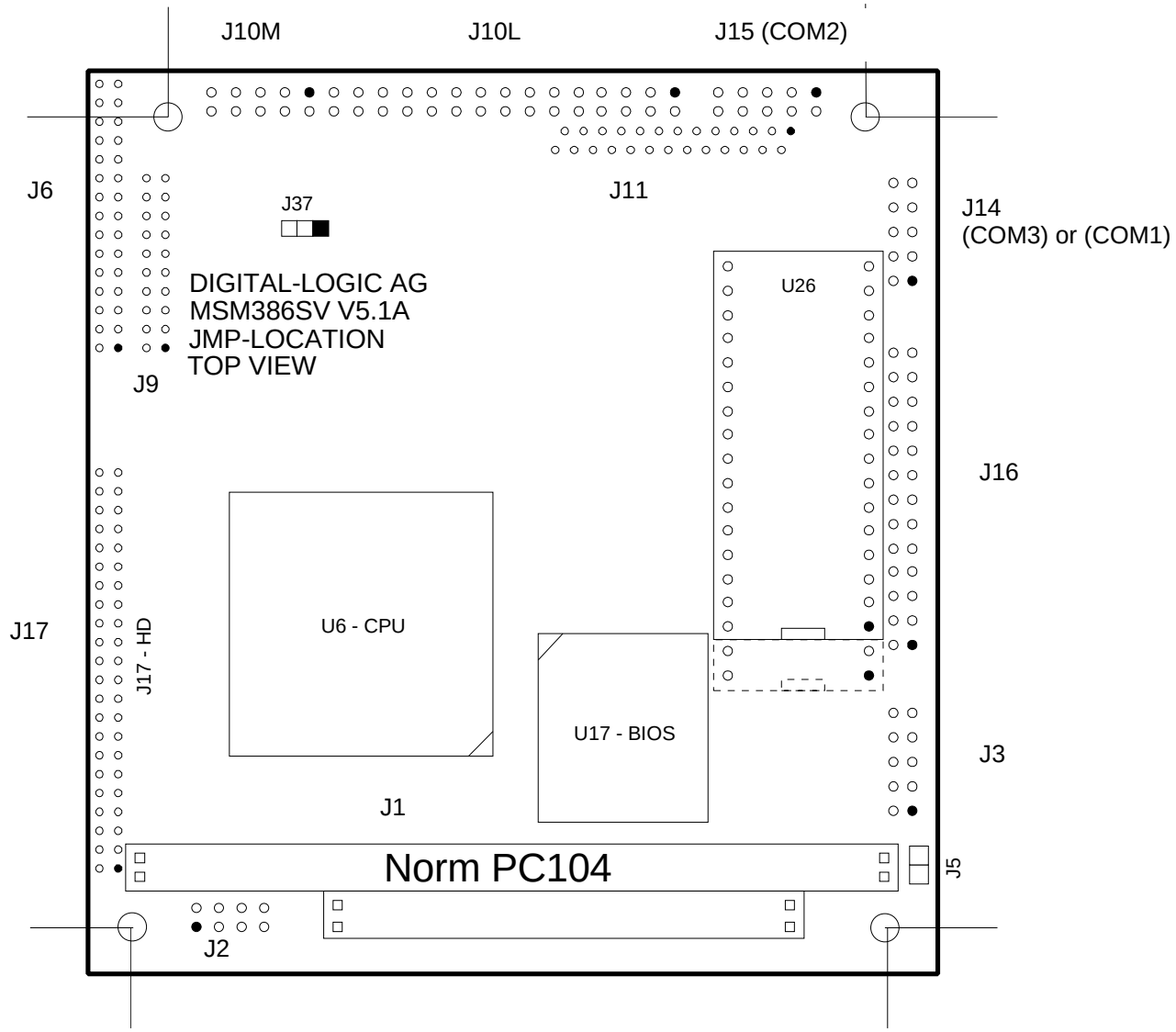
The SMC37C666 has to have the pin97 (A10) connected to the criterion A10.
This is available either on the ISA- bus (A21) or ELAN (pin62) or vga controller 65540 (pin 189).
One has to make a hardwire- fix and afterwards the EPP/ECP mode should work.

WARNING:

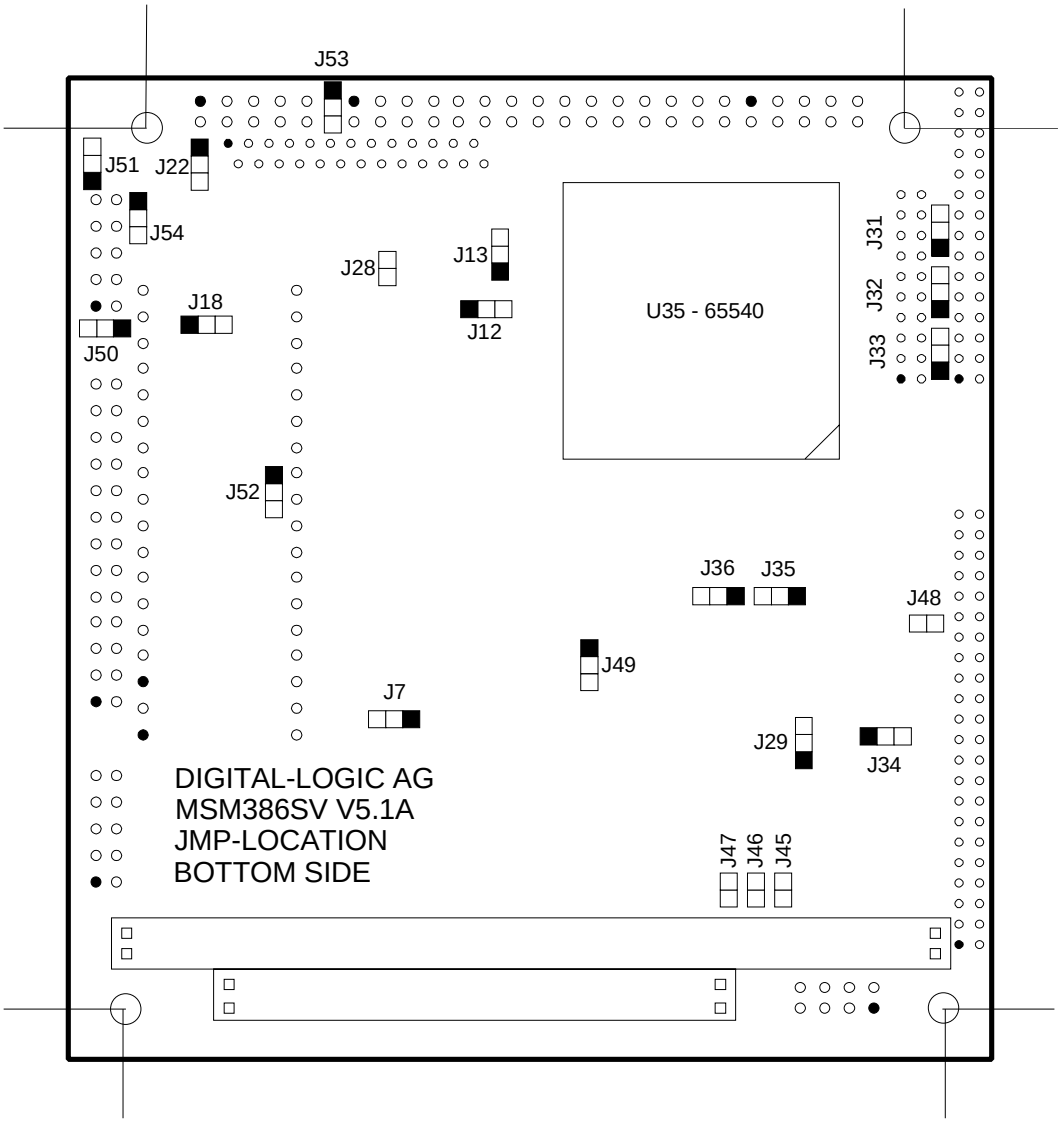
1. If the SMC primary serial port is selected to be COM1, make sure that the ELAN UART is disabled, otherwise the SMC primary port and the ELAN's serial port will access the same addresses (this is done in the BIOS-Setup). This situation can damage the parts! The SMC primary port is COM3 and the ELAN's internal UART is COM1.

2. The very first time, as the board is still a virgin, one has to have the J5 open. Feed first the MSM386 with +5volts and after that close J5. Proceed the same way by replacing a rechargeable battery, otherwise the ELAN300/310 needs more than 200µA and will empty the accu within 3 days.
   There is always a warning label with the MSM386 included.

6.1.1 Jumper locations front side



6.1.2 Jumper locations rear side



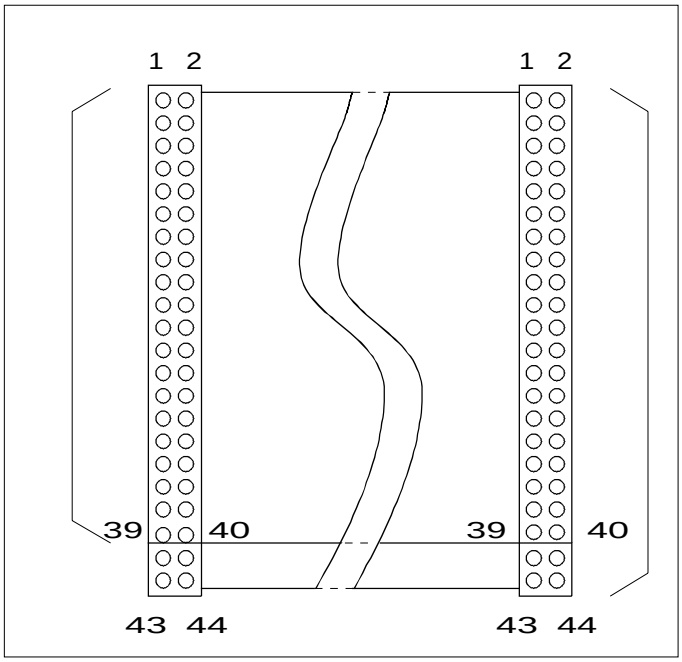
7 LED CRITERIONS:

LED	Color	Function
D9	red	Primary HDD

8 CABLE INTERFACE

8.1 The harddisk cable 44pins

IDT Terminal for Dual Row (2.00 mm grid) and 1.00 mm flat cable. 44 pins = 40 pins signal and 4 pins power.

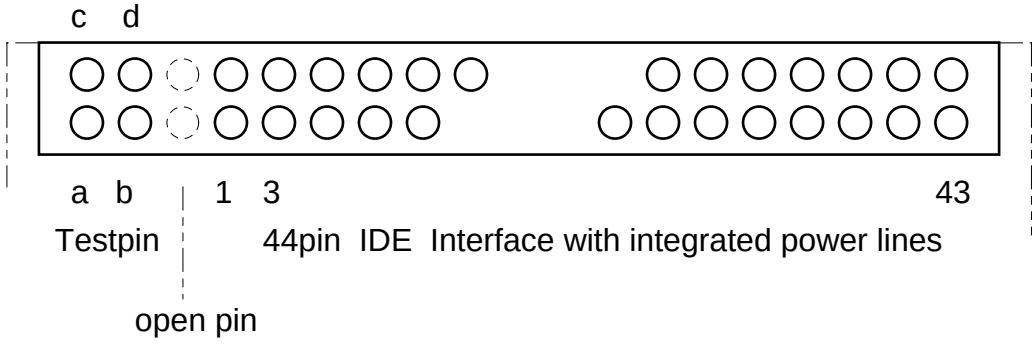


Max. length for the IDE cable is 30 cm (on Rev. B3 ELAN: make the cable as short as possible!).

ATTENTION:

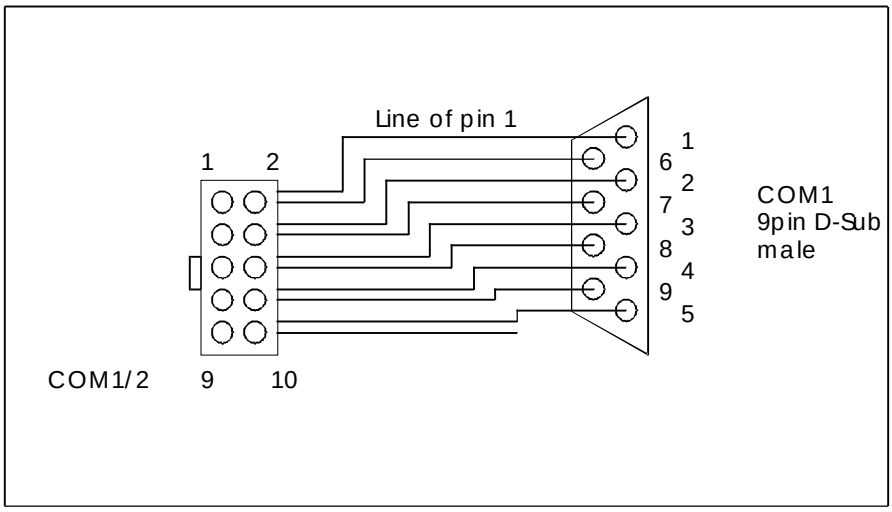
Check the pin 1 marker of the cable and the connector before you power on. Refer to the technical manual of the used drives, because a wrong cable will immediately destroy the drive and/or the MICROSPACE MSM386SV/SN board. There is no warranty in this case! Without the technical manual you cannot connect this type of drive.

The 44pin IDE connector on the drives are normally composed of the 44 pins and 2 open pins and 4 test pins, 50 pins in total. Leave the 4 test pins unconnected .



8.2 The COM 1/2 serial interface cable

DT terminal for dual row 0.1" (2.54 mm grid) and 1.27 mm flat cable.

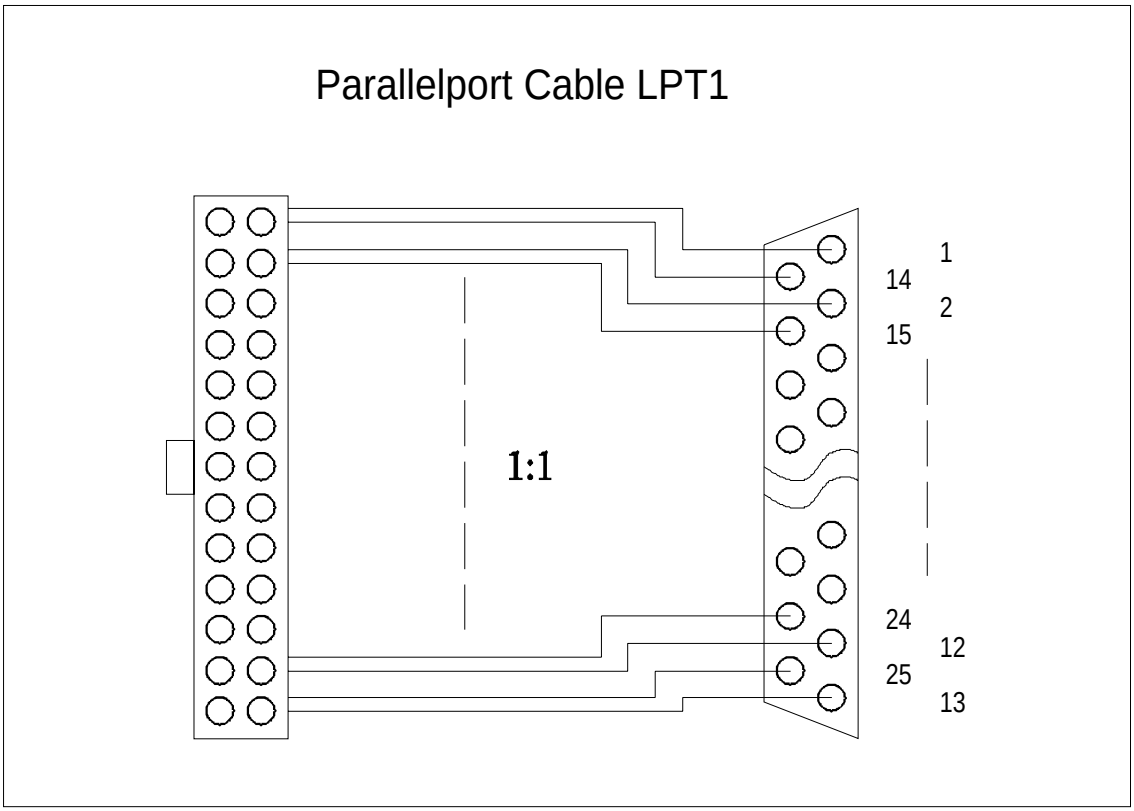


ATTENTION:

- Do not short-circuit these signal lines.
- Never connect any pins either on the same plug or to any other plug on the MICROSPACE MSM386SV/SN. The +/-10 volts will destroy the MICROSPACE core logic immediately. No warranty in this case!
- Do not overload the output: max. output current converters: 10 mA

8.3 The printer interface cable (P4)

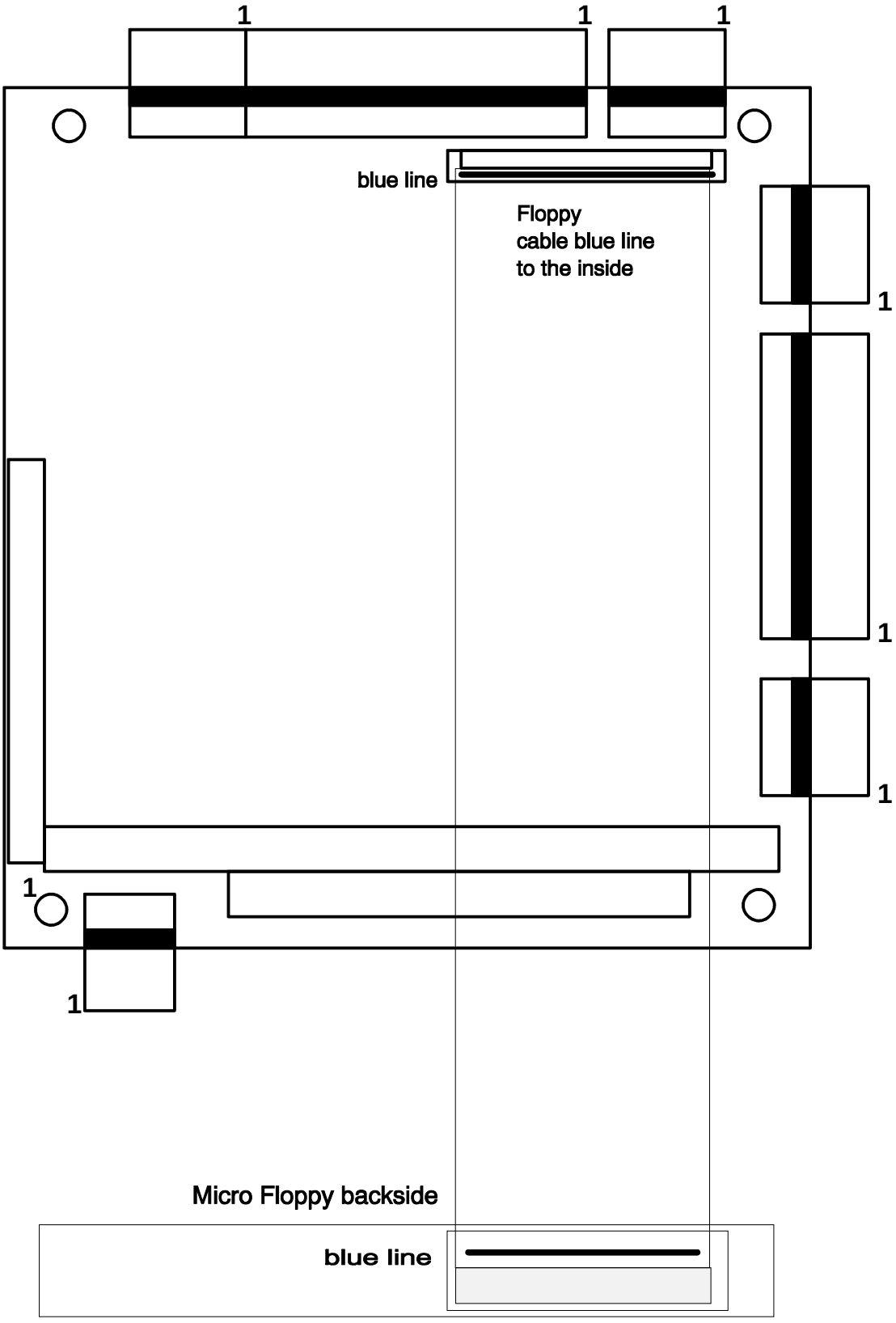
IDT terminal for dual row 0.1" (2.54mm grid) and 1.27 mm flat cable



ATTENTION:

- Maximum length of this cable is 6 meters.
- Prevent short-circuits.
- Never apply power to these signals, the MICROSPACE MSM386SV/SN will be destroyed.

8.4 The micro floppy interface cable



9 SPECIAL PERIPHERALS, CONFIGURATION

9.1 Special peripherals

9.1.1 Multifunction Latch

The multifunction latch allows control over several functions such as powerdown, contrast and watchdog. This latch can be controlled by the application program.

Latch 1: Programming address is: 2B0 hex (write only)

MSM386SV/SN:	Function:	Bit Number:
LCDWR	LSB Default = High	0
LCDCD	Default = Low	1
LCDE	Default = High	2
EEPROM Data	Default = Low	3
EEPROM SK	Default = Low	4
EEPROM Clock	Default = Low	5
NC	Default = Low	6
Watch DOG Strobe	MSB Default = Low	7

9.2 The Special Function Interface SFI

All functions are performed by starting the SW-interrupt 15h with the following arguments:

9.2.1 EEPROM Functions:

Function:	WRITE TO EEPROM
Number:	E0h
Description:	Writes the data byte into the addressed memory cell of the serial EEPROM. The old value is automatically deleted and the new databyte will be stored.
Input Values:	AH = E0h Function Request AL = Data byte to store into the EEPROM BX = Address of the EEPROM (0 - 1024 possible)
Output Values:	none; all registers are preserved.

Function:	READ FROM EEPROM
Number:	E1h
Description:	Reads the data byte from the addressed memory cell of the serial EEPROM.
Input Values:	AH = E1h Function Request BX = Address of the EEPROM (0 - 1024 possible)
Output Values:	AL = Read databyte

Function:	**READ SERIAL NUMBER**
Number:	E3h
Description:	Reads out the serial number of the board out of the EEPROM.
Input Values:	AH = E3h Function Request
Output Values:	DX, CX, BX = serial number binary (not ascii!)

Function:	**READ PRODUCTION DATE**
Number:	E5h
Description:	Reads out the production date of the board out of the EEPROM.
Input Values:	AH = E5h Function Request
Output Values:	BX, CX = BX = year, CH = month, CI = day

Function:	**TRANSFER CHARACTER FROM KEYMATRIX TO EEPROM**
Number:	E6h
Description:	Writes the data byte into the addressed memory cell of the keymatrix area of the serial EEPROM.
Input Values:	AH = E6h Function Request AL = Data byte to store into the EEPROM BX = Address of the keymatrix in the EEPROM (0 - 512 possible)
Output Values:	none; all registers are preserved.

Function:	**TRANSFER KEYMATRIX TO EEPROM**
Number:	E7h
Description:	Writes the keymatrix bytes from the 80C42PD into the EEPROM at the defined address.
Input Values:	AH = E7h Function Request
Output Values:	none

Function:	**READ INFO2**
Number:	E9h
Description:	Reads out the information bytes out of the EEPROM from the defined address.
Input Values:	AH = E9h Function Request
Output Values:	AL = Board Type (M= PC/104, E= Euro, W= MSWS, S= Slot, C= Custom) DI = CPU Type (1= ELAN310, 2= ELAN400, 3= 486SLC, 4= DX, 5= P5) BH, BL= Board version (Ex.: V1.5 -> BH= 1, BL= 5) CH, CL= BIOS version (Ex.: V3.0 -> CH= 3, CL= 0) DH = Number of 512k Flash (0= none, 1= 0,5M, 2= 1M, 3= 1.5M etc.) DL = Number of 512k SRAM (0= none, 1= 0,5M etc.)

Function:	**READ INFO3**
Number:	EAh
Description:	Reads out the information bytes out of the EEPROM from the defined address.
Input Values:	AH = EAh Function Request
Output Values:	AX = number of boot errors BX = number of setup entries CX = number of low battery errors DX = number of power on starts

9.2.2 Watchdog functions:

Function:	**WATCHDOG**	
Number:	EBh	
Description:	Enables, strobes and disables the watchdog. After power-up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. Once the watchdog has been enabled, the user application must perform a strobe at least every 800ms, otherwise the watchdog performs a hardware reset.	
Input Values:	AH = EBh Function Request AL = Disable / Enable and strobe of the watchdog	0 = Disable 01 - FE = Enable FF = send strobe
Output Values:	none	

9.2.3 INT15 Information:

Function: Information about INT15-support on the board
Number: EFh

Description: Gives informations about the supported interrupt 15 functions.

Input Values:
- AH = EFh Function Request
- AL Number of Interrupt, where you need information

Output Values:
- BX Interrupt-Information Word
- BH Versionsnumber of Interrupt (0 = Not supported)
- BL Second-Versionsnumber.

If AL is 0EFh you will get special Information.
- BX
  - BH Bit0...Bit5 Versionsnumber of Interrupt
  - Bit6 Extendet Interrupts not available. If it sets, there is no DLAG-Interrupt with request higher than 0EFh.
  - Bit7 Must be Zero
- BL Second-Versionsnumber.
- CX DLAG Indentification Code, must be 'DL'. This Register gives you the posibility to check if there are DLAG-Interrupts installed. If you want to check, set register CX to zero before calling Interrupt 15 with request 0Efh in AL. After this command, there must be 'DL' in the CX register (CH=>'D', CL=>'L'). If it is not so, the BIOS does not support DLAG-Interrupts 15. Ask your Distributor for the newest DLAG-BIOS.

9.3 The Flashdisk

The following Flashdisk/drives may be installed on the board:

1. IDE-Flashdrive module with 2, 4, 10MByte are 100% IDE disk compatible.
   Up to 2 drives are possible as master and slave drive interface. The capacity may be doubled up to 2 x 10MByte.
2. Flashmodule from DIGITAL-LOGIC AG with 2, 4, 6, 8MByte are fully DOS compatible.
3. Single 512k Flashdevice with 512k.
4. M-Systems DISK-ON-CHIP module with capacities up to 12MByte.

The IDE-Flashdrive may be mixed with one of the 3 Flashdisk modules/devices.

	Memory Windows	Write Speed	Read Speed	Reliabil-ity	FFS	Supported OS	Drive Letter
IDE-Flashdrive Module	none, IDE-Interface	150kByte/s	300kByte/s	100kCycle	Controller	all	C: (boot)
Master-Slave IDE Flashdrive	none, IDE-Interface	150kByte/s	300kByte/s	100kCycle	Controller	all	C: (boot) D:
Flashmodule	D0000 - DFFFF	25kByte/s	150kByte/s	100kCycle	FFS-Bios	DOS, Win	C: (boot)
Flashdevice	D0000 - DFFFF	25kByte/s	150kByte/s	100kCycle	FFS-BIOS	DOS, Win	C: (boot)
M-Systems DiskOnChip	D0000-DFFFF	25kByte/s	150kByte/s	100kCycle	TFFS	DOS, Win	C: (boot)

9.3.1 Which Flashdisk Systems need a Flash-File-System

The Flash-File-System allows you to READ and WRITE information to and from the flashdisk, without limitation. Only on the flashdrives of 4 or 10MByte, a special controller emulates this flash as an IDE drive. All other flashdisks need a BIOS extension containing the Flash-File-System software. This FFS-BIOS must correspond to the used flashdisk capacity.

9.3.2 Usable DOS size of a Flash-File-System

Depending on the MICROSPACE product, different sizes and types are supported:

On the Flashdisk, the real usable capacity must be smaller than the installed devices, due to the spare sector of 2 x 64kByte and the memory area used by the FFS.

onboard	usable DOS size
512k installed flash	usable DOS size = 396 kByte
2048k installed flash	usable DOS size = 1920 kByte
4096k installed flash	usable DOS size = 3968 kByte
8192k installed flash	usable DOS size = 8064 kByte

WARNING:

Disable the SHADOW-RAM option in the BIOS-Setup, otherwise the Flashdisk is not accessible, as the D-Segment is not transparent to the ISA-Bus.

9.3.3 Used Memory Window on the PC

The FFS software uses a 64k memory window at ELAN300:D000-DFFFF to transfer data to and from the flashdisk.

Only the IDE Flashdrive needs no memory window.

The DiskOnChip needs also a memory window as the FFS software with 64k in the D-Segment.

The EMM386 and the HIMEM tools may not use this memory space.

9.3.4 Access and Data Integrity of the Flashdisk Technologies

The IDE Flashdrives operates with 512 byte sectors, the same size as a standard harddisk. This drives needs max. 10ms to store the information. That means, that the application must not preview any protections for powerloss or other mistakes. In this flashdrives no time consuming reorganizing is needed.

At the flashdisk based on standard flashdevices as 29F040 or 29F016 or M-System flashes needing a FFS-BIOS, the smallest sector is 64kByte. In this case a reorganizing is needed. This reorganizing may dure up to 2 seconds, depending on the CPU performance, the disksize, the number and size of the entire files. Therefore, the application must remark a powerfailure in advance and stop the transfer of data at least 3 - 5 seconds before the supply ot the PC is falling down. A powerloss until reorganizing or accessing the flashdisk may result in dataloss, up to fully destroy the disk information. You must compare this technology to a floppy access. For floppy- and harddisk, if the power fails until the acces is performed, the data integrity may not be guaranteed and a dataloss must be expected.

9.3.5 Installing the IDE-Flashdrives

On the IDE connector the MSM-Flashdrives with 4MByte or 10MByte may be mounted directly onboard. With 3 screws and plastic bolts the module is fixed onto the PC-board.

To install two drives, the second one must be jumpered as slave, the first as master.

The slave drive may be stacked onto the master flashdrive and also fixed with 3 screws and plastic bolts.

Operating Systems:

All operating systems are working with these drives, because the flashdrives emulate a standard IDE harddisk with 4 or 10 MBytes. No drivers are nedded.

9.3.5.1 Enabling and Formatting IDE-Flashdrives

Enabling:

After installing the flashdrives, enter the BIOS-Setup. In the BIOS-Setup install drive C: with autodetect. If the slave drive is also installed, select drive D: also as autodetect. Both drives will be recognised automatically. Please verify the capacity. If OK, exit the CMOS-Setup with EXIT and SAVE.

Formatting:

1. Start the tools FDISK from the DOS-Diskette and enter the partition for the master and (if available) the slave drive.

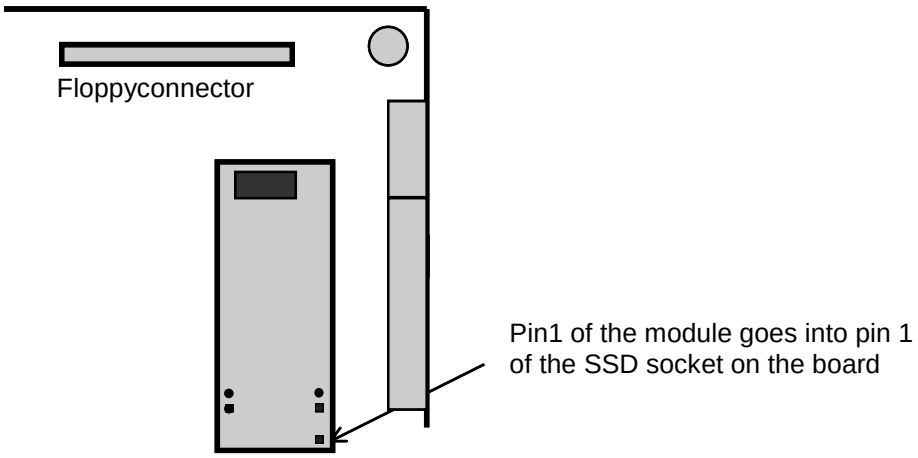
2. Start the FORMAT tool from the DOS-Diskette and format the whole drive as usual on a standard IDE harddisk. Use the SYS to transfer the bootfiles or use the option /S with the format.exe.

9.3.6 Installing the DIGITAL-LOGIC Flashdisk Module

On the SSD 36pin socket the MSM-Flashmodules with 2, 4, 6, 8MByte may be installed directly onboard.

Operating Systems:

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN are working with these drives.
All other non DOS compatible systems need a driver.
Give attention to the pin 1 orientation:



9.3.6.1 Enabling and formatting the Flashdisk Module

Enabling:

After installing the flashdisk module, make the following settings in the BIOS-Setup:

➔	"Standard"	-> "Diskette Disk"	-> Disk Drive B : "DLAG FLASH"
➔	"Preferences"	-> "Virus Alert"	-> Disable
➔	"Memory"	-> "Video & BIOS shadow"	-> Disable

Format:

- copy onto a bootable floppy disk the file "`CD:\xxx\ffs_v600\dlffsfmt.exe`"
  and the DOS programm "`sys.com`"
- boot from this floppy disk
- start the flash format program `dlffsfmt c:`
  If not accessible try the following: `dlffsfmt 80` (only needed at the first format cycle)

  -> The screen should inform about the status of the flashdisk.
  transfer the bootfiles to the flash with the command `sys a: c:`

- From this moment, the flashdisk is now the bootable drive C: and if any harddisks are connected, the drive letter changes form C: -> D: and form D: -> E: .

Please note, that each FFS version needs a specific tool:

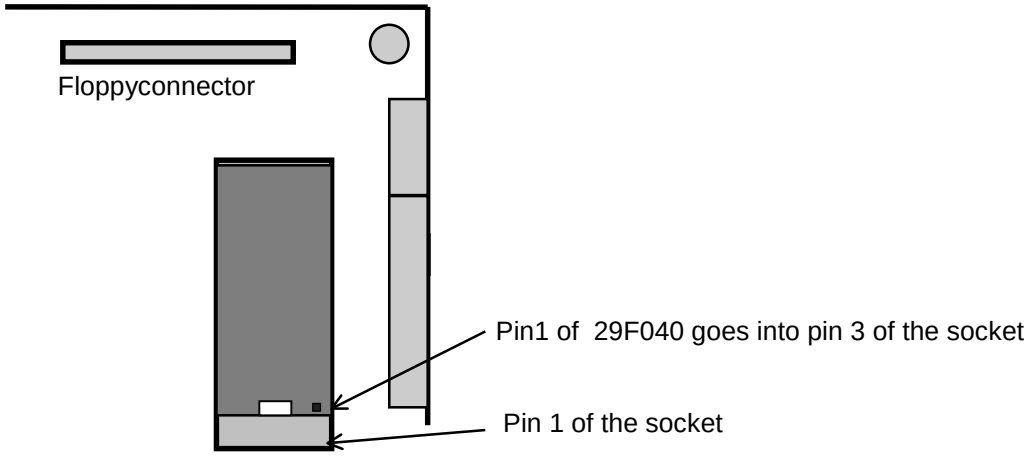
If this is version 5.xx (first boot), then one has to use	DLFMT.EXE
If this is version 6.xx (first boot), then one has to use	DLFFSFMT.EXE
If this is version 7.xx (last boot), then one shall use	FXFMT.EXE

9.3.7 Installing the flashdevice 29F040

On the SSD 36pin socket a standard 32pin DIL 29F040 flashdevice with 5V programming voltage may be installed with a capacity of 512k Byte. This device is available from AMD.
Do not use a 27C040, because the Pin 1 is not compatible (Flash = A18, EPROM = VPP)

Operating Systems:

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN are working with these drives.
All other non DOS compatible systems need a driver.
Give attention to the pin 1 orientation in the 36pin SSD socket.
Pins 1, 2 and 35, 36 are not used by the 29F040 device and must be open.



9.3.7.1 Enabling and formatting the 29F040 flashdevice

Enabling:

After installing the flashdisk module make the following settings in the BIOS-Setup:

➔	"Standard"	-> "Diskette Disk"	-> Disk Drive B : "DLAG FLASH"
➔	"Preferences"	-> "Virus Alert"	-> Disable
➔	"Memory"	-> "Video & BIOS shadow"	-> Disable

Format:

- copy the format utility "`CD:\xxx\ffs_v500\dlfmt.exe`" and the DOS programm "`sys.com`" onto a bootable floppy disk
- boot from this floppy disk
- start the flash format program `dlfmt c:`
  If not accessible try the following: `dlfmt 80` (only needed at the first format cycle)
  -> The screen should inform about the status of the flashdisk.
- transfer the bootfiles to the flash with the command `sys a: c:`

  From this moment, the flashdisk is now the bootable drive C: and if any harddisks are connected, the drive letter changes form C: -> D: and form D: -> E: .

Please note, that each FFS version needs a specific tool:

If this is version 5.xx (first boot), then one has to use DLFMT.EXE
If this is version 6.xx (first boot), then one has to use DLFFSFMT.EXE
If this is version 7.xx (last boot), then one shall use FXFMT.EXE

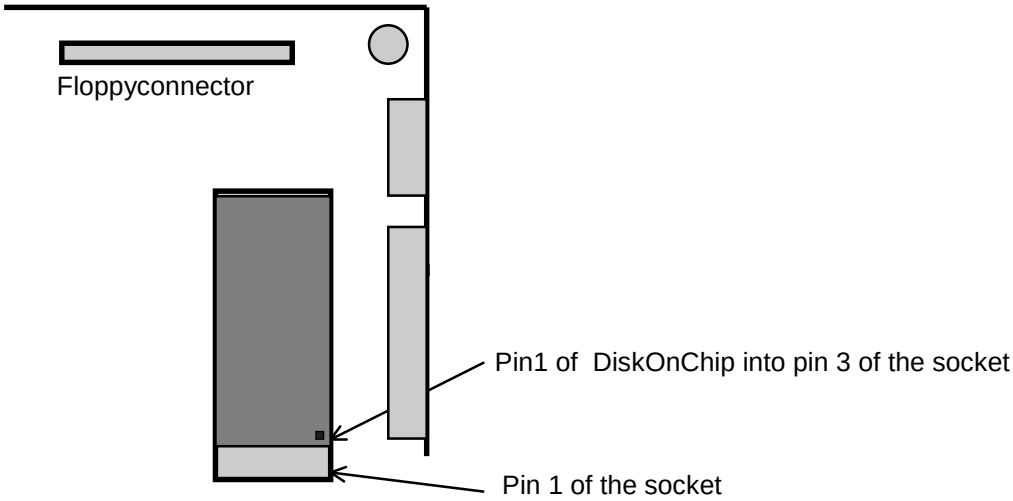
9.3.8 Installing the DOC2000 (M-System)

On the SSD 36pin socket a DiskOnChip module from M-Systems may be installed with a capacity of 512k to 12MByte. This device is available from DIGITAL-LOGIC AG.

Operating Systems:

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN are working with these drives.
All other non DOS compatible systems need a driver.

Give attention to the pin 1 orientation in the 36pin SSD socket.
Pins 1, 2 and 35, 36 are not used by the DiskOnChip device and must be open.



9.3.8.1 Enabling and formatting of the DOC2000 (M-System)

Enabling:

After installing the flashdisk module make the following settings in the BIOS-Setup:

➔ "Standard" -> "Diskette Disk" -> Disk Drive B: "none"
➔ "Preferences" -> "Virus Alert" -> Disable
➔ "Memory" -> "Video & BIOS shadow" -> Disable
(Check folder of the BIOS shadow !)

Formatting:

- Copy the format utility "`CD:\xxx\doc2000\v1.0x\dformat.exe`",
  the "`CD:\xxx\doc2000\v1.0x\doc10x.exb`" and the DOS-program "`sys.com`"
  onto a bootable floppydisk.

- boot form this floppydisk and start dformat.exe
  The screen should inform about the status of the flashdisk.
  use: `dformat /win:dc00 /s:doc10x.exb /first`
  use: on DOC2000 V1.04 modules dformat /win:DE00 /S:DOC104.EXB /FIRST
  use: on DOC2000 V1.05 modules dformat /win:DE00 /S:DOC105.EXB /FIRST
  etc.

- Make the flash bootable with the command: `sys a: c:`

From this moment, the flashdisk is now the bootable drive C: and if any harddisk is connected it changes to letter D: and E:
(This is part of the DOC2000 BIOS extension and can not be changed by DLAG)

9.4 The Powersave Functions

9.4.1 Hardware controlled suspend/resume Function

The suspend input pin may be used to suspend the system or to resume the system. The input is TTL compatible. A falling pulse generates a suspend. The second puls generates a resume of the system. The next one will again generate a suspend, and so on. This input is internally pulled up with 10k Ohms. The external circuit must be glitch free.

9.4.2 Software controlled Power Management Functions

1. Step: Enable the Power Manager by connecting the AC-Sense input (J2 pin3) to Ground.
The open AC-Sense input is onboard pulled up, so the Power Manager is disabled.

2. Step: Enter into the BIOS-Setup and select the Power Management options.
Click onto the general Power Manger to enable the function.
Enter the timeout for the different powermodes.

3. Step: Restart the system

9.4.3 The different Powermodes

PM Mode	CPU Clock	VGA Status	HD Status	Keyboard	Wakeup Activity	Powerdown
Highspeed	33MHz	working	working	working	Software	Timeout
Lowspeed	1MHz	sleep	sleep	working	KBD	Timeout
Doze	pulsed 1MHz	sleep	sleep	pulsed work	KBD	Timeout
Sleep	DC	sleep	sleep	sleep	resume-pin	Timeout
Suspend	DC	sleep	sleep	sleep	resume-pin	

9.4.4 Software controlled Powermode Switching

The powermodes may also be switched with software commands directly from the application.

The register 88h in the ELAN chipset enables the switching to another powermode:

Index 88h: 00h = Highspeed 33MHz
04h = Lowspeed 1MHz
01h = Doze Mode
03h = Sleep Mode
02h = Suspend Mode

To program an ELAN register use the following assembly code:

```
mov al,88h    Registerindex 88h
out  22h,al
mov al,04h    Lowspeed
out  23h,al
```

or with 16Bit access:

```
mov ax,8804h
out 22h,ax
```

The register B1h in the ELAN chipset selects the clock of the Highspeed mode:

Reg.B1h	D7	D6	D5	D4	D3	D2	D1	D0
Bit:	EBRMMD1	EBRMMD0	-	HSPLL1	HSPLL0	XTAL-USE	LCDDUEN	-
used for:	PCMCIA	PCMCIA		HiSpeed	HiSpeed	UART	int LCD	
Bit = 0	1x 512k	2 x 512k				X1OUT=Z	disabled	
Bit = 1	2MB	2 x 2MB				X1OUT= 14.3MHz	enabled	

Hi speed: 00 = 40MHz
01 = 50MHz
10 = 66MHz
11 = not used

The register ADh in the ELAN chipset selects the clock of the Lowspeed mode:

Reg.ADh	D7	D6	D5	D4	D3	D2	D1	D0
Bit:	-	IRQ0SMIE	-	ENACIN	XTKBDEN	MainON	LSpeed1	LSpeed0
used for:		SMI		PMU	XT - KBD	PMU	LoSpeed	LoSpeed
Bit = 0		off		Disable	off	on		
Bit = 1		on		Enable	on	off		

Low speed: 00 = 4.6MHz
01 = 2.3MHz
10 = 1.1MHz
11 = 0.5MHz

For further information about the ELAN Power Management refer to the programmer's reference manual.

10 BUILDING A SYSTEM

To build up a system based on your board, you should prepare the following equipments:

- A stable power supply of 5V (> 3 ampères), depending on the cpu, memory, etc.
- Assemble CPU with the proper clk- settings and cooling (fan) depending on board.
- If necessary, a 12V power supply for LCD or onboard sound.
- 8 ohm speaker for an executed beep code (if available on the board). One may use a capacity of 1µF connected to VCC depending on the board.
- A micro- floppy disk drive (3,5") with a PC floppy cable (26 pin) or a standard FDD with appropriate cable converter. You need at least one floppy to boot for the first time.
- A harddisk IDE 2,5" or 1,8" with the appropriate cable (44 pin and 2mm grid). Do not use a too long a cable to avoid accessing problem as the IDE controller is may not able to drive the HDD.
- Connect a LCD or a monitor.
- Use an AT-compatible keyboard (5 PC) or (6 PC {PS/2} with an appropriate adapter).
- If desired, connect a mouse to it (COM or PS/2 if usable on the board).
- Connect a battery (Lithium 3V or NiMH 3.6V depending on the board) to store the data in the BIOS.

10.1 Starting up the System

Power-up the system and wait for the BIOS to show the BIOS activity on the screen. The BIOS diagnoses the system and displays the size of the memory being tested. Note: you may can not bypass the memory test depending on the BIOS producer.

CMOS-SETUP

If the CMOS configuration is incorrect, the BIOS tells you to enter the setup screen by pressing a key. Select the correct options with the arrow keys and save them.

	SYSTEM SOFT CO
BIOS setup	CTRL- ALT- S
Change values	ARROWS / SPACE
Jump	TAB
Save	ARROWS
Back / exit	ESC

BEEP CODE:

SYSTEM SOFT CO	
4 short	RAM
3 s / 1 l	RAM test failed
2 s / 1 l / 1 s	BIOS is not shadowed
1 s / 1 l / 2 s	BIOS checksum bad
1 l / 1 s / 1 l / 1 s	CRISIS code / CR bad

11 THE POD-ERRORS

The following numeric codes appear on the System Board LEDs (in hex) to report the progress of the Power-On Diagnostics, or on the LEDs and on the screen (in decimal) to report errors found by the Diagnostics. The Pod-Latch address is 80h on 386/486 chipsets.

Error Codes -- Power-on Diagnostics

LEDs (hex)	Screen (dec)	Meaning
00H	00	Some Type Of Long Reset
01H	01	Turn off FASTA20 for POST
02H	02	Reset Cache Controller
03H	03	Signal Power On Reset
04H	04	Initialize the Chipset
05H	05	special init of VGA
06H	06	Search For ISA Bus VGA Adapter
07H	07	Reset PIC's
08H	08	Reset Counter/Timer 1
09H	09	Initialize Video Adapter(s)
0AH	10	Initialize Color Adapter
0BH	11	Initialize Monochrome Adapter
0CH	12	Test 8237A Page Registers
0DH	13	checksum the ROM
0EH	14	Test Keyboard
0FH	15	Test Keyboard Controller
10H	16	Check If CMOS Ram Valid
11H	17	Test Battery Fail & CMOS X-SUM
12H	18	user register config through CMOS
13H	19	Size Memory
14H	20	Test Memory Refresh Working
15H	21	Dispatch To RAM Test
16H	22	Test the DMA controllers
17H	23	Initialize 8237A Controller
18H	24	Initialize Int Vectors
19H	25	RAM Quick Sizing
1AH	26	Protected mode entered safely
1BH	27	RAM test completed
1CH	28	Protected mode exit successful
1DH	29	Setup Shadow
1EH	30	Going To Initialize Video
1FH	31	Search For Monochrome Adapter
20H	32	Search For Color Adapter
21H	33	No video display
22H	34	Signon messages displayed
23H	35	special init of keyboard ctlr
24H	36	Test If Keyboard Present
25H	37	Test Keyboard Interrupt
26H	38	Test Keyboard Command Byte
27H	39	Fatal Error - HALT POST
28H	40	TEST, Blank and count all RAM
29H	41	Protected mode entered safely (2).
2AH	42	RAM test complete
2BH	43	Protected mode exit successful
2CH	44	Update OUTPUT port
2DH	45	Setup Cache Controller
2EH	46	Test If 18.2Hz Periodic Working
2FH	47	test for RTC ticking

LEDs (hex)	Screen (dec)	Meaning
30H	48	initialize the hardware vectors
31H	49	special init of COMM and LPT ports
32H	50	Configure the COMM and LPT ports
33H	51	Initialize the floppies
34H	52	Initialize the hard disk
35H	53	Initialize option ROMs
36H	54	OEM's init of power management
37H	55	Search and Init the Mouse
38H	56	Update NUMLOCK status
39H	57	Test For Coprocessor Installed
3AH	58	OEM functions before boot
3BH	59	Dispatch To Op. Sys. Boot
3CH	60	Jump Into Bootstrap Code
70H	112	Save EEP to CMOS
71H	113	Save CMOS to EEP
72H	114	Save EEP to Matrix

12 THE BIOS HARDDISK LIMITATIONS

Note:
The ELAN300 with the SYSTEMSOFT- BIOS does support maximum 8192 cylinders (ca 3GB !)

by Jan Steunebrink
Version 2, June 1999
This article is published at <http://web.inter.nl.net/hcc/J.Steunebrink/bioslim.htm>

Contents

Introduction

In the last few years, harddisks have become larger and faster at an incredible rate.
Due to the favorable prices of the present large Enhanced IDE drives and the ever expanding software footprint, the whole class of 486 and Pentiums PCs can benefit of a harddisk upgrade.
This article targets at these PCs that have a system BIOS dated from 1992 to 1998.
These BIOSes can limit the usable capacity of your new (E)IDE drive.

Note: All MB values in this article are 1,048,576 Bytes (1024x1024).

The Interrupt 13h interface

When IBM engineered the AT they put the interface for the harddisk (Int 13h) in the system BIOS.
Whenever an application wants to read from/write to a drive, it calls DOS.
DOS knows the structure of the disk and where the target file is located. It then calculates a CHS (Cylinder, Head, Sector) address and calls the BIOS via Int 13h.
The BIOS then executes the read or write command at this CHS address by accessing the HD controller directly via its I/O-port addresses.
The result is passed back to DOS who passes it back to the application.
This scheme makes DOS (drive) hardware independent and leaves the hardware specifics to the BIOS.

The traditional BIOS Int 13h interface has the following limitations (when called from DOS):
1024 Cylinders, 256 Heads and 63 Sectors/track.
With 512 bytes/sector this counts up to 8 GB (8064 MB)!

The 504 MB BIOS Limit

The (in)famous 504 MB (528 million bytes) limit comes from the fact that the ATA (IDE) specification has different limits than the BIOS. When the traditional BIOS Int 13h interface is used to control an (E)IDE harddisk, the limits are combined as illustrated below.

	BIOS	IDE	Combined Limit
Max. Sectors/track	63	255	63
Max. Heads	256	16	16
Max. Cylinders	1024	65536	1024
Max. Capacity	8 GB	127.5 GB	**504 MB**

If you do not have an Enhanced BIOS, you need one of these solutions to break the 504 MB barrier:

1. A translating (Enhanced) BIOS upgrade
2. Add-in card with an Enhanced BIOS (this takes over the Int 13h interface only)
3. Software like Disk Manager from Ontrack or EZ-Drive from StorageSoft (formerly Micro House).

The translating BIOS

The traditional BIOS Int 13h interface passes the CHS address directly onto the harddisk controller, thereby creating the 504 MB barrier in case of an (E)IDE drive.
Nowadays we have the translating BIOS whose Int 13h interface can translate the CHS address to a different geometry or to an LBA (Logical Block Address).

The CHS which DOS uses to call the BIOS is now called the L-CHS (Logical CHS) and the CHS which the BIOS uses to control the drive is the P-CHS (Physical CHS).

Two translation methods can be distinguished:

1. The first method is normally used for direct L-CHS to P-CHS translation.
   According the ATA-2 specification, all EIDE drives up to 8 GB should conform to the (BIOS) Sector limit of 63 sectors/track. On a >504 MB drive with a maximum of 16 Heads (IDE limit), only the number of Cylinders will be above the BIOS limit of 1024.
   This makes a simple CHS translation scheme possible in which the number of Cylinders is divided by 2, 4, 8 or 16 and the number of Heads is multiplied with the same number.
   The number of sectors/track will remain unchanged.
   The maximum capacity depends on the number of sectors/track and is equal to the BIOS limit of 8064 MB if the drive has 63 sectors/track.

   The following table illustrates this.

Actual Cylinders	Actual Heads	Altered Cylinders	Altered Heads	Max. Capacity
1<C≤1024	1<H≤16	C=C	H=H	504MB
1024<C≤2048	1<H≤16	C=C/2	H=H*2	1008MB
2048<C≤4096	1<H≤16	C=C/4	H=H*4	2016MB
4096<C≤8192	1<H≤16	C=C/8	H=H*8	4032MB
8192<C≤16384	1<H≤16	C=C/16	H=H*16	8064MB

Example: A 2014MB drive has a CHS count of 4092x16x63. According to the above method, this will be translated into 1023x64x63, nicely within the Int 13h interface limit.
In other words; DOS (or any other OS which uses the BIOS Int 13h interface for that matter) thinks that it deals with a drive which has 1023 Cylinders, 64 Heads and 63 Sectors/track while the BIOS still controls the drive with its original geometry.
Note: A drive which has 16 Heads and more than 8192 Cylinders (> 4 GB) will be translated to 256 Heads. This is a problem because DOS can't handle 256 Heads, but there is an easy workaround for that. See "The 4 GB Limit" below.

Because the translation is done with powers of 2, the software inside the BIOS can accomplish this by simply shifting the bit patrons of the Cylinder and Head addresses one or more places to the right respectively to the left.
This translation is therefore known as the bit-shifting translation.

2. The second method is used with drives that can be accessed with LBA.
The translation here is from L-CHS (DOS) to LBA (drive).
With LBA, all sectors are numbered sequentially and the P-CHS is not used anymore.
The BIOS controls the drive by sending the required sectornumber (= LBA) to the drive instead of the P-CHS.
DOS however, still works with the CHS address so the BIOS has to calculate an artificial L-CHS and present this geometry to DOS.
This L-CHS is calculated from the total capacity of the drive as indicated below.

Capacity X in bytes	Sectors	Heads	Cylinders
1<X≤504MB	63	16	X/(63*16*512)
504MB<X≤1008MB	63	32	X/(63*32*512)
1008MB<X≤2016MB	63	64	X/(63*64*512)
2016MB<X≤4032MB	63	128	X/(63*128*512)
4032MB<X≤8032.5MB	63	255*	X/(63*255*512)

As you can see, the number of Sectors/track is fixed at 63 and the number of Heads is 16 or a multiple of that. Then the number of Cylinders is calculated by dividing the total capacity in bytes by the number of bytes per cylinder.
This translation is called the LBA assisted method.
*Note: The last row of the above table indicates that a drive over 4 GB should be translated to 255 i.s.o. 256 Heads. This to avoid problems with DOS which is unable to handle 256 Heads. For more information see "The 4 GB Limit" below.

The two translation methods produce similar geometries (L-CHS) in many cases. The difference becomes apparent when a drive reports less than 63 Sectors/track.
The LBA assisted method **always** assigns 63 Sectors/track.
The LBA assisted method is therefore more flexible than the bit-shifting translation and places no limits on the reported drive geometry (P-CHS).
The bit-shifting method however, has to be used if the drive cannot handle LBA.
Note that most translating BIOSes require you to set the P-CHS values in the BIOS setup.

With any translation method, the BIOS has to ensure that the sectors are accessed in the same order as with "untranslated" access.
This however, is NOT always the case. Therefore, it can be DANGEROUS to your data if you change to another translation mode on an already formatted drive!

Does my BIOS support translation?

Now that the theory has been dealt with, it is time to answer this question.
First check your BIOS date. If it is 7/94 or later, chances are pretty good that you have a translating BIOS. With older BIOSes, your chances are reducing.
Secondly, you can check in the BIOS SETUP if you have User definable drive types and if there is a translation MODE selection. MODE indications like LARGE or ECHS are normally used for bit-shifting translation. If you can select LBA mode, your BIOS supports the LBA assisted translation method.

But to know for sure, we have to examine the Fixed Disk Parameter Table (FDPT).
The BIOS maintains such a (16 byte) table for each physical drive it supports.
When a BIOS supports translation it uses an enhanced version of this table, the so-called Enhanced Disk Parameter Table (EDPT)
The location of the FDPT or EDPT for the first drive is stored in Interrupt vector 41h and Interrupt vector 46h holds the location of the table for the second drive.
(There are no pointers to the FDPTs for the third and subsequent drives because direct access to these tables is not used anymore. The pointers for the first two drives are however still there to remain compatible with older software. Nowadays, data from a FDPT/EDPT is provided by the BIOS via Interrupt 13h functions 8h and 48h.)

The table below indicates what is stored in the FDPT or EDPT.

Offset	Type	FDPT	EDPT
0-1	Word	Physical Cylinders	Logical Cylinders, limit 1024
2	Byte	Physical Heads	Logical Heads, limit 256
3	Byte	Reserved	A0h Signature, indicating EDPT
4	Byte	Reserved	Physical Sectors/Track
5-6	Word	Precompensation (Obsolete)	Precompensation (Obsolete)
7	Byte	Reserved	Reserved
8	Byte	Drive Control Byte	Drive Control Byte
9-10	Word	Reserved	Physical Cylinders, limit 65536
11	Byte	Reserved	Physical Heads, limit 16
12-13	Word	Landing Zone (Obsolete)	Landing Zone (Obsolete)
14	Byte	Physical Sectors/Track	Logical Sectors/Track, limit 63
15	Byte	Reserved	Checksum

If your BIOS builds an EDPT for a certain drive, it is a translating BIOS!
You can find an EDPT with the WDTBLCHK utility from Western Digital. This very useful program can be downloaded from my webpage. It is a self extracting file called CHKBIOS.EXE.
Or you can get it from <ftp://ftp.wdc.com/drivers/hdutil/chkbios.exe>.

There is a problem however. Most translating BIOSes only build an EDPT i.s.o. a FDPT if the drive is accessed in a translation mode. I therefore use the following trick.

This trick assumes a PC with one < 504 MB harddisk and a BIOS with user definable drive types.

- Enter the BIOS setup and select for the second (non-present) drive a CHS of 2048x16x63.
- If possible select a mode like ECHS, LARGE or LBA for this drive. You probably see the CHS numbers change, indicating the translation.
- Now exit the BIOS setup via "save and exit" and let the computer reboot.
- You probably get an error message because of the missing second drive. Ignore this and continue the boot to the DOS prompt. (If you have Windows 95/98, hit the F8 key when you see "Starting Windows 95/98 ....." and select "Command prompt only" from the menu.)
- Now run the WDTBLCHK utility and check on screen 3-1 if the BIOS build an Enhanced table for the second drive. Look under "INT 46 DRIVE". On the same screen you can also check both the L-CHS and P-CHS as stored in the EDPT. This to confirm a correct translation.
- If this works, repeat the whole procedure with different CHS values to check the boundary conditions of the translation algorithm(s). Note that the **red** figures may bring you into problems as described in "The 2 GB BIOS Limit" below.
  Use 4095x16x63 / 4096x16x63 (2 GB); 8191x16x63 / 8192x16x63 (4 GB) and 16320x16x63 for the 8 GB limit. (The last figure should translate to 1024x255x63 in LBA mode.)

Restore the BIOS setup to its original settings after these tests.
Caution: To be on the safe side, (and to protect the data on your harddisk) it is best to use a boottable floppy with the WD Table Check utility on it. Reboot from this floppy, i.s.o. your harddisk, as long as the BIOS setup is in the 'test' mode.

There is another way to detect a translating BIOS but you need a > 504 MB (actually > 1024 cylinders) drive for that. Connect this drive as slave on the primary IDE-port and, if possible, have the BIOS setup autodetect this drive's geometry. After "save and exit" and reboot use the WD utility to check for an Enhanced table on the second drive.

Finally, if you have a BIOS which supports the IBM/Microsoft Int 13h extensions, you do not need all these tricks because **all** those BIOSes support translation. These BIOSes started to appear in 1995. See "The Int 13h extensions" below.

The 2 GB BIOS Limit

All major harddisk manufacturers have reported about a 2 GB BIOS limit.
It appears that a number of translating BIOSes, manufactured *before* May 1996 have problems translating drives with cylinder values over 4095. This limits the capacity to 2 GB (2015 MB).
To break this limitation, many harddisk manufacturers supply a software solution like Disk Manager or EZ-Drive with their large harddisks.
Alternately, there may be a BIOS upgrade available for your system.

A nice article about this problem and its various solutions is "The other BIOS Limitation!" from Western Digital. Look at <http://www.westerndigital.com/service/tip1196.html>
Details from one of the BIOS manufacturers can be found in Micro Firmware's article "Notes on Installing Hard Drives Larger Than 2 GB". See <http://www.firmware.com/pb4ts/over2gb.htm>

Reported problem scenarios for the affected BIOSes are:

- The BIOS can only see a maximum of 4095 cylinders thereby truncating the usable drive space to 2015 MB
- The BIOS uses only the lower 12 bits of the 16-bit cylinder word thereby **losing 2015 MB** of the drive's capacity when a drive is larger then 2 GB!
- When a cylinder count of over 4095 is entered in the BIOS setup, the BIOS will cause a system lock-up at boot time, making the entire system inaccessible.

Apart from the last scenario, I don't know any other reliable method to detect this 2 GB limit than by hooking up a drive with more then 4095 cylinders. However, you may have found something when using "the trick" for detecting a translating BIOS. (See above)

BIOSes dated May 1996 or later should be free of these problems and support translation up to the Int 13h interface limit of 8 GB.

Related to the 2 GB limit is the Award BIOS harddisk size display limit bug.
I've found that all Award BIOSes dated July 1994 or later correctly support the LBA assisted translation up to the 8 GB limit. There is however a bug in the BIOSes dated before January 1996 that limits the harddisk size display, on the BIOS Setup and boot screens, to 2015 MB.
Whenever a drive is 2016 MB or larger, the display starts to count from zero again. The same happens at 4032 and 6048 MB.
This looks a lot like the above mentioned 2 GB limit but is actually only a bug in the harddisk size calculation routine, and it doesn't affect the BIOS support for these large drives.
For these Award v4.50(P)(G) BIOSes, just use the HDD AUTO DETECTION feature to Setup the drive, select the option with LBA at the end, and disregard the incorrect HD size display.

The 4 GB Limit

Yes, there is another limit! This is actually an Operating System issue but the appropriate way to deal with this problem is to account for it in the system BIOS.
It appears that DOS and Windows 95/98 are limited to 255 Heads.
A translated geometry of 256 Heads will therefore create a problem.
This can happen when a drive has 16 Heads and more than 8192 Cylinders (> 4032 MB).

As indicated under "The translating BIOS" the LBA assisted method should translate to 255 i.s.o. 256 Heads when a drive is larger than 4032 MB.
If this is not the case, then the bit-shifting translation (select ECHS or LARGE) should be used with the following workaround:

1. Enter the CHS values of the drive in CMOS setup or do a "HDD autodetect" and do not select a translation mode yet
2. Adjust the number of heads from 16 to 15
3. Multiply the number of cylinders by 16/15 (round down to a whole number)
4. Adjust the number of cylinders to this higher amount
5. Check or select a bit-shifting translation mode
6. Save and exit CMOS setup and partition and format the drive.

With this workaround, a translated geometry of 15 X 16 = 240 Heads will be used.
This limits the maximum L-CHS to 1024x240x63 which is equivalent to 7560 MB.

For more information read the excellent article "Issues with Hard Drives Over 4 GB".
Look at <http://www.firmware.com/pb4ts/over4gb.htm>

The Int 13h extensions - Breaking the 8 GB barrier

With the rate in which the harddisk technology is progressing, we are now faced with EIDE drives exceeding the 8064 MB limit of the Int 13h interface.
The only way to break this limit is to ditch the CHS system in favor of a direct LBA interface.
The SCSI drive technology uses this kind of LBA interface already for years.
LBA works with a 64-bit sector address, so we can (theoretically) access the staggering amount of 8,796,093,022,208 GB! Due to limitations of the ATA interface, only the lower 28 bits of the LBA address can used by an EIDE drive resulting in a, still formidable, limit of 128 GB.

Windows 95/98 is ready for this because it already uses LBA internally.
Except in Safe or Compatibility Mode, the protected mode diskdriver takes over the BIOS Int 13h interface and can access a drive directly in LBA.

To remain compatible with all the Operating Systems that still use the CHS system to call the BIOS (including Windows 95/98 at boottime), we need an extension on, rather than a replacement of, the Int 13h BIOS interface.
This is where the IBM/Microsoft Int 13h extensions come in.
This specification adds new functions to the Int 13h interface. These new functions are fundamentally different from the conventional Int 13h interface and allow the BIOS to be called directly with the required LBA.

A BIOS with the IBM/Microsoft Int 13h extensions supports both LBA capable and LBA non-capable drives. To do this, such a BIOS must support all of the following translations.
Traditional Int 13h functions:

- direct CHS addressing (Normal mode)
- L-CHS to P-CHS translation
- L-CHS to LBA translation

Extended Int 13h functions:

- direct LBA addressing
- LBA to P-CHS translation

Because BIOSes with the IBM/Microsoft Int 13h extensions also support at least four (sometimes eight) drives, including removable drives, you will find them in most modern PC's.
Most BIOSes dated January 1998 or later will support the Int 13h extensions.
To detect such a BIOS, you can download the EXTBIOS utility from my webpage.

Just as with the 504 MB barrier, you need one of these solutions to break the 8 GB barrier if you do not have the Int 13h extensions:
1. A BIOS upgrade
2. Add-in card with an Int 13h extension BIOS (this takes over the Int 13h interface only)
3. Software like Disk Manager or EZ-Drive.

Now that the BIOS is ready for it, what else do we need to break the 8 GB barrier?
Well, an Operating System capable of addressing a drive in LBA, either directly in protected mode or via the extended Int 13h BIOS interface. Windows 95 (all versions), Windows 98, Windows NT 4.0 (with SP4), Linux, and OS/2 Warp 3 and 4 (on HPFS) are fully equipped for this.
(So DOS 6.x, Windows 3.x, and Windows NT 3.5x and earlier versions are limited to 8 GB.)

Last but not least, we need a partition utility capable of creating partitions above the 8 GB boundary which the OS can see. The version of FDISK supplied with these Operating Systems is able to do this with the aid of new partition types 0Eh and 0Fh (FAT16) or 0Bh and 0Ch (FAT32; Win95b-OSR2 / Win98 only). Except for primary partitions below the 8 GB boundary, these new FDISK versions automatically select the new partition types, i.s.o. the old ones, when a BIOS with Int 13h extensions is detected.
Microsoft Knowledge Base article Q69912 gives a brief description of the various partition types. Look at <http://www.microsoft.com/kb/articles/q69/9/12.htm>
A nice article about the various versions of FDISK and their limitation is "Notes on DOS FDISK Command". Look at <http://www.firmware.com/support/bios/fdisk.htm>
Third party partition managers like "Partition Magic" from PowerQuest <http://www.powerquest.com> or "Partition Commander" from V Communications <http://www.v-com.com> can also go above the 8 GB boundary, and make the job of creating, re-sizing, and moving partitions, and selecting partition types much easier. And all this without loosing data!

Needless to say that the new partition types are invisible to DOS and that compatibility has to be sacrificed in the name of progress.

More information on the net

Possibly the most extensive source of information on this subject is
The Enhanced IDE/Fast-ATA/ATA-2 FAQ by John Wehman and Peter den Haan.
“Peter den Haan’s EIDE storage page” at <http://thef-nym.sci.kun.nl/~pieterh/storage.html> is the place to look for this FAQ. This page contains loads of links to other sites as well.

A good starting point for finding a BIOS upgrade is "Wim's BIOS page at"
<http://www.ping.be/bios/>
Start with the FAQ and then work your way through the other pages.

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