VT82C586B

PIPC
PCI Integrated Peripheral Controller

PC97 Compliant PCI-to-ISA Bridge with ACPI, Distributed DMA, Plug and Play, Master Mode PCI-IDE Controller with UltraDMA-33 USB Controller, Keyboard Controller, and RTC

Revision 1.0
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VIA TECHNOLOGIES, INC.

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Offices:

USA Office:
5020 Brandin Court
Fremont, CA 94538
USA
Tel: (510) 683-3300
Fax: (510) 683-3301

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 218-5452
Fax: (886-2) 218-5453

Online Services:

Home Page: http://www.via.com.tw/
FTP Server: ftp.via.com.tw
BBS: 886-2-2185208

REVISION HISTORY

Document Release	Date	Revision	Initials
Revision 0.1	10/13/96	Initial release for 586A	DH
Revision 0.5	12/23/96 reprinted 1/8/97 to fix Acrobat PDF file size problem	Update to reflect 586B: • Updated pin definitions: Pins 18,31,33,58,60,131,133 (removed EXTSMI2-7 & DACEN) Pins 77-78,80-83,85-86 (added GPI8-15 and GPO8-15) Pins 94,87-88,92,136 (changed to GPIO0-4 and added alternate functions) Pins 90,106,137 (added MIRQ0, MIRQ1, and MIRQ2 functions) Pins 91,93,103,107 (changed to PWRBTN#, RI#, VDD-5VSB, PWRON) Pins 113-114,116-119,121-122 (added GPI, GPO, and EXTSMI functions) Fixed doc error DACK0-7 pin names changed to active low (DACK0-7#) Removed options: IRQ12 (pin 137), strap (pin 48), RTCAS (pin 94) • Updated register definitions Removed VIA-specific port A8/A9 registers Updated function 0 Rx5-4[3], Rx7-6[13], Rx41[0-4,6-7], Rx42[4-7], Rx44, Rx46[2-4], Rx47[3], Rx48[3], Rx4A[4-6], Removed Rx50 (MDRQ) **Rx55[7-4] change PIRQD# to MIRQ1, Rx56 swap A/B, Rx57 swap C/D** Added 58-5B for PnP, XD, KBC/RTC config; added 60-6F for DDMA ctrl Removed power mgmt regs 80-94 & added function 3 ACPI Power Mgmt • Straps: moved 95-96 to 5A, allow RW after powerup, removed strap XD3 • Expanded CMOS RAM: added ports 72-75 & table 5 CMOS Reg Summary • Added Power Management Subsystem Overview • Incorporated App Note #53 APM-Compliant Pwr Mgmt Model of 82C586A • Added AC Timing Section with IDE Interface Timing Diagrams & Specs	DH
Revision 1.0	5/13/97	• Overview Changes: Added System Block Diagram • Pin Function Changes: Pin 90 added alternate function "POS" output **(3040F and 3041 silicon)** Pin 106 added alternate function "IRQ8#" input **(3040F and 3041 silicon)** Pin 137 added alternate function "SDDIR" output **(3041 only silicon)** • Register Definition Changes: Fixed typos: Port 75 note, Fn0 Rx48[3], Rx55-57[7:0]; Fn1 Rx4[7]; Fn2 Rx3C-3D; Fn3 Rx26[9], Rx2F, Rx62-63, Table 7 Added missing register: Function 0 Rx59[3] MIRQ Pin Config Register Function 0 PCI-to-ISA Bridge **(3041 only silicon)** Rx08[7:0] (changed) Revision Code Register Rx2C[31:0] (new) Subsystem ID Register (read) Rx41[0] (changed) ISA Test Mode Register Rx46[7:5] and Rx48[5:4] (new) Misc Control Registers 1 and 3 Rx5C[0] (new) DMA Control Register Rx70[31:0] (new) Subsystem ID Register (write) Function 1 IDE Controller **(3041 only silicon)** Rx43[7] (new) FIFO Configuration Register Rx44[1:0] (new) Misc Control Register 1 Function 3 Power Management **(3040F and 3041 silicon)** Rx04[0] (moved to Rx41[7]) Command Register Rx08[7:0] (changed) Revision ID Register Rx10[4:1], Rx14 (changed) Processor Control and Processor Level 2 Rx20[31:0] (moved to Rx48) I/O Base Address Register Power Management I/O**(3040F and 3041 silicon)** Rx40[6:5] (new) GPIO Direction Control Register • Electrical Spec Changes: Added PCI Cycle Timing • Mechanical Spec Changes: Added marking specs for 3040E/F, 3041 silicon	DH

Incorrect Change →

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VT82C586B PIPC
PCI INTEGRATED PERIPHERAL CONTROLLER

PC97 COMPLIANT PCI-TO-ISA BRIDGE WITH ACPI, DISTRIBUTED DMA, PLUG AND PLAY, MASTER MODE PCI IDE CONTROLLER WITH ULTRADMA-33, USB CONTROLLER, KEYBOARD CONTROLLER, AND REAL TIME CLOCK

- **PC97 Compliant PCI to ISA Bridge**
  - Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated USB Controller with root hub and two function ports
  - Integrated master mode enhanced IDE controller with enhanced PCI bus commands and UltraDMA-33 extensions
  - PCI-2.1 compliant with delay transaction
  - Eight double-word line buffer between PCI and ISA bus
  - One level of PCI to ISA post-write buffer
  - Supports type F DMA transfers
  - Distributed DMA support for ISA legacy DMA across the PCI bus
  - Fast reset and Gate A20 operation
  - Edge trigger or level sensitive interrupt
  - Flash EPROM, 2MB EPROM and combined BIOS support
  - Programmable ISA bus clock
  - Supports external IOAPIC interface for symmetrical multiprocessor configurations
- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - Combine with VT82C585VPX/587VP for a complete 75MHz 6x86 / PCI / ISA system (Apollo VPX)
  - Combine with VT82C595 for a complete Pentium / PCI / ISA system (Apollo VP2)
  - Combine with VT82C685/687 for a complete Pentium-Pro /PCI / ISA system (Apollo P6)
  - Combine with VIA Apollo-AGP and Apollo Pro chipsets for new high-performance / enhanced-functionality systems
  - Inter-operable with other Intel or non-Intel Host-to-PCI bridges for a complete PC97 compliant PCI/ISA system
- **Enhanced Master Mode PCI IDE Controller with Extension to UltraDMA-33**
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
  - Sixteen levels (doublewords) of prefetch and write buffers
  - Interlaced commands between two channels
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support

- **Universal Serial Bus Controller**
  - USB v.1.0 and Intel Universal HCI v.1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Root hub and two function ports
  - Integrated physical layer transceivers with over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **Sophisticated PC97-Compatible Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant (all required features plus extensions for most efficient desktop power management)
  - APM v1.2 Compliant
  - Supports soft-off (suspend to disk) and power-on suspend with hardware automatic wake-up
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Dedicated input pin for external modem ring indicator for system wake-up
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Normal, doze, sleep, suspend and conserve modes
  - System event monitoring with two event classes
  - Five multi-purpose I/O pins plus support for up to 16 general purpose input ports and 16 output ports
  - I^2C serial bus support for JEDEC-compatible DIMM identification and on-board-device power control
  - Seven external event input ports with programmable SMI condition
  - Primary and secondary interrupt differentiation for individual channels
  - Clock throttling control
  - Multiple internal and external SMI sources for flexible power management models
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Three steerable interrupt channels for on-board plug and play devices
  - Microsoft Windows 95™ and plug and play BIOS compliant
- **Pin-compatible upgrade from VT82C586 and VT82C586A for existing designs**
- **Built-in Nand-tree pin scan test capability**
- **0.5um mixed voltage, high speed and low power CMOS process**
- **Single chip 208 pin PQFP**

OVERVIEW

The VT82C586B PIPC (PCI Integrated Peripheral Controller) is a high integration, high performance and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC97-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C586B includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C586B also supports the emerging UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-95 compliant.

b) Universal Serial Bus controller that is USB v1.0 and Universal HCI v1.1 compliant. The VT82C586B includes the root hub with two function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

c) Keyboard controller with PS2 mouse support.

d) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm and other enhancements for compatibility with the ACPI standard.

e) Notebook-class power management functionality that is compliant with ACPI and legacy APM requirements. Two types of sleep states (soft-off and power-on-suspend) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling (Intel processor protocol), modular power control, hardware- and software-based event handling, general purpose IO, chip select and external SMI.

f) Distributed DMA capability for support of ISA legacy DMA over the PCI bus.

g) Plug and Play controller that allows complete steerability of all PCI interrupts to any interrupt channel. Three additional steerable interrupt channels are provided to allow plug and play and reconfigurability of on-board peripherals for Windows 95 compliance.

h) External IOAPIC support for Intel-compliant symmetrical multiprocessor systems.

The VT82C586B also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.1 specification, the VT82C586B supports delayed transactions so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

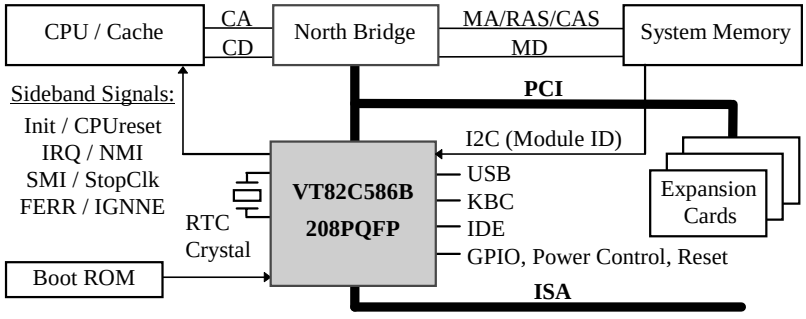

Figure 1. PC System Configuration Using the VT82C586B

PINOUTS

Figure 2. Pin Diagram

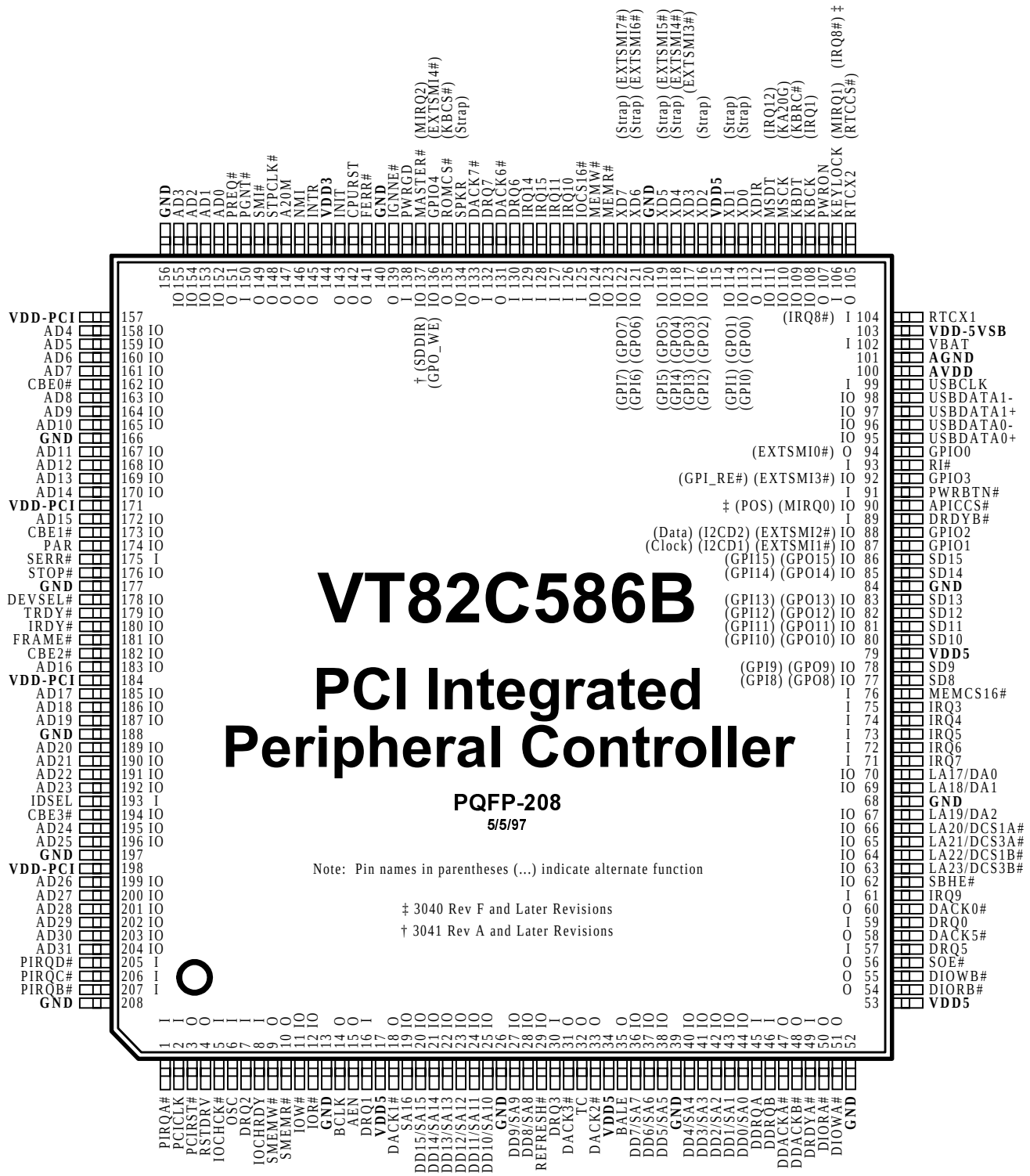

Table 1. Pin Descriptions

CPU Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
CPURST	142	O	**CPU Reset.** The VT82C586B asserts CPURST to reset the CPU during power-up.
INTR	145	O	**CPU Interrupt.** INTR is driven by the VT82C586B to signal the CPU that an interrupt request is pending and needs service.
NMI	146	O	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT82C586B generates an NMI when either SERR# or IOCHK# is asserted.
INIT	143	O	**Initialization.** The VT82C586B asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
STPCLK#	148	O	**Stop Clock.** STPCLK# is asserted by the VT82C586B to the CPU in response to different Power-Management events.
SMI#	149	O	**System Management Interrupt.** SMI# is asserted by the VT82C586B to the CPU in response to different Power-Management events.
FERR#	141	O	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU.
IGNNE#	139	O	**Ignore Numeric Error.** This pin is connected to the “ignore error” pin on the CPU.

PCI Bus Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
PCLK	2	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.
FRAME#	181	B	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
AD[31:0]	204-199, 196-195, 192-189, 187-185, 183, 172, 170-167, 165-163, 161-158, 155-152	B	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
C/BE[3:0]#	194, 182, 173, 162	B	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
IRDY#	180	B	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	179	B	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	176	B	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	178	B	**Device Select.** The VT82C586B asserts this signal to claim PCI transactions through positive or subtractive decoding.
PAR	174	B	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	175	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT82C586B can be programmed to generate an NMI to the CPU.
IDSEL	193	I	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write cycles.
PIRQA-D#	1, 207-205	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PCI Slot 1: PIRQA# INTA#, PIRQB# INTB#, PIRQC# INTC#, PIRQD# INTD# PCI Slot 2: PIRQA# INTB#, PIRQB# INTC#, PIRQC# INTD#, PIRQD# INTA# PCI Slot 3: PIRQA# INTC#, PIRQB# INTD#, PIRQC# INTA#, PIRQD# INTB# PCI Slot 4: PIRQA# INTD#, PIRQB# INTA#, PIRQC# INTB#, PIRQD# INTC#
PREQ#	151	O	**PCI Request.** This signal goes to the North Bridge to request the PCI bus.
PGNT#	150	I	**PCI Grant.** This signal is driven by the North Bridge to grant PCI access to the VT82C586B.

ISA Bus Control			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
SA[15:0] / DD[15:0]	20-25, 27-28, 36-38, 40-44	B	**System Address Bus / IDE Data Bus**
SA16	19	B	**System Address Bus**
LA23/DCS3B#, LA22/DCS1B#, LA21/DCS3A#, LA20/DCS1A#, LA[19:17] / DA[2:0]	63-67, 69-70	B	**Multifunction Pins** **ISA Bus Cycles:** Address: The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA bus up to 16MBytes. **PCI IDE Cycles:** Chip Select: DCS1A# is for the ATA command register block and corresponds to CS1FX# on the primary IDE connector. DCS3A# is for the ATA command register block and corresponds to CS3FX# on the primary IDE connector. DCS1B# is for the ATA command register block and corresponds to CS17X# on the primary IDE connector. DCS3B# is for the ATA command register block and corresponds to CS37X# on the primary IDE connector. Disk Address: DA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SD[15:8] / GPI[15:8] / GPO[15:8]	86-85, 83-80, 78-77	B	**System Data.** SD[15:8] provide the high order byte data path for devices residing on the ISA bus. These pins also function as **General Purpose Inputs** 15-8 if the GPIO3_CFG bit is low (pin 92 becomes GPI_RE# for enabling external inputs onto the SD pins using an external buffer). These pins also function as **General Purpose Outputs** 15-8 if the GPIO4_CFG bit is low (pin 136 becomes GPO_WE for control of an external latch).
SBHE#	62	B	**System Byte High Enable.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles.
IOR#	12	B	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus.
IOW#	11	B	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus.
MEMR#	123	B	**Memory Read.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus.
MEMW#	124	B	**Memory Write.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
SMEMR#	10	O	**Standard Memory Read.** SMEMR# is the command to a memory slave, under 1MB, which indicates that it may drive data onto the ISA data bus
SMEMW#	9	O	**Standard Memory Write.** SMEMW# is the command to a memory slave, under 1MB, which indicates that it may latch data from the ISA data bus.
BALE	35	O	**Bus Address Latch Enable.** BALE is an active high signal asserted by the VT82C586B to indicate that the address (SA[19:0], LA[23:17] and the SBHE# signal) is valid
IOCS16#	125	I	**16-Bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
MEMCS16#	76	I	**Memory Chip Select 16.** ISA slaves that are 16-bit memory devices drive this line low to indicate they support 16-bit memory bus cycles.
IOCHCK#	5	I	**I/O Channel Check.** When this signal is asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA Bus.
IOCHRDY	8	I	**I/O Channel Ready.** Devices on the ISA Bus negate IOCHRDY to indicate that additional time (wait states) is required to complete the cycle.

ISA Bus Control (continued)			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
REFRESH#	29	B	**Refresh.** As an output REFRESH# indicates when a refresh cycle is in progress. As an input REFRESH# is driven by 16-bit ISA Bus masters to indicate refresh cycle.
AEN	15	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles.
IRQ15, 14, 11-9, 7-3	128-129, 127-126, 61, 71-75	I	**Interrupt Request.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU.
DRQ7-5, 3-0	132, 130, 57, 30, 7, 16, 59	I	**DMA Request.** The DRQ lines are used to request DMA services from the VT82C586B's DMA controller.
DACK7:5, 3-0#	133, 131, 58, 31, 33, 18, 60	O	**Acknowledge.** The DACK# output lines indicate a request for DMA service has been granted.
TC	32	O	**Terminal Count.** The VT82C586B asserts TC to DMA slaves as a terminal count indicator.
MASTER#	(see below)	I	**ISA Master Request.** (see below pin 137)
SPKR / Power-up Strap	134	B	**Multifunction Pin** Normal Operation: **Speaker Drive.** The SPKR signal is the output of counter 2. Power-up Strapping: **0/1 = Fixed/flexible IDE I/O base**

On Board Plug and Play

Signal Name	Pin No.	I/O	Signal Description
MIRQ0 / APICCS# / POS (3040F)	90	I O O	**Multifunction Pin** (see PCI Configuration Register Function 0 Rx59[3,0]) **MIRQ0.** Steerable interrupt request input for on-board devices. **APICCS#**. Chip select for external IOAPIC chip for symmetric multiprocessor implementations. **POS.** Power-On Suspend Status Output (see Function 0 Rx59 bit-3). This function was introduced in rev F of the 3040 silicon and is not available in earlier chips. Rx59[3] Rx59[0] Pin Function 0 0 MIRQ0 (input) 0 1 APICCS# (output) 1 0 -illegal- 1 1 POS (output)
MIRQ1 / KEYLOCK / IRQ8# (3040F)	106	I I I	**Multifunction Pin** (see PCI Configuration Register Function 0 Rx59[1] & Rx48[4]) **MIRQ1.** Steerable interrupt request input for on-board devices. **KEYLOCK.** Keyboard lock input. **IRQ8#.** Interrupt input for external RTC. This function was introduced in revision F of the 3040 silicon and is not available in earlier chips. Rx48[4] Rx59[1] Pin Function 0 0 MIRQ1 (input) 0 1 KEYLOCK (input) 1 0 -illegal- 1 1 IRQ8# (input) (see also Rx5A[2] and table below). With this setting, Rx57[3:0] must be set to 0 (MIRQ1 routing) Rx5A[2] Rx48[4] Pin Function 0 0 External RTC - IRQ8# input on pin 104 0 1 External RTC - IRQ8# input on pin 106 1 x Internal RTC - IRQ8# input not required
MIRQ2 / MASTER# / SDDIR (3041A)	137	I I O	**Multifunction Pin** (see PCI Configuration Register Function 0 Rx59[2] & Rx48[5]) **MIRQ2.** Steerable interrupt request input for on-board devices. **MASTER#.** ISA Master Request indicator. This pin also serves as the direction control for the IDE interface DD / SA transceivers (see SOE#). **SDDIR.** This pin may be programmed to serve as a direction control for the IDE interface DD / SA transceivers (see SOE#) separate from MASTER#. This function was introduced in revision A of the 3041 silicon and not available in earlier chips. Rx48[5] Rx59[2] Pin Function 0 0 MASTER# (input) 0 1 MIRQ2 (input) 1 0 -illegal- 1 1 SDDIR (output)

UltraDMA-33 Enhanced IDE Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
DRDYA# / DDMARDYA# / DSTROBEA	49	I	EIDE Mode: **I/O Channel Ready A.** Primary channel device ready indicator UltraDMA Mode: **Device DMA Ready A**. Primary channel output flow control The device may assert DDMARDY# to pause output transfers **Device Strobe A**. Primary channel input data strobe (both edges) The device may stop DSTROBE to pause input data transfers
DRDYB# / DDMARDYB# / DSTROBEB	89	I	EIDE Mode: **I/O Channel Ready B.** Secondary channel device ready UltraDMA Mode: **Device DMA Ready B**. Secondary channel output flow control The device may assert DDMARDY# to pause output transfers **Device Strobe B**. Secondary channel input strobe (both edges) The device may stop DSTROBE to pause input data transfers
DIORA# / HDMARDYA# / HSTROBEA	50	O	EIDE Mode: **Device I/O Read A.** Primary channel device read strobe UltraDMA Mode: **Host DMA Ready A**. Primary channel input flow control The host may assert HDMARDY# to pause input transfers **Host Strobe A**. Primary channel output data strobe (both edges) The host may stop HSTROBE to pause output data transfers
DIORB# / HDMARDYB# / HSTROBEB	54	O	EIDE Mode: **Device I/O Read B.** Secondary channel device read strobe UltraDMA Mode: **Host DMA Ready B**. Secondary channel input flow control The host may assert HDMARDY# to pause input transfers **Host Strobe B**. Secondary channel output strobe (both edges) The host may stop HSTROBE to pause output data transfers
DIOWA# / STOPA	51	O	EIDE Mode: **Device I/O Write A.** Primary channel device write strobe UltraDMA Mode: **Stop A**. Primary channel stop transfer: asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
DIOWB# / STOPB	55	O	EIDE Mode: **Device I/O Write B.** Secondary channel device write strobe UltraDMA Mode: **Stop B**. Secondary channel stop transfer: asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SOE#	56	O	**System Address Transceiver Output Enable.** This signal controls the output enables of the 245 transceivers that interface the DD[15:0] signals to SA[15:0]. The transceiver direction controls are driven by MASTER# with DD[15-0] connected to the “A” side of the transceivers and SA[15-0] connected to the “B” side.
DDRQA	45	I	**Device DMA Request A.** Primary channel DMA request
DDRQB	46	I	**Device DMA Request B.** Secondary channel DMA request
DDACKA#	47	O	**Device DMA Acknowledge A.** Primary channel DMA acknowledge
DDACKB#	48	O	**Device DMA Acknowledge B.** Secondary channel DMA acknowledge

Note: Refer to the ISA bus interface pin descriptions for remaining IDE interface pin descriptions (the IDE address, data, and drive select pins are multiplexed with the ISA bus LA and SA pins). Also, the MASTER# pin description may be found in the "On Board Plug and Play" pin group (DD / SA transceiver direction control).

XD Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
XD7-0, EXTSMI7-3#, GPI7-0, GPO7-0, Power-up Straps	122 121 119 118 117 116 114 113	B	**Multifunction Pins** **X-bus Data Bus.** For connection to external X-Bus devices (e.g. BIOS ROM) **External SMI Inputs.** External SCI/SMI ports. **General Purpose Inputs.** GPIO3_CFG bit low (pin 92 = GPI_RE#) **General Purpose Outputs.** GPIO4_CFG bit low (pin 136 = GPO_WE) **Power-up Strap Option Inputs.** (see Configuration Register Offset 5Ah) XD0: 0/1 - Disable/enable internal KBC XD1: 0/1 - Disable/enable internal PS/2 Mouse XD2: 0/1 - Disable/enable internal RTC XD4~XD7: RP13~RP16 for internal KBC
XDIR	112	O	**X-Bus Data Direction.** XDIR is tied directly to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA-Bus data (the output enable of the transceiver should be grounded). SD0-7 connect to the "A" side of the transceiver and XD0-7 connect to the "B" side. XDIR high indicates that SD0-7 drives XD0-7.
ROMCS# / KBCS#	135	O	**Multifunction Pin. ROM Chip Select / Keyboard Controller Chip Select.** ISA memory cycle: **ROMCS#.** Chip Select to the BIOS ROM. ISA I/O cycle: **KBCS#.** Chip Select to the external keyboard controller.

General Purpose I/O			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
GPIO0 / EXTSMI0#	94	B	**General Purpose I/O 0**: General Purpose I/O with external SCI/SMI capability. This pin sits on the VDD-5VSB power plane and is available even under soft-off state.
GPIO1 / EXTSMI1# / I2CD1 (Clock)	87	B	**General Purpose I/O 1**: General Purpose I/O with external SCI/SMI capability. Can be used along with pin 88 as an I^2C pair (by software convention this pin is defined as clock).
GPIO2 / EXTSMI2# / I2CD2 (Data)	88	B	**General Purpose I/O 2**: General Purpose I/O with external SCI/SMI capability. Can be used along with pin 87 as an I^2C pair (by software convention this pin is defined as data).
GPIO3 / EXTSMI3# / GPI_RE#	92	B	**Multifunction Pin** (per GPIO3 Configuration Bit: Function 3 Rx40 bit-6) GPIO3 Configuration bit high: **General Purpose I/O 3**: General Purpose I/O with external SCI/SMI capability. GPIO3 Configuration bit low: **Read Enable for General Purpose Inputs**: Connects to the output enable (OE# pin) of the external 244 buffers whose data pins connect to SD15-8 and XD7-0 for GPI15-0.
GPIO4 / EXTSMI4# / GPO_WE	136	B	**Multifunction Pin** (per GPIO4 Configuration Bit: Function 3 Rx40 bit-7) GPIO4 Configuration bit high: **General Purpose I/O 4**: General Purpose I/O with external SCI/SMI capability. GPIO4 Configuration bit low: **Write Enable for General Purpose Outputs**: Connects to the latch enable (LE pin) of the external 373 latches whose data pins connect to SD15-8 and XD7-0 for GPO15-0.

Universal Serial Bus Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
USBDATA0+	95	B	**USB Port 0 Data +**
USBDATA0-	96	B	**USB Port 0 Data -**
USBDATA1+	97	B	**USB Port 1 Data +**
USBDATA1-	98	B	**USB Port 1 Data -**
USBCLK	99	I	**USB Clock.** Clock input for Universal Serial Bus interface

Keyboard Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
KBCK / KA20G	108	B	**Multifunction Pin.** Function depends on enable/disable of internal KBC. Internal KBC enabled: **Keyboard Clock.** Clock to keyboard interface. Internal KBC disabled: **Gate A20:** Gate A20 output from external KBC
KBDT / KBRC#	109	B	**Multifunction Pin.** Function depends on enable/disable of internal KBC. Internal KBC enabled: **Keyboard Data.** Data to keyboard interface. Internal KBC disabled: **Keyboard Reset:** Reset input from external KBC.
MSCK / IRQ1	110	B	**Multifunction Pin.** Function depends on enable/disable of internal KBC. PS/2 mouse enabled: **Mouse Clock.** Clock to PS/2 mouse interface. PS/2 mouse disabled and internal KBC disabled: **Interrupt Request 1.** IRQ 1 input from external KBC.
MSDT / IRQ12	111	B	**Multifunction Pin.** Function depends on enable/disable of internal KBC. PS/2 mouse enabled: **Mouse Data.** Data to PS/2 mouse interface. PS/2 mouse disabled: **Interrupt Request 12.** IRQ 12 input from external KBC
A20M	147	O	**A20 Mask.** Direct connect A20 mask on CPU.
KEYLOCK / MIRQ1 / IRQ8#	106	I	**Keyboard Lock.** Keyboard lock signal for internal keyboard controller. (For reference only - see pin 106 description in "Onboard Plug and Play" section)

Internal Real Time Clock			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
RTCX1 / IRQ8#	104	I	**Multifunction Pin** Internal RTC enabled: **RTC Crystal Input**: 32.768Khz crystal or oscillator input. Internal RTC disabled: **Interrupt Request 8**: IRQ8 input from external RTC Rx5A[2] Rx48[4] Pin Function 0 0 External RTC - IRQ8# input on pin 104 0 1 External RTC - IRQ8# input on pin 106 1 x Internal RTC - IRQ8# input not required
RTCX2 / RTCCS#	105	O	**Multifunction Pin** Internal RTC enabled: **RTC Crystal Output**: 32.768Khz crystal output Internal RTC disabled: **External RTC Chip Select**
VBAT	102	I	**RTC Battery.** Battery input for internal RTC

Resets and Clocks			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
PWRGD	138	I	**Power Good.** Connected to the POWERGOOD signal on the Power Supply.
PCIRST#	3	O	**PCI Reset.** An active low reset signal for the PCI bus. The VT82C586B will generate PCIRST# during power-up or from the control register.
RSTDRV	4	O	**Reset Drive.** RSTDRV is the reset signal to the ISA bus.
BCLK	14	O	**Bus Clock.** ISA bus clock.
OSC	6	I	**Oscillator.** OSC is the 14.31818 MHz clock signal. It is used by the internal Timer.

Power Management			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
PWRBTN#	91	I	**Power Button.** Referenced to VDD-5VSB.
PWRON	107	O	**Power Supply Control.** Powered by VDD-5VSB.
RI#	93	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. Input referenced to VDD-5VSB.

Power and Ground			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
VDD5	17, 34, 53, 79, 115	P	**Power Supply.** 4.75 to 5.25V. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.
VDD-5VSB	103	P	**Power Supply.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be connected to VDD5.
VDD3	144	P	**Power Supply.** This pin should be connected to the same voltage as the CPU I/O circuitry.
VDD_PCI	157, 171, 184, 198	P	**PCI Voltage.** 3.3 or 5V.
AVDD	100	P	**USB Differential Output Power Source**
AGND	101	P	**USB Differential Output Ground**
GND	13, 26, 39, 52, 68, 84, 120, 140, 156, 166, 177, 188, 197, 208	P	**Ground**

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT82C586B. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x nnnn
20-3F	Master Interrupt Controller	0000 0000 001x xxxn
40-5F	Timer / Counter	0000 0000 010x xxnn
60-6F	Keyboard Controller	0000 0000 0110 xnxn
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Spkr Ctrl	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0nnn
78-7F	-available for system use-	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 nnnn
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use-	0000 0000 1001 nnnn
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxn
C0-DF	Slave DMA Controller	0000 0000 110n nnnx
E0-FF	-available for system use-	0000 0000 111x xxxx
100-CF7	-available for system use-	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

Table 3. Registers

Legacy I/O Registers

Port	Master DMA Controller Registers	Default	Acc
00	Channel 0 Base & Current Address		RW
01	Channel 0 Base & Current Count		RW
02	Channel 1 Base & Current Address		RW
03	Channel 1 Base & Current Count		RW
04	Channel 2 Base & Current Address		RW
05	Channel 2 Base & Current Count		RW
06	Channel 3 Base & Current Address		RW
07	Channel 3 Base & Current Count		RW
08	Status / Command		RW
09	Write Request		**WO**
0A	Write Single Mask		**WO**
0B	Write Mode		**WO**
0C	Clear Byte Pointer FF		**WO**
0D	Master Clear		**WO**
0E	Clear Mask		**WO**
0F	Read / Write Mask		RW

Port	Master Interrupt Controller Regs	Default	Acc
20	Master Interrupt Control	—	*
21	Master Interrupt Mask	—	*
20	Master Interrupt Control Shadow	—	**RW**
21	Master Interrupt Mask Shadow	—	**RW**

* RW if shadow registers are disabled

Port	Timer/Counter Registers	Default	Acc
40	Timer / Counter 0 Count		RW
41	Timer / Counter 1 Count		RW
42	Timer / Counter 2 Count		RW
43	Timer / Counter Control		**WO**

Port	Keyboard Controller Registers	Default	Acc
60	Keyboard Controller Data		RW
61	Misc Functions & Speaker Control		RW
64	Keyboard Ctrlr Command / Status		RW

Port	CMOS / RTC / NMI Registers	Default	Acc
70	CMOS Memory Address & NMI Disa		**WO**
71	CMOS Memory Data (128 bytes)		RW
72	CMOS Memory Address		RW
73	CMOS Memory Data (256 bytes)		RW
74	CMOS Memory Address		RW
75	CMOS Memory Data (256 bytes)		RW

NMI Disable is port 70h (CMOS Memory Address) bit-7.
RTC control occurs via specific CMOS data locations (0-0Dh).
Ports 72-73 may be used to access all 256 locations of CMOS.
Ports 74-75 may be used to access CMOS if the internal RTC is disabled.

Port	DMA Page Registers	Default	Acc
87	DMA Page - DMA Channel 0		RW
83	DMA Page - DMA Channel 1		RW
81	DMA Page - DMA Channel 2		RW
82	DMA Page - DMA Channel 3		RW
8F	DMA Page - DMA Channel 4		RW
8B	DMA Page - DMA Channel 5		RW
89	DMA Page - DMA Channel 6		RW
8A	DMA Page - DMA Channel 7		RW

Port	System Control Registers	Default	Acc
92	System Control		RW

Port	Slave Interrupt Controller Regs	Default	Acc
A0	Slave Interrupt Control	—	*
A1	Slave Interrupt Mask	—	*
A0	Slave Interrupt Control Shadow	—	**RW**
A1	Slave Interrupt Mask Shadow	—	**RW**

* RW accessible if shadow registers are disabled

Port	Slave DMA Controller Registers	Default	Acc
C0	Channel 0 Base & Current Address		RW
C2	Channel 0 Base & Current Count		RW
C4	Channel 1 Base & Current Address		RW
C6	Channel 1 Base & Current Count		RW
C8	Channel 2 Base & Current Address		RW
CA	Channel 2 Base & Current Count		RW
CC	Channel 3 Base & Current Address		RW
CE	Channel 3 Base & Current Count		RW
D0	Status / Command		RW
D2	Write Request		**WO**
D4	Write Single Mask		**WO**
D6	Write Mode		**WO**
D8	Clear Byte Pointer FF		**WO**
DA	Master Clear		**WO**
DC	Clear Mask		**WO**
DE	Read / Write Mask		RW

PCI Function 0 Registers - PCI-to-ISA Bridge

Configuration Space PCI-to-ISA Bridge Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0586	RO
5-4	Command	000F	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	01	RO
B	Base Class Code	06	RO
C	-reserved- (cache line size)	00	—
D	-reserved- (latency timer)	00	—
E	Header Type	80	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2F-2C	Subsystem ID Read	00	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	ISA Bus Control	Default	Acc
40	ISA Bus Control	00	RW
41	ISA Test Mode	00	RW
42	ISA Clock Control	00	RW
43	ROM Decode Control	00	RW
44	Keyboard Controller Control	00	RW
45	Type F DMA Control	00	RW
46	Miscellaneous Control 1	00	RW
47	Miscellaneous Control 2	00	RW
48	Miscellaneous Control 3	01	RW
49	-reserved-	00	—
4A	IDE Interrupt Routing	04	RW
4B	-reserved-	00	—
4C	DMA / Master Mem Access Control 1	00	RW
4D	DMA / Master Mem Access Control 2	00	RW
4F-4E	DMA / Master Mem Access Control 3	0300	RW

Offset	Plug and Play Control	Default	Acc
50	-reserved- (do not program)	24	RW
51-53	-reserved-	00	—
54	PCI IRQ Edge / Level Selection	00	RW
55	PnP Routing for External MIRQ0-1	00	RW
56	PnP Routing for PCI INTB-A	00	RW
57	PnP Routing for PCI INTD-C	00	RW
58	PnP Routing for External MIRQ2	00	RW
59	MIRQ Pin Configuration	04	RW
5A	XD Power-On Strap Options	†	RW
5B	Internal RTC Test Mode	00	RW
5C	DMA Control	00	RW
5F-5D	-reserved-	00	—

† Power-up default value depends on external strapping

Offset	Distributed DMA	Default	Acc
61-60	Channel 0 Base Address / Enable	0000	RW
63-62	Channel 1 Base Address / Enable	0000	RW
65-64	Channel 2 Base Address / Enable	0000	RW
67-66	Channel 3 Base Address / Enable	0000	RW
69-68	-reserved-	0000	—
6B-6A	Channel 5 Base Address / Enable	0000	RW
6D-6C	Channel 6 Base Address / Enable	0000	RW
6F-6E	Channel 7 Base Address / Enable	0000	RW

Offset	Miscellaneous	Default	Acc
70	Subsystem ID Write	00	WO
71-7F	-reserved-	00	—

PCI Function 1 Registers - IDE Controller

Configuration Space IDE Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0571	RO
5-4	Command	0080	RO
7-6	Status	0280	**RW**
8	Revision ID	nn	RO
9	Programming Interface	85	**RW**
A	Sub Class Code	01	RO
B	Base Class Code	01	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Base Address - Pri Data / Command	000001F0	RO
17-14	Base Address - Pri Control / Status	000003F4	RO
1B-18	Base Address - Sec Data / Command	00000170	RO
1F-1C	Base Address - Sec Control / Status	00000374	RO
23-20	Base Address - Bus Master Control	0000CC01	**RW**
24-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	0E	RW
3D	Interrupt Pin	00	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space IDE-Specific Registers

Offset	Configuration Space IDE Registers	Default	Acc
40	Chip Enable	08	RW
41	IDE Configuration	02	RW
42	-reserved- (do not program)	09	**RW**
43	FIFO Configuration	3A	RW
44	Miscellaneous Control 1	68	RW
45	Miscellaneous Control 2	00	RW
46	Miscellaneous Control 3	C0	RW
4B-48	Drive Timing Control	A8A8A8A8	RW
4C	Address Setup Time	FF	RW
4D	-reserved- (do not program)	00	**RW**
4E	Sec Non-1F0 Port Access Timing	FF	RW
4F	Pri Non-1F0 Port Access Timing	FF	RW
53-50	UltraDMA33 Extd Timing Control	03030303	RW
54-5F	-reserved-	00	—
61-60	Primary Sector Size	0200	RW
62-67	-reserved-	00	—
69-68	Secondary Sector Size	0200	RW
70-FF	-reserved-	00	—

I/O Registers - IDE Controller

These registers are compliant with the SFF 8038 v1.0 standard. Refer to that specification for additional information.

Offset	IDE I/O Registers	Default	Acc
0	Primary Channel Command	00	RW
1	-reserved-	00	—
2	Primary Channel Status	00	WC
3	-reserved-	00	—
4-7	Primary Channel PRD Table Addr	00	RW
8	Secondary Channel Command	00	RW
9	-reserved-	00	—
A	Secondary Channel Status	00	WC
B	-reserved-	00	—
C-F	Secondary Channel PRD Table Addr	00	RW

PCI Function 2 Registers - USB Controller

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3038	RO
5-4	Command	0000	**RW**
7-6	Status	0200	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	03	RO
B	Base Class Code	0C	RO
C	Cache Line Size	00	RO
D	Latency Timer	16	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	Base Address	00000301	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	04	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	Miscellaneous Control 1	00	**RW**
41	Miscellaneous Control 2	00	**RW**
42-43	-reserved-	00	RO
44-45	-reserved- (test only, do not program)		**RW**
46-47	-reserved- (test)		RO
48-5F	-reserved-	00	—
60	Serial Bus Release Number	10	RO
61-BF	-reserved-	00	—
C1-C0	Legacy Support	2000	**RW**
C2-FF	-reserved-	00	—

I/O Registers - USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	40	RW
11-10	Port 1 Status / Control	0080	**WC**
13-12	Port 2 Status / Control	0080	**WC**

PCI Function 3 Registers - Power Management

Configuration Space Power Management Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3040	RO
5-4	Command	0000	RO
7-6	Status	0280	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00†	RO
A	Sub Class Code	00†	RO
B	Base Class Code	00†	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	RO
E	Header Type	00	RO
F	BIST	00	RO
10-3F	-reserved-	00	—

† The default values for these registers may be changed by writing to offsets 61-63h (see below).

Configuration Space Power Management-Specific Registers

Offset	Power Management	Default	Acc
40	Pin Configuration	00	RW
41	General Configuration	00	RW
42	SCI Interrupt Configuration	00	RW
43	-reserved-	00	—
45-44	Primary Interrupt Channel	0000	RW
47-46	Secondary Interrupt Channel	0000	RW
4B-48	I/O Base Address (256 Bytes)	0000 0001	RW
4F-4C	-reserved-	00	—
53-50	GP Timer Control	0000 0000	RW
54-60	-reserved-	00	—
61	Write value for Offset 9 (Prog Intfc)	00	**WO**
62	Write value for Offset A (Sub Class)	00	**WO**
63	Write value for Offset B (Base Class)	00	**WO**
64-FF	-reserved-	00	—

I/O Space Power Management- Registers

Offset	Basic Control / Status Registers	Default	Acc
1-0	Power Management Status	0000	WC
3-2	Power Management Enable	0000	RW
5-4	Power Management Control	0000	RW
7-6	-reserved-	00	—
B-8	Power Management Timer	0000 0000	RW
F-C	-reserved-	00	—
Offset	**Processor Registers**	**Default**	**Acc**
13-10	Processor Control	0000 0000	RW
14	Processor LVL2	00	**RO**
15	Processor LVL3	00	**RO**
1F-16	-reserved-	00	—
Offset	**General Purpose Registers**	**Default**	**Acc**
21-20	General Purpose Status	0000	**WC**
23-22	General Purpose SCI Enable	0000	RW
25-24	General Purpose SMI Enable	0000	RW
27-26	General Purpose Power Supply Ctrl	0200	RW
Offset	**Generic Registers**	**Default**	**Acc**
29-28	Global Status	0000	**WC**
2B-2A	Global Enable	0000	RW
2D-2C	Global Control	00	RW
2E	-reserved-	00	—
2F	SMI Command	00	RW
33-30	Primary Activity Detect Status	0000 0000	**WC**
37-34	Primary Activity Detect Enable	0000 0000	RW
3B-38	GP Timer Reload Enable	0000 0000	RW
3F-3C	-reserved-	00	—
Offset	**General Purpose I/O Registers**	**Default**	**Acc**
41-40	GPIO Direction Control	0000	RW
43-42	GPIO Port Output Value	0000	RW
45-44	GPIO Port Input Value	input	**RO**
47-46	GPO Port Output Value	0000	RW
49-48	GPI Port Input Value	input	**RO**
FF-4A	-reserved-	00	—

Configuration Space I/O

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address .....RW

31 Configuration Space Enable
- 0 Disabled .....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific DWORD in the device's configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data .....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Port 61 - Misc Functions & Speaker Control .....RW

7 **Reserved** ..... always reads 0

6 **IOCHCK# Active** ..... RO
This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK#. IOCHCK# generates NMI to the CPU if NMI is enabled.

5 **Timer/Counter 2 Output** ..... RO
This bit reflects the output of Timer/Counter 2 without any synchronization.

4 **Refresh Detected** ..... RO
This bit toggles on every rising edge of the ISA bus REFRESH# signal.

3 **IOCHCK# Disable** ..... RW
- 0 Enable IOCHCK# assertions.....default
- 1 Force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6

2 **Reserved** ..... RW, default=0

1 **Speaker Enable**..... RW
- 0 Disable .....default
- 1 Enable Timer/Ctr 2 output to drive SPKR pin

0 **Timer/Counter 2 Enable**..... RW
- 0 Disable .....default
- 1 Enable Timer/Counter 2

Port 92h - System Control..... RW

7-6 **Hard Disk Activity LED Status**
- 0 Off ..... default
- 1-3 On

5-4 **Reserved** ..... always reads 0

3 **Power-On Password Bytes Inaccessable** .. default=0

2 **Reserved** ..... always reads 0

1 **A20 Address Line Enable**
- 0 A20 disabled / forced 0 (real mode) ..... default
- 1 A20 address line enabled

0 **High Speed Reset**
- 0 Normal
- 1 Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60.

A "Control" register is also available. It is accessable by writing commands 20h / 60h to the command port (port 64h); The control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" with specific pins dedicated to certain functions and other pins available for general purpose I/O. Specific commands are provided to set these pins high and low. All outputs are "open-collector" so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port	Lo Code	Hi Code
0	P10 - Keyboard Data In	B0	B8
1	P11 - Mouse Data In	B1	B9
2	P12 - Turbo Pin (PS/2 mode only)	B2	BA
3	P13 - user-defined	B3	BB
4	P14 - user-defined	B6	BE
5	P15 - user-defined	B7	BF
6	P16 - user-defined	–	–
7	P17 - undefined	–	–

Bit	Output Port	Lo Code	Hi Code
0	P20 - SYSRST (1=execute reset)	–	–
1	P21 - GATEA20 (1=A20 enabled)	–	–
2	P22 - Mouse Data Out	B4	BC
3	P23 - Mouse Clock Out	B5	BD
4	P24 - Keyboard OBF Interrupt (IRQ1)	–	–
5	P25 - Mouse OBF Interrupt (IRQ 12)	–	–
6	P26 - Keyboard Clock Out	–	–
7	P27 - Keyboard Data Out	–	–

Bit	Test Port	Lo Code	Hi Code
0	T0 - Keyboard Clock In	–	–
1	T1 - Mouse Clock In	–	–

Note: Command code C0h transfers input port data to the output buffer. Command code D0h copies output port values to the output buffer. Command code E0h transfers test input port data to the output buffer.

Port 60 - Keyboard Controller Input Buffer ..... WO

Only write to port 60h if port 64h bit-1 = 0 (1=full).

Port 60 - Keyboard Controller Output Buffer .....RO

Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Port 64 - Keyboard / Mouse Status ..... RO

0 Keyboard Output Buffer Full
- 0 Keyboard Output Buffer Empty..... default
- 1 Keyboard Output Buffer Full

1 Input Buffer Full
- 0 Input Buffer Empty..... default
- 1 Input Buffer Full

2 System Flag
- 0 Power-On Default..... default
- 1 Self Test Successful

3 Command / Data
- 0 Last write was data write ..... default
- 1 Last write was command write

4 Keylock Status
- 0 Locked
- 1 Free

5 Mouse Output Buffer Full
- 0 Mouse output buffer empty..... default
- 1 Mouse output buffer holds mouse data

6 General Receive / Transmit Timeout
- 0 No error ..... default
- 1 Error

7 Parity Error
- 0 No parity error (odd parity received)..... default
- 1 Even parity occurred on last byte received from keyboard / mouse

KBC Control Register .....(R/W via Commands 20h/60h)

7 Reserved .....always reads 0

6 PC Compatibility
- 0 Disable scan conversion
- 1 Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes ..... default

5 Mouse Disable
- 0 Enable Mouse Interface ..... default
- 1 Disable Mouse Interface

4 Keyboard Disable
- 0 Enable Keyboard Interface ..... default
- 1 Disable Keyboard Interface

3 Keyboard Lock Disable
- 0 Enable Keyboard Inhibit Function..... default
- 1 Disable Keyboard Inhibit Function

2 System Flag .....default=0

This bit may be read back as status register bit-2

1 Mouse Interrupt Enable
- 0 Disable mouse interrupts ..... default
- 1 Generate interrupt on IRQ12 when mouse data comes in output bufer

0 Keyboard Interrupt Enable
- 0 Disable Keyboard Interrupts..... default
- 1 Generate interrupt on IRQ1 when output buffer has been written.

Port 64 - Keyboard / Mouse Command..... WO

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT82C586B are listed n the table below.

Note: The VT82C586B Keyboard Controller is compatible with the VIA VT82C42 Industry-Standard Keyboard Controller except that due to its integrated nature, many of the input and output port pins are not available externally for use as general purpose I/O pins (even though P13-P16 are set on power-up as strapping options). In other words, many of the commands below are provided and "work", but otherwise perform no useful function (e.g., commands that set P12-P17 high or low). Also note that setting P10-11, P22-23, P26-27, and T0-1 high or low directly serves no useful purpose, since these bits are used to implement the keyboard and mouse ports and are directly controlled by keyboard controller logic.

Table 4. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
60h	Write Control Byte (next byte is Control Byte)
9xh	Write low nibble (bits 0-3) to P10-P13
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) (value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error)
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
B0h	Set P10 low
B1h	Set P11 low
B2h	Set P12 low
B3h	Set P13 low
B4h	Set P22 low
B5h	Set P23 low
B6h	Set P14 low
B7h	Set P15 low
B8h	Set P10 high
B9h	Set P11 high
BAh	Set P12 high
BBh	Set P13 high
BCh	Set P22 high
BDh	Set P23 high
BEh	Set P14 high
BFh	Set P15 high
C0h	Read input port (read P10-17 input data to the output buffer)
C1h	Poll input port low (read input data on P11-13 repeatably & put in bits 5-7 of status
C2h	Poll input port high (same except P15-17)
C8h	Unblock P22-23 (use before D1 to change active mode)
C9h	Reblock P22-23 (protection mechanism for D1)
CAh	Read mode (output KBC mode info to port 60 output buffer (bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy P10-17 output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read test inputs (T0-1 read to bits 0-1 of resp byte)
Exh	Set P23-P21 per command bits 3-1
Fxh	Pulse P23-P20 low for 6usec per command bits 3-0

All other codes not listed are undefined.

DMA Controller I/O Registers

Ports 00-0F - Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 000x 0000	**Ch 0 Base / Current Address**	**RW**
0000 0000 000x 0001	**Ch 0 Base / Current Count**	**RW**
0000 0000 000x 0010	**Ch 1 Base / Current Address**	**RW**
0000 0000 000x 0011	**Ch 1 Base / Current Count**	**RW**
0000 0000 000x 0100	**Ch 2 Base / Current Address**	**RW**
0000 0000 000x 0101	**Ch 2 Base / Current Count**	**RW**
0000 0000 000x 0110	**Ch 3 Base / Current Address**	**RW**
0000 0000 000x 0111	**Ch 3 Base / Current Count**	**RW**
0000 0000 000x 1000	**Status / Command**	**RW**
0000 0000 000x 1001	**Write Request**	**WO**
0000 0000 000x 1010	**Write Single Mask**	**WO**
0000 0000 000x 1011	**Write Mode**	**WO**
0000 0000 000x 1100	**Clear Byte Pointer F/F**	**WO**
0000 0000 000x 1101	**Master Clear**	**WO**
0000 0000 000x 1110	**Clear Mask**	**WO**
0000 0000 000x 1111	**R/W All Mask Bits**	**RW**

Note that not all bits of the address are decoded.

The Master DMA Controller is compatible with the Intel 8237 DMA Controller chip. Detailed descriptions of 8237 DMA Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports C0-DF - Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 1100 000x	**Ch 0 Base / Current Address**	**RW**
0000 0000 1100 001x	**Ch 0 Base / Current Count**	**RW**
0000 0000 1100 010x	**Ch 1 Base / Current Address**	**RW**
0000 0000 1100 011x	**Ch 1 Base / Current Count**	**RW**
0000 0000 1100 100x	**Ch 2 Base / Current Address**	**RW**
0000 0000 1100 101x	**Ch 2 Base / Current Count**	**RW**
0000 0000 1100 110x	**Ch 3 Base / Current Address**	**RW**
0000 0000 1100 111x	**Ch 3 Base / Current Count**	**RW**
0000 0000 1101 000x	**Status / Command**	**RW**
0000 0000 1101 001x	**Write Request**	**WO**
0000 0000 1101 010x	**Write Single Mask**	**WO**
0000 0000 1101 011x	**Write Mode**	**WO**
0000 0000 1101 100x	**Clear Byte Pointer F/F**	**WO**
0000 0000 1101 101x	**Master Clear**	**WO**
0000 0000 1101 110x	**Clear Mask**	**WO**
0000 0000 1101 111x	**Read/Write All Mask Bits**	**WO**

Note that not all bits of the address are decoded.

The Slave DMA Controller is compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports 80-8F - DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Register Name
0000 0000 1000 0111	**Channel 0 DMA Page (M-0).....RW**
0000 0000 1000 0011	**Channel 1 DMA Page (M-1).....RW**
0000 0000 1000 0001	**Channel 2 DMA Page (M-2).....RW**
0000 0000 1000 0010	**Channel 3 DMA Page (M-3).....RW**
0000 0000 1000 1111	**Channel 4 DMA Page (S-0) .....RW**
0000 0000 1000 1011	**Channel 5 DMA Page (S-1) .....RW**
0000 0000 1000 1001	**Channel 6 DMA Page (S-2) .....RW**
0000 0000 1000 1010	**Channel 7 DMA Page (S-3) .....RW**

Interrupt Controller Registers

Ports 20-21 - Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7. Two registers control the Master Interrupt Controller. They are:

I/O Address Bits 15-0	Register Name	
0000 0000 001x xxx0	**Master Interrupt Control**	**RW**
0000 0000 001x xxx1	**Master Interrupt Mask**	**RW**

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports A0-A1 - Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Register Name	
0000 0000 101x xxx0	**Slave Interrupt Control**	**RW**
0000 0000 101x xxx1	**Slave Interrupt Mask**	**RW**

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting bit 4 of Rx47 to 1 (offset 47h in the PCI-ISA Bridge function 0 register group). If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes to the interrupt controller register ports are directed to the standard interrupt controller registers).

Port 20 - Master Interrupt Control Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4 OCW3 bit 5**
- **3 OCW2 bit 7**
- **2 ICW4 bit 4**
- **1 ICW4 bit 1**
- **0 ICW1 bit 3**

Port 21 - Master Interrupt Mask Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4-0 T7-T3 of Interrupt Vector Address**

Port A0 - Slave Interrupt Control Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4 OCW3 bit 5**
- **3 OCW2 bit 7**
- **2 ICW4 bit 4**
- **1 ICW4 bit 1**
- **0 ICW1 bit 3**

Port A1 - Slave Interrupt Mask Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4-0 T7-T3 of Interrupt Vector Address**

Timer / Counter Registers

Ports 40-43 - Timer / Counter Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Register Name	
0000 0000 010x xx00	**Timer / Counter 0 Count**	**RW**
0000 0000 010x xx01	**Timer / Counter 1 Count**	**RW**
0000 0000 010x xx10	**Timer / Counter 2 Count**	**RW**
0000 0000 010x xx11	**Timer / Counter Cmd Mode**	**WO**

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

CMOS / RTC Registers

Port 70 - CMOS Address..... WO

7 NMI Disable.....WO
- 0 Enable NMI Generation. NMI is asserted on encountering IOCHCK# on the ISA bus or SERR# on the PCI bus.
- 1 Disable NMI Generation .....default

6-0 CMOS Address (lower 128 bytes).....WO

Port 71 - CMOS Data.....RW

7-0 CMOS Data (128 bytes)

Note: Ports 70-71 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

Port 72 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 73 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 72-73 may be accessed if Rx5A bit-2 is set to one to select the internal RTC. If Rx5A bit-2 is set to zero, accesses to ports 72-73 will be directed to an external RTC.

Port 74 - CMOS Address.....RW

7-0 CMOS Address (256 bytes)..... RW

Port 75 - CMOS Data.....RW

7-0 CMOS Data (256 bytes)

Note: Ports 74-75 may be accessed only if Function 0 Rx5B bit-1 is set to one to enable the internal RTC SRAM and if Rx48 bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 72-73 may be used to access the full extended 256-byte space. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Offset	Description		Binary Range	BCD Range
00	**Seconds**		00-3Bh	00-59h
01	**Seconds Alarm**		00-3Bh	00-59h
02	**Minutes**		00-3Bh	00-59h
03	**Minutes Alarm**		00-3Bh	00-59h
04	**Hours**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
05	**Hours Alarm**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
06	**Day of the Week**	Sun=1:	01-07h	01-07h
07	**Day of the Month**		01-1Fh	01-31h
08	**Month**		01-0Ch	01-12h
09	**Year**		00-63h	00-99h

0A Register A

7	**UIP**	Update In Progress
6-4	**DV2-0**	Divide (010=ena osc & keep time)
3-0	**RS3-0**	Rate Select for Periodic Interrupt

0B Register B

7	**SET**	Inhibit Update Transfers
6	**PIE**	Periodic Interrupt Enable
5	**AIE**	Alarm Interrupt Enable
4	**UIE**	Update Ended Interrupt Enable
3	**SQWE**	No function (read/write bit)
2	**DM**	Data Mode (0=BCD, 1=binary)
1	**24/12**	Hours Byte Format (0=12, 1=24)
0	**DSE**	Daylight Savings Enable

0C Register C

7	**IRQF**	Interrupt Request Flag
6	**PF**	Periodic Interrupt Flag
5	**AF**	Alarm Interrupt Flag
4	**UF**	Update Ended Flag
3-0	**0**	Unused (always read 0)

0D Register D

7	**VRT**	Reads 1 if VBAT voltage is OK
6-0	**0**	Unused (always read 0)

0E-7C Software-Defined Storage Registers (111 Bytes)

Offset	Extended Functions	Binary Range	BCD Range
7D	**Date Alarm**	01-1Fh	01-31h
7E	**Month Alarm**	01-0Ch	01-12h
7F	**Century Field**	13-14h	19-20h

80-FF Software-Defined Storage Registers (128 Bytes)

Table 5. CMOS Register Summary

PCI to ISA Bridge Registers (Function 0)

All registers are located in the function 0 PCI configuration space of the VT82C586B. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8/CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h ..... RO

Offset 3-2 - Device ID = 0586h ..... RO

Offset 5-4 - Command ..... RW

- **15-4 Reserved** ..... always reads 0
- **3 Special Cycle Enable** ..... Normally RW†, default = 1
- **2 Bus Master** ..... always reads 1
- **1 Memory Space** ..... Normally RO†, reads as 1
- **0 I/O Space** ..... Normally RO†, reads as 1

† If the test bit at offset 46 bit-4 is set, access to the above indicated bits is reversed: bit-3 above becomes read only (reading back 1) and bits 0-1 above become read / write (with a default of 1).

Offset 7-6 - Status ..... RWC

- **15 Detected Parity Error** ..... write one to clear
- **14 Signalled System Error** ..... always reads 0
- **13 Signalled Master Abort** ..... write one to clear
- **12 Received Target Abort** ..... write one to clear
- **11 Signalled Target Abort** ..... always reads 0
- **10-9 DEVSEL# Timing** ..... fixed at 01 (medium)
- **8 Data Parity Detected** ..... always reads 0
- **7 Fast Back-to-Back** ..... always reads 0
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID = nn ..... RO

- **7-0 ID for VT82C586 = 0xh**
  ID for VT82C586A = 2xh
  ID for VT82C586B = 3xh (3040 OEM Silicon)
  ID for VT82C586B = 4xh (3041 Production Sil.)

Offset 9 - Program Interface = 00h ..... RO

Offset A - Sub Class Code = 01h ..... RO

Offset B - Class Code = 06h ..... RO

Offset E - Header Type = 80h ..... RO

- **7-0 Header Type Code .....** 80h (Multifunction Device)

Offset F - BIST = 00h ..... RO

Offset 2F-2C - Subsystem ID ..... RO

ISA Bus Control

Offset 40 - ISA Bus Control ..... RW

- **7 ISA Command Delay**
  - 0 Normal ..... default
  - 1 Extra
- **6 Extended ISA Bus Ready**
  - 0 Disable ..... default
  - 1 Enable
- **5 ISA Slave Wait States**
  - 0 4 Wait States ..... default
  - 1 5 Wait States
- **4 Chipset I/O Wait States**
  - 0 2 Wait States ..... default
  - 1 4 Wait States
- **3 I/O Recovery Time**
  - 0 Disable ..... default
  - 1 Enable
- **2 Extend-ALE**
  - 0 Disable ..... default
  - 1 Enable
- **1 ROM Wait States**
  - 0 1 Wait State ..... default
  - 1 0 Wait States
- **0 ROM Write**
  - 0 Disable ..... default
  - 1 Enable

Offset 41 - ISA Test Mode ..... RW

- **7 Bus Refresh Arbitration** (do not program) default=0
- **6 XRDY Test Mode** (do not program) ..... default=0
- **5 Port 92 Fast Reset**
  - 0 Disable ..... default
  - 1 Enable
- **4 A20G Emulation** (do not program) ..... default=0
- **3 Double DMA Clock**
  - 0 Disable (DMA Clock = ½ ISA Clock)... default
  - 1 Enable (DMA Clock = ISA Clock)
- **2 SHOLD Lock During INTA** (do not program) def=0
- **1 Refresh Request Test Mode** (do not program). def=0
- **0 Refresh Test Mode ..... (3041 silicon only)**
  - 0 Disable ISA Refresh ..... default
  - 1 Enable ISA Refresh

  Note: This bit should always be set to one in the OEM 3040 silicon.

Offset 42 - ISA Clock Control. .....RW

7 Latch IO16#
- 0 Enable (recommended setting) .....default
- 1 Disable

6 Reserved (no defined function) ..... default = 0

5 Master Request Test Mode (do not program) . def=0

4 Reserved (no defined function) ..... default = 0

3 ISA CLOCK Select Enable
- 0 ISA Clock = PCICLK/4 .....default
- 1 ISA Clock selected per bits 2-0

2-0 ISA Bus Clock Select (if bit-3 = 1)
- 000 PCICLK/3 .....default
- 001 PCICLK/2
- 010 PCICLK/4
- 011 PCICLK/6
- 100 PCICLK/5
- 101 PCICLK/10
- 110 PCICLK/12
- 111 OSC/2

Note: Procedure for ISA CLOCK switching:
1) Set bit 3 to 0; 2) Change value of bit 2-0; 3) Set bit 3 to 1

Offset 43 - ROM Decode Control .....RW

Setting these bits enables the indicated address range to be included in the ROMCS# decode:

7 FFFE0000h-FFFEFFFFh..... default=0
6 FFF80000h-FFFDFFFFh ..... default=0
5 000E8000h-000EFFFFh ..... default=0
4 000E0000h-000E7FFFh ..... default=0
3 000D8000h-000DFFFFh ..... default=0
2 000D0000h-000D7FFFh ..... default=0
1 000C8000h-000CFFFFh ..... default=0
0 000C0000h-000C7FFFh..... default=0

Offset 44 - Keyboard Controller Control.....RW

7 KBC Timeout Test (do not program)..... default = 0

6-4 Reserved (do not program)..... default = 0

3 Mouse Lock Enable
- 0 Disabled .....default
- 1 Enabled

2-1 Reserved (do not program)..... default = 0

0 Reserved (no function)..... default = 0

Offset 45 - Type F DMA Control.....RW

7 ISA Master / DMA to PCI Line Buffer .... default=0
6 DMA type F Timing on Channel 7 ..... default=0
5 DMA type F Timing on Channel 6 ..... default=0
4 DMA type F Timing on Channel 5 ..... default=0
3 DMA type F Timing on Channel 3 ..... default=0
2 DMA type F Timing on Channel 2 ..... default=0
1 DMA type F Timing on Channel 1 ..... default=0
0 DMA type F Timing on Channel 0 ..... default=0

Offset 46 - Miscellaneous Control 1 ..... RW

7 PCI Master Write Wait States .(3041 Silicon Only)
- 0 0 Wait States..... default
- 1 1 Wait State

6 Gate INTRQ.....(3041 Silicon Only)
- 0 Disable..... default
- 1 Enable

5 Flush Line Buffer for Int or DMA IOR Cycle ....(3041 Silicon Only)
- 0 Disable..... default
- 1 Enable

4 Config Command Reg Rx04 Access (Test Only)
- 0 Normal: Bits 0-1=RO, Bit 3=RW..... default
- 1 Test Mode: Bits 0-1=RW, Bit-3=RO

3 Reserved (do not program).....default = 0

2 Reserved (no function) .....default = 0

1 PCI Burst Read Interruptability
- 0 Allow burst reads to be interrupted..... default
- 1 Don't allow PCI burst reads to be interrupted

0 Post Memory Write Enable
- 0 Disable..... default
- 1 Enable

The Post Memory Write function is automatically enabled when Delay Transaction (see Rx47 bit-6 below) is enabled, independent of the state of this bit.

Offset 47 - Miscellaneous Control 2 ..... RW

7 CPU Reset Source
- 0 Use CPURST as CPU Reset..... default
- 1 Use INIT as CPU Reset

6 PCI Delay Transaction Enable
- 0 Disable..... default
- 1 Enable

The "Post Memory Write" function is automatically enabled when this bit is enabled, independent of the state of Rx46 bit-0 above.

5 EISA 4D0/4D1 Port Enable
- 0 Disable (ignore ports 4D0-1)..... default
- 1 Enable (ports 4D0-1 per EISA specification)

4 Interrupt Controller Shadow Register Enable
- 0 Disable..... default
- 1 Enable

3 Reserved (always program to 0).....default = 0

Note: Always mask this bit. This bit may read back as either 0 or 1 but must always be programmed with 0.

2 Write Delay Transaction Time-Out Timer Enable
- 0 Disable..... default
- 1 Enable

1 Read Delay Transaction Time-Out Timer Enable
- 0 Disable..... default
- 1 Enable

0 Software PCI Reset .....write 1 to generate PCI reset

Offset 48 - Miscellaneous Control 3.....RW

7-6 Reserved ..... always reads 0

5 MASTER# Pin Function (Pin 137)... (3041 Silicon)
- 0 "Input" Mode (Pin 137 = MASTER#) ...default
- 1 "Output" Mode (Pin 137 = SDDIR)

4 IRQ8# Input Source.....(3040F and 3041 Silicon)
- 0 IRQ8# input on RTCX1 pin 104.....default
- 1 IRQ8# input on KEYLOCK pin 106

See also Rx5A[2] - internal/external RTC:

Rx5A[2]	Rx48[4]	Pin Function
0	0	Ext RTC, IRQ8# in pin 104
0	1	Ext RTC, IRQ8# in pin 106
1	x	Int RTC, no IRQ8# in req'd

3 Extra RTC Port 74/75 Enable
- 0 Disable .....default
- 1 Enable

2 Integrated USB Controller Disable
- 0 Enable.....default
- 1 Disable

1 Integrated IDE Controller Disable
- 0 Enable.....default
- 1 Disable

0 512K PCI Memory Decode
- 0 Use Rx4E[15-12] to select top of PCI memory
- 1 Use contents of Rx4E[15-12] plus 512K as top of PCI memory.....default

Offset 4A - IDE Interrupt Routing .....RW

7 Wait for PGNT Before Grant to ISA Master / DMA
- 0 Disable .....default
- 1 Enable **(must be set to 1)**

6 Bus Select for Access to I/O Devices Below 100h
- 0 Access ports 00-FFh via XD bus.....default
- 1 Access ports 00-FFh via SD bus (applies to external devices only; internal devices such as the mouse controller are not effected)

5-4 Reserved (do not program) ..... default = 0

3-2 IDE Second Channel IRQ Routing
- 00 IRQ14
- 01 IRQ15.....default
- 10 IRQ10
- 11 IRQ11

1-0 IDE Primary Channel IRQ Routing
- 00 IRQ14.....default
- 01 IRQ15
- 10 IRQ10
- 11 IRQ11

4C - ISA DMA/Master Memory Access Control 1 ..... RW

7-0 PCI Memory Hole Bottom Address
These bits correspond to HA[23:16] .....default=0

4D - ISA DMA/Master Memory Access Control 2 ..... RW

7-0 PCI Memory Hole Top Address (HA[23:16])
These bits correspond to HA[23:16] .....default=0

Note: Access to the memory defined in the PCI memory hole will not be forwarded to PCI. This function is disabled if the top address less than or equal to the bottom address.

4F-4E - ISA DMA/Master Memory Access Control 3... RW

15-12 Top of PCI Memory for ISA DMA/Master accesses
- 0000 1M ..... default
- 0001 2M
- ... ...
- 1111 16M

Note: All ISA DMA / Masters that access addresses higher than the top of PCI memory will not be directed to the PCI bus.

11 Forward E0000-EFFFF Accesses to PCI.....def=0
10 Forward A0000-BFFFF Accesses to PCI .....def=0
9 Forward 80000-9FFFF Accesses to PCI .....def=1
8 Forward 00000-7FFFF Accesses to PCI .....def=1
7 Forward DC000-DFFFF Accesses to PCI .....def=0
6 Forward D8000-DBFFF Accesses to PCI .....def=0
5 Forward D4000-D7FFF Accesses to PCI .....def=0
4 Forward D0000-D3FFF Accesses to PCI .....def=0
3 Forward CC000-CFFFF Accesses to PCI .....def=0
2 Forward C8000-CBFFF Accesses to PCI .....def=0
1 Forward C4000-C7FFF Accesses to PCI .....def=0
0 Forward C0000-C3FFF Accesses to PCI .....def=0

Plug and Play Control

Offset 50 - Reserved (Do Not Program) .....RW

7-0 Reserved ..... default = 04h

Offset 54 - PCI IRQ Edge / Level Select.....RW

7-4 Reserved ..... always reads 0

The following bits all default to "level" triggered (0)

3 PIRQA# Invert (edge) / Non-invert (level).....(1/0)

2 PIRQB# Invert (edge) / Non-invert (level).....(1/0)

1 PIRQC# Invert (edge) / Non-invert (level).....(1/0)

0 PIRQD# Invert (edge) / Non-invert (level).....(1/0)

Note: PIRQA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Note: The definitions of the fields of the following three registers were incorrectly documented in some earlier revisions of this document. The silicon has not changed and the following definition should be used for all silicon revisions:

Offset 55 - PNP IRQ Routing 1 .....RW

These bits control routing for external IRQ inputs MIRQ0-1.

7-4 PIRQD# Routing (see PnP IRQ routing table)

3-0 MIRQ0 Routing (see PnP IRQ routing table)

Offset 56 - PNP IRQ Routing 2 .....RW

7-4 PIRQA# Routing (see PnP IRQ routing table)

3-0 PIRQB# Routing (see PnP IRQ routing table)

Offset 57 - PNP IRQ Routing 3 .....RW

7-4 PIRQC# Routing (see PnP IRQ routing table)

3-0 MIRQ1 Routing (see PnP IRQ routing table)

Note: these bits must be set to 0 if Rx48[4]=1 and Rx59[1]=1 (input IRQ8# on MIRQ1 pin 106)

Offset 58 - PNP IRQ Routing 4 ..... RW

These bits control routing for external IRQ input MIRQ2.

7-4 Reserved .....always reads 0

3-0 MIRQ2 Routing (see PnP IRQ routing table)

PnP IRQ Routing Table

0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 Reserved
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 Reserved
1110 IRQ14
1111 IRQ15

Offset 59 - MIRQ Pin Configuration ..... RW

7-4 Reserved .....always reads 0

3 Power-On Suspend Status Output Enable (Pin 90) ..(3040 Rev F and 3041 Silicon Only))

0 Disable POS Status Output..... default

1 Enable POS Status output on pin 90. Alternate functions of pin 90 are APICCS# and MIRQ0 if this bit is not set (see bit-0 below).

2 MIRQ2 / MASTER# Selection (Pin 137)

0 MIRQ2..... default

1 MASTER#

1 MIRQ1 / KEYLOCK Selection (Pin 106)

0 MIRQ1..... default

1 KEYLOCK

0 MIRQ0 / APICCS# Selection (Pin 90)

0 MIRQ0..... default

1 APICCS#

Offset 5A - XD Power-On Strap Options.....RW

The bits in this register are latched from pins XD7-0 at power-up but are read/write accessible so may be changed after power-up to change the default strap setting:

- **7** **Keyboard RP16**.....latched from XD7
- **6** **Keyboard RP15** .....latched from XD6
- **5** **Keyboard RP14** .....latched from XD5
- **4** **Keyboard RP13** .....latched from XD4
- **3** **Reserved** ..... always reads 0
- **2** **Internal RTC Enable** .....latched from XD2
  - 0 Disable
  - 1 Enable
- **1** **Internal PS2 Mouse Enable**.....latched from XD1
  - 0 Disable
  - 1 Enable
- **0** **Internal KBC Enable**.....latched from XD0
  - 0 Disable
  - 1 Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1) or driving it low during reset with a 7407 TTL open collector buffer (for 0) as shown in the suggested circuit below:

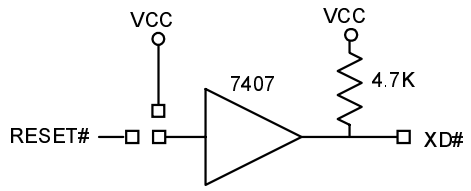

Figure 3. Strap Option Circuit

Offset 5B - Internal RTC Test Mode ..... RW

- **7-3** **Reserved** .....always reads 0
- **2** **RTC Reset Enable** (do not program) .....default=0
- **1** **RTC SRAM Access Enable**
  - 0 Disable..... default
  - 1 Enable

  This bit is set if the internal RTC is disabled but it is desired to still be able to access the internal RTC SRAM via ports 74-75. If the internal RTC is enabled, setting this bit does nothing (the internal RTC SRAM should be accessed at either ports 70/71 or 72/73.
- **0** **RTC Test Mode Enable** (do not program) . default=0

Offset 5C - DMA Control (3041 Silicon Only) ..... RW

- **7-1** **Reserved** .....always reads 0
- **0** **DMA Line Buffer Disable**
  - 0 DMA cycles can be to/from line buffer ..... def
  - 1 Disable DMA Line Buffer

Distributed DMA Control

Offset 61-60 - Distributed DMA Ch 0 Base / Enable.....RW

15-4 Channel 0 Base Address Bits 15-4 ..... default = 0

3 Channel 0 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 63-62 - Distributed DMA Ch 1 Base / Enable.....RW

15-4 Channel 1 Base Address Bits 15-4 ..... default = 0

3 Channel 1 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 65-64 - Distributed DMA Ch 2 Base / Enable.....RW

15-4 Channel 2 Base Address Bits 15-4 ..... default = 0

3 Channel 2 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 67-66 - Distributed DMA Ch 3 Base / Enable.....RW

15-4 Channel 3 Base Address Bits 15-4 ..... default = 0

3 Channel 3 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 6B-6A - Distributed DMA Ch 5 Base / Enable ....RW

15-4 Channel 5 Base Address Bits 15-4 ..... default = 0

3 Channel 5 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 6D-6C - Distributed DMA Ch 6 Base / Enable ....RW

15-4 Channel 6 Base Address Bits 15-4 ..... default = 0

3 Channel 6 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Offset 6F-6E - Distributed DMA Ch 7 Base / Enable.....RW

15-4 Channel 7 Base Address Bits 15-4 ..... default = 0

3 Channel 7 Enable

0 Disable .....default

1 Enable

2-0 Reserved ..... always reads 0

Miscellaneous

Offset 73-70 - Subsystem ID (3041 Silicon Only) ..... WO

31-0 Subsystem ID and Subsystem Vendor ID

Write Only. Always reads back 0.

Contents may be read at offset 2C.

Enhanced IDE Controller Registers (Function 1)

This Enhanced IDE controller interface is fully compatible with the SFF 8038i v.1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the function 1 PCI configuration space of the VT82C586B. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h=VIA).....RO

Offset 3-2 - Device ID (0571h=IDE Controller).....RO

Offset 5-4 - Command.....RW

15-10 Reserved ..... always reads 0

9 Fast Back to Back Cycles .....fixed at 0 (disabled)

8 SERR# Enable.....fixed at 0 (disabled)

7 Address Stepping ..... default=**1 (enabled)**
VIA recommends that this bit always be set to 1 to provide additional address decode time to IDE devices.

6 Parity Error Response.....fixed at 0 (disabled)

5 VGA Palette Snoop .....fixed at 0 (disabled)

4 Memory Write & Invalidate .....fixed at 0 (disabled)

3 Special Cycles.....fixed at 0 (disabled)

2 Bus Master ..... default=0 (disabled)
S/G operation can be issued only when the "Bus Master" bit is enabled.

1 Memory Space.....fixed at 0 (disabled)

0 I/O Space ..... default=0 (disabled)
When the "I/O Space" bit is disabled, the device will not respond to any I/O addresses for both compatible and native mode.

Offset 7-6 - Status.....RWC

15 Detected Parity Error..... default=0

14 Signalled System Error..... default=0

13 Received Master Abort..... default=0

12 Received Target Abort ..... default=0

11 Signalled Target Abort.....Fixed at 0

10-9 DEVSEL# Timing .....default = 01 (medium)

8 Data Parity Detected..... default=0

7 Fast Back to Back .....Fixed at 1

6-0 Reserved ..... always reads 0

Offset 8 - Revision ID.....RO

0-7 Revision Code for IDE Controller Logic Block

Offset 9 - Programming Interface ..... RW

7 Master IDE Capability..... fixed at 1 (Supported)

6-4 Reserved .....always reads 0

3 Programmable Indicator - Secondary ..... fixed at 1
0 Fixed (mode is determined by bit-2)
1 Supports both modes (may be set to either mode by writing bit-2)

2 Channel Operating Mode - Secondary
0 Compatibility Mode .....default if SPKR=0
1 Native PCI Mode .....default if SPKR=1
The default value for this bit is determined at power-up as strapped by the SPKR pin (pin 134)): 0 = fixed IDE addressing, 1 = flexible IDE addressing. See figure 2 for strap circuit.

1 Programmable Indicator - Primary..... fixed at 1
0 Fixed (mode is determined by bit-2)
1 Supports both modes (may be set to either mode by writing bit-0)

0 Channel Operating Mode - Primary
0 Compatibility Mode.....default if SPKR=0
1 Native PCI Mode .....default if SPKR=1
The default value for this bit is determined at power-up as strapped by the SPKR pin (pin 134)): 0 = fixed IDE addressing, 1 = flexible IDE addressing. See figure 2 for strap circuit.

Compatibility Mode (fixed IRQs and I/O addresses):

Channel	Command Block Registers	Control Block Registers	IRQ
Pri	1F0-1F7	3F6	14
Sec	170-177	376	15

Native PCI Mode (registers are programmable in I/O space)

Channel	Command Block Registers	Control Block Registers
Pri	BA @offset 10h	BA @offset 14h
Sec	BA @offset 18h	BA @offset 1Ch

Command register blocks are 8 bytes of I/O space
Control registers are 4 bytes of I/O space (only byte 2 is used)

Offset A - Sub Class Code (01h) ..... RO

Offset B - Base Class Code (01h)..... RO

Offset D - Latency Timer (Default=0)..... RW

Offset E - Header Type (00h)..... RO

Offset F - BIST (00h)..... RO

Offset 13-10 - Pri Data / Command Base Address.....RW

Specifies an 8 byte I/O address space.

31-16 Reserved .....always read 0
15-3 Port Address..... default=01F0h
2-0 Fixed at 001b ..... fixed

Offset 17-14 - Pri Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 3F6h for the default base address of 3F4h).

31-16 Reserved .....always read 0
15-2 Port Address..... default=03F4h
1-0 Fixed at 01b ..... fixed

Offset 1B-18 - Sec Data / Command Base Address .....RW

Specifies an 8 byte I/O address space.

31-16 Reserved .....always read 0
15-3 Port Address ..... default=0170h
2-0 Fixed at 001b ..... fixed

Offset 1F-1C - Sec Control / Status Base Address.....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 376h for the default base address of 374h).

31-16 Reserved .....always read 0
15-2 Port Address ..... default=0374h
1-0 Fixed at 01b ..... fixed

Offset 23-20 - Bus Master Control Regs Base Address..RW

Specifies a 16 byte I/O address space compliant with the **SFF-8038**i **rev 1.0** specification.

31-16 Reserved .....always read 0
15-4 Port Address ..... default=CC0h
3-0 Fixed at 0001b ..... fixed

Offset 3C - Interrupt Line (0Eh) ..... RW

Offset 3D - Interrupt Pin (00h)..... RO

7-0 Interrupt Routing Mode
00h Legacy mode interrupt routing..... default
01h Native mode interrupt routing

Offset 3E - Min Gnt (00h) ..... RO

Offset 3F - Max Latency (00h)..... RO

IDE-Controller-Specific Confiiguration Registers

Offset 40 - Chip Enable.....RW

7-2 Reserved ..... always reads 000001b
1 Primary Channel Enable..... default = 0 (disabled)
0 Secondary Channel Enable .... default = 0 (disabled)

Offset 41 - IDE Configuration.....RW

7 Primary IDE Read Prefetch Buffer
0 Disable .....default
1 Enable
6 Primary IDE Post Write Buffer
0 Disable .....default
1 Enable
5 Secondary IDE Read Prefetch Buffer
0 Disable .....default
1 Enable
4 Secondary IDE Post Write Buffer
0 Disable .....default
1 Enable
3 Reserved (read write) .....**do not change**, default=0
2 Reserved (read write) .....**do not change**, default=1
1 Reserved (read write) .....**do not change**, default=1
0 Reserved (read write) .....**do not change**, default=0

Offset 42 - Reserved (Do Not Program) .....RW

Offset 43 - FIFO Configuration .....RW

7 PREQ# Asserted Till DDACK# De-Asserted .... (3041 Silicon Only)
0 Disabled .....default
1 Enabled
6-5 FIFO Configuration Between the Two Channels

	Primary	Secondary
00	16	0
01	8	8.....default
10	8	8
11	0	16

4 Reserved ..... always reads 1
3-2 Threshold for Primary Channel
00 1
01 3/4
10 1/2 .....default
11 1/4
1-0 Threshold for Secondary Channel
00 1
01 3/4
10 1/2 .....default
11 1/4

Offset 44 - Miscellaneous Control 1 ..... RW

7 Reserved .....always reads 0
6 Master Read Cycle IRDY# Wait States
0 0 wait states
1 1 wait state..... default
5 Master Write Cycle IRDY# Wait States
0 0 wait states
1 1 wait state..... default
4 FIFO Output Data 1/2 Clock Advance
0 Disabled..... default
1 Enabled
3 Bus Master IDE Status Register Read Retry
Retry bus master IDE status register read when master write operation for DMA read is not complete
0 Disabled
1 Enabled..... default
2 Reserved .....always reads 0
1 B-Channel Threshold Value 0 (3041 Silicon Only)
0 Disabled..... default
1 Enabled
0 A-Channel Threshold Value 0 (3041 Silicon Only)
0 Disabled..... default
1 Enabled

Offset 45 - Miscellaneous Control 2 ..... RW

7 Reserved .....always reads 0
6 Interrupt Steering Swap
0 Don't swap channel interrupts ..... default
1 Swap interrupts between the two channels
5-0 Reserved .....always reads 0

Offset 46 - Miscellaneous Control 3 ..... RW

7 Primary Channel Read DMA FIFO Flush
1 = Enable FIFO flush for read DMA when interrupt asserts primary channel. .....default=1 (enabled)
6 Secondary Channel Read DMA FIFO Flush
1 = Enable FIFO flush for Read DMA when interrupt asserts secondary channel. .....Default=1 (enabled)
5 Primary Channel End-of-Sector FIFO Flush
1 = Enable FIFO flush at the end of each sector for the primary channel. ..... Default=0 (disabled)
4 Secondary Channel End-of-Sector FIFO Flush
1 = Enable FIFO flush at the end of each sector for the secondary channel..... Default=0 (disabled)
3-2 Reserved .....always reads 0
1-0 Max DRDY Pulse Width
Maximum DRDY# pulse width after the cycle count. Command will deassert in spite of DRDY# status to avoid system ready hang.
00 No limitation..... default
01 64 PCI clocks
10 128 PCI clocks
11 192 PCI clocks

Offset 4B-48 - Drive Timing Control.....RW

The following fields define the Active Pulse Width and Recovery Time for the IDE DIOR# and DIOW# signals:

31-28 Primary Drive 0 Active Pulse Width..... def=1010b
27-24 Primary Drive 0 Recovery Time..... def=1000b
23-20 Primary Drive 1 Active Pulse Width..... def=1010b
19-16 Primary Drive 1 Recovery Time..... def=1000b
15-12 Secondary Drive 0 Active Pulse Width .. def=1010b
11-8 Secondary Drive 0 Recovery Time ..... def=1000b
7-4 Secondary Drive 1 Active Pulse Width .. def=1010b
3-0 Secondary Drive 1 Recovery Time ..... def=1000b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4C - Address Setup Time.....RW

7-6 Primary Drive 0 Address Setup Time
5-4 Primary Drive 1 Address Setup Time
3-2 Secondary Drive 0 Address Setup Time
1-0 Secondary Drive 1 Address Setup Time
For each field above:
00 1T
01 2T
10 3T
11 4T .....default

Offset 4E - Secondary Non-1F0 Port Access Timing.....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b
The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4F - Primary Non-1F0 Port Access Timing` .....RW

7-4 DIOR#/DIOW# Active Pulse Width..... def=1111b
3-0 DIOR#/DIOW# Recovery Time..... def=1111b
The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 53-50 - UltraDMA33 Extended Timing Control. RW

31 Pri Drive 0 UltraDMA33-Mode Enable Method
0 Enable by using "Set Feature" command..... def
1 Enable by setting bit-6 of this register
30 Pri Drive 0 UltraDMA33-Mode Enable
0 Disable..... default
1 Enable UltraDMA33-Mode Operation
29 Pri Drive 0 Transfer Mode..... read only
0 Based on UltraDMA33 DMA mode..... default
1 Based on UltraDMA33 PIO Mode
28-26 Reserved .....always reads 0
25-24 Pri Drive 0 Cycle Time
0 2T
1 3T
2 4T
3 5T ..... default

23 Pri Drive 1 UltraDMA33-Mode Enable Method
22 Pri Drive 1 UltraDMA33-Mode Enable
21 Pri Drive 1 Transfer Mode..... read only
20-18 Reserved .....always reads 0
17-16 Pri Drive 1 Cycle Time

15 Sec Drive 0 UltraDMA33-Mode Enable Method
14 Sec Drive 0 UltraDMA33-Mode Enable
13 Sec Drive 0 Transfer Mode..... read only
12-10 Reserved .....always reads 0
9-8 Sec Drive 0 Cycle Time

7 Sec Drive 1 UltraDMA33-Mode Enable Method
6 Sec Drive 1 UltraDMA33-Mode Enable
5 Sec Drive 1 Transfer Mode..... read only
4-2 Reserved .....always reads 0
1-0 Sec Drive 1 Cycle Time

Each byte defines UltraDMA33 operation for the indicated drive. The bit definitions are the same within each byte.

Offset 61-60 - Primary Sector Size ..... RW

15-12 Reserved .....always reads 0
11-0 Number of Bytes Per Sector .....default=200h

Offset 69-68 - Secondary Sector Size ..... RW

15-12 Reserved .....always reads 0
11-0 Number of Bytes Per Sector .....default=200h

IDE I/O Registers

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details.

Offset 0 - Primary Channel Command

Offset 2 - Primary Channel Status

Offset 4-7 - Primary Channel PRD Table Address

Offset 8 - Secondary Channel Command

Offset A - Secondary Channel Status

Offset C-F - Secondary Channel PRD Table Address

Universal Serial Bus Controller Registers (Function 2)

This USB host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 2 PCI configuration space of the VT82C586B. The USB I/O registers are defined in the UHCI v1.1 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3038h = VT82C586B USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate . default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error) ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h) ..... RO

Offset B - Base Class Code (0Ch) ..... RO

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset 0E - Header Type (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 IRQ15 (see note below)

Note: Some software incorrectly sets this register to 0FFh to disable USB interrupts. A value of 0FFh will program the USB interrupt to interrupt controller channel 15 and cause the secondary IDE channel to work improperly.

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1.....RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, and Memory-Write-and-Invalidate .....default
- 1 Only support Memory Read, Memory Write Commands

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs.....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation.....default
- 1 Enable parity check and PERR# generation

4 Reserved ..... always reads 0

3 USB Data Length Option
- 0 Support TD length up to 1280.....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management.....default
- 1 Enable USB power management

1 DMA Option
- 0 16 DW burst access.....default
- 1 8 DW burst access

0 PCI Wait States
- 0 Zero wait .....default
- 1 One wait

Offset 41 - Miscellaneous Control 2.....RW

7-3 Reserved ..... always reads 0

2 Trap Option
- 0 Set trap 60/64 status bits without checking enable bits .....default
- 1 Set trap 60/64 status bits only when trap 60/64 enable bits are set.

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI.....default
- 1 Don't pass through Write I/O port 64 (ff)

0 Reserved ..... always reads 0

Offset 60 - Serial Bus Release Number.....RO

7-0 Release Number..... always reads 10h

Offset C1-C0 - Legacy Support.....RO

15-0 UHCI v1.1 Compliant..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

Offset 1-0 - USB Command

Offset 3-2 - USB Status

Offset 5-4 - USB Interrupt Enable

Offset 7-6 - Frame Number

Offset B-8 - Frame List Base Address

Offset 0C - Start Of Frame Modify

Offset 11-10 - Port 1 Status / Control

Offset 13-12 - Port 2 Status / Control

Offset 1F-14 - Reserved

Power Management Registers (Function 3)

This section describes the ACPI (Advanced Configuration and Power Interface) Power Management system of the VT82C586B. This system supports both ACPI and legacy power management functions and is compatible with the APM v1.2 and ACPI v0.9 specifications.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID ..... (3040h = ACPI Power Mgmt)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... fixed at 0
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... fixed at 0
0 Disable ..... always reads 0 in 3040F and later
1 Enable

Note: In 3040E and earlier silicon, this bit could be set to 1 to allow access to the Power Management I/O Register Block (the quadword at offset 20 was used in that silicon to set the base address for this register block). Beginning with 3040F silicon, the function of this bit was moved to offset 41 bit-7 and the base address register for the PM I/O register block was moved from to offset 48.

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... always reads 0
13 Received Master Abort ..... always reads 0
12 Received Target Abort ..... always reads 0
11 Signalled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8 Data Parity Detected ..... always reads 0
7 Fast Back to Back ..... always reads 1
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-4 Silicon Version Code
0 OEM Version ("3040 Silicon")
1 Production Version ("3041 Silicon")
2-F -reserved for future use-
3-0 Silicon Revision Code
OEM Version
0 Revision E ("3040E")
1 Revision F ("3040F")
2-F -reserved for future use-
Production Version
0 Revision A ("3041" or "3041A")
1-F -reserved for future use-

Programming and pin differences between the above silicon versions and revisions are indicated in this document in the appropriate section. Marking specifications corresponding to the above versions and revisions are also included in the Mechanical Specifications section of this document.

Offset 9 - Programming Interface (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 61h.

Offset A - Sub Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 62h.

Offset B - Base Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 3 offset 63h.

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset 0E - Header Type (00h) ..... RO

Offset 23-20 - I/O Register Base Address (3040E only). RW

31-16 Reserved ..... always reads 0
15-8 Power Management I/O Register Base Address. Port Address for the base of the 256-byte Power Management I/O Register block, corresponding to AD[15:8]. The "I/O Space" bit at offset 5-4 bit-0 enables access to this register block.
7-0 00000001b

Power Management-Specific PCI Configuration Registers

Offset 40 - Pin Configuration (C0h) .....RW

7 GPIO4 Configuration
- 0 Define pin 136 as GPO_WE
- 1 Define pin 136 as GPIO4 .....default

6 GPIO3 Configuration
- 0 Define pin 92 as GPI_RE#
- 1 Define pin 92 as GPIO4 .....default

5-0 Reserved ..... always reads 0

Offset 41 - General Configuration (00h) .....RW

7 3040E and earlier: Reserved

7 3040F and later: I/O Enable for ACPI I/O Base
- 0 Disable access to ACPI I/O block .....default
- 1 Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.

6 ACPI Timer Reset
- 0 Disable .....default
- 1 Enable

5-4 Reserved (Do Not Program)..... default = 0

3 ACPI Timer Count Select
- 0 24-bit Timer .....default
- 1 32-bit Timer

2 PCI Frame Activation in C2 as Resume Event
- 0 Disable .....default
- 1 Enable

1 Clock Throttling Clock Selection
- 0 32 usec (512 usec cycle time).....default
- 1 1 msec (16 msec cycle time)

0 Reserved (Do Not Program)..... default = 0

Offset 42 - SCI Interrupt Configuration (00h) .....RW

7-4 Reserved ..... always reads 0

3-0 SCI Interrupt Assignment
- 0000 Disabled .....default
- 0001 IRQ1
- 0010 Reserved
- 0011 IRQ3
- 0100 IRQ4
- 0101 IRQ5
- 0110 IRQ6
- 0111 IRQ7
- 1000 IRQ8
- 1001 IRQ9
- 1010 IRQ10
- 1011 IRQ11
- 1100 IRQ12
- 1101 IRQ13
- 1110 IRQ14
- 1111 IRQ15

Offset 45-44 - Primary Interrupt Channel (0000h) ..... RW

15 1/0 = Ena/Disa IRQ15 as Primary Intrpt Channel
14 1/0 = Ena/Disa IRQ14 as Primary Intrpt Channel
13 1/0 = Ena/Disa IRQ13 as Primary Intrpt Channel
12 1/0 = Ena/Disa IRQ12 as Primary Intrpt Channel
11 1/0 = Ena/Disa IRQ11 as Primary Intrpt Channel
10 1/0 = Ena/Disa IRQ10 as Primary Intrpt Channel
9 1/0 = Ena/Disa IRQ9 as Primary Intrpt Channel
8 1/0 = Ena/Disa IRQ8 as Primary Intrpt Channel
7 1/0 = Ena/Disa IRQ7 as Primary Intrpt Channel
6 1/0 = Ena/Disa IRQ6 as Primary Intrpt Channel
5 1/0 = Ena/Disa IRQ5 as Primary Intrpt Channel
4 1/0 = Ena/Disa IRQ4 as Primary Intrpt Channel
3 1/0 = Ena/Disa IRQ3 as Primary Intrpt Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Primary Intrpt Channel
0 1/0 = Ena/Disa IRQ0 as Primary Intrpt Channel

Offset 47-46 - Secondary Interrupt Channel (0000h).... RW

15 1/0 = Ena/Disa IRQ15 as Secondary Intr Channel
14 1/0 = Ena/Disa IRQ14 as Secondary Intr Channel
13 1/0 = Ena/Disa IRQ13 as Secondary Intr Channel
12 1/0 = Ena/Disa IRQ12 as Secondary Intr Channel
11 1/0 = Ena/Disa IRQ11 as Secondary Intr Channel
10 1/0 = Ena/Disa IRQ10 as Secondary Intr Channel
9 1/0 = Ena/Disa IRQ9 as Secondary Intr Channel
8 1/0 = Ena/Disa IRQ8 as Secondary Intr Channel
7 1/0 = Ena/Disa IRQ7 as Secondary Intr Channel
6 1/0 = Ena/Disa IRQ6 as Secondary Intr Channel
5 1/0 = Ena/Disa IRQ5 as Secondary Intr Channel
4 1/0 = Ena/Disa IRQ4 as Secondary Intr Channel
3 1/0 = Ena/Disa IRQ3 as Secondary Intr Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Secondary Intr Channel
0 1/0 = Ena/Disa IRQ0 as Secondary Intr Channel

Offset 4B-48 - I/O Register Base Address (3040F and later silicon; see Offset 23-20 for 3040E and earlier) ..... RW

31-16 Reserved .....always reads 0

15-8 Power Management I/O Register Base Address. Port Address for the base of the 256-byte Power Management I/O Register block, corresponding to AD[15:8]. The "I/O Space" bit at offset 41 bit-7 (offset 5-4 bit-0 in 3040E and earlier silicon) enables access to this register block. The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power-Management-Specific PCI Configuration register descriptions and the Power Management Subsystem overview.

7-0 00000001b

Offset 53-50 - GP Timer Control (0000 0000h) .....RW

31-30 Conserve Mode Timer Count Value
- 00 1/16 second .....default
- 01 1/8 second
- 10 1 second
- 11 1 minute

29 Conserve Mode Status
This bit reads 1 when in Conserve Mode

28 Conserve Mode Enable
Set to 1 to enable Conserve Mode (not used in desktop applications).

27-26 Secondary Event Timer Count Value
- 00 2 milliseconds.....default
- 01 64 milliseconds
- 10 ½ second
- 11 by EOI + 0.25 milliseconds

25 Secondary Event Occurred Status
This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.

24 Secondary Event Timer Enable
- 0 Disable .....default
- 1 Enable

23-16 GP1 Timer Count Value (base defined by bits 5-4)

15-8 GP0 Timer Count Value (base defined by bits 1-0)

7 GP1 Timer Start
On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit is set to one (bit-3 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP1 Timer Timeout Enable bit is set (bit-3 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP1 Timer Automatic Reload
This bit is set to one to enable the GP1 timer to reload automatically after counting down to 0.

5-4 GP1 Timer Base
- 00 Disable .....default
- 01 32 usec
- 10 1 second
- 11 1 minute

3 GP0 Timer Start
On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit is set to one (bit-2 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP0 Timer Timeout Enable bit is set (bit-2 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP0 Timer Automatic Reload
This bit is set to one to enable the GP0 timer to reload automatically after counting down to 0.

1-0 GP0 Timer Base
- 00 Disable..... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 61 - Programming Interface Read Value ..... WO

7-0 Rx09 Read Value
The value returned by the register at offset 9h (Programming Interface) may be changed by writing the desired value to this location.

Offset 62 - Sub Class Read Value..... WO

7-0 Rx0A Read Value
The value returned by the register at offset 0Ah (Sub Class Code) may be changed by writing the desired value to this location.

Offset 63 - Base Class Read Value..... WO

7-0 Rx0B Read Value
The value returned by the register at offset 0Bh (Base Class Code) may be changed by writing the desired value to this location.

Power Management Subsystem Overview

The power management function of the VT82C586B is indicated in the following block diagram:

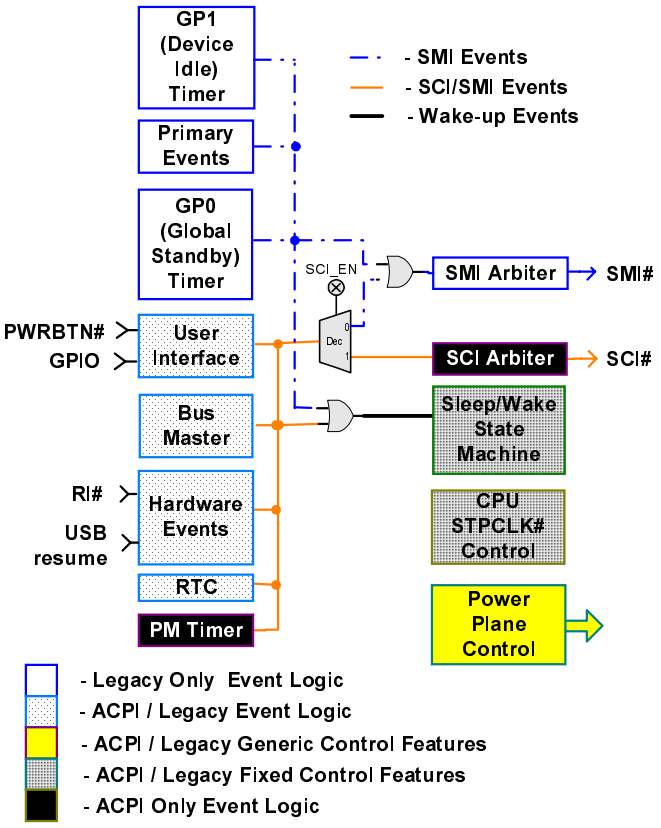

Figure 4. Power Management Subsystem Block Diagram

Refer to ACPI Specification v0.9 and APM specification v1.2 for additional information.

Power Plane Management

There are three power planes inside the VT82C586B. The scheme is optimal for systems with ATX power supplies, although it also works using non-ATX power supplies. The key feature of the ATX power supply is that two sets of power sources are available: the first set is always on unless turned off by the mechanical switch. Only one voltage (5V) is available for this set. The second set includes the normal 5V and 12V and is controlled by an input signal PWRON as well as the mechanical switch. This set of voltages is available only when both the mechanical switch is on and the PWRON signal is high. The power planes powered by the above two sets of supplies are referred to as VDD-5VSB and VDD-5V (also called VDD5), respectively. In addition to the two power planes, a third plane is powered by the combination of 5VSB and VBAT for the integrated real time clock. Most of the circuitry inside the VT82C586B is powered by VDD-5V. The amount of logic powered by VDD-5VSB is very small and remains functional as long as the mechanical switch of the power supply is turned on. The main function of this logic is to control the power supply of the VDD-5V plane.

General Purpose I/O Ports

As ACPI compliant hardware, the VT82C586B includes PWRBTN# (pin 91) and RI# (pin 93) pins to implement power button and ring indicator functionality. In addition, a PWRON pin (pin 107) is also available to control the VDD-5V power plane by VDD-5VSB powered logic. Furthermore, the VT82C586B offers many general purpose I/O ports with the following capabilities:

- **I^2C support**
- **Three GPIO ports** without external logic in addition to the I^2C port. Five GPIO ports are available if I^2C functionality is not used. Every port can be used inputs, outputs or I/O with external SCI/SMI capabilities.
- **Sixteen GPI and sixteen GPO pins** using external buffers (244 buffers for input and 373 latches for output).

Pins 87, 88 and 94 of the VT82C586B are dedicated general purpose I/O pins that can be used as inputs, outputs or I/O with external SMI capability. In particular, pins 87 and 88 can be used to implement a software-implemented I^2C port for system configuration and general purpose peripheral communication. Pins 92 and 136 can be configured either as dedicated general purpose I/O pins or as control signals for external buffers for implementing up to sixteen GPI and sixteen GPO ports. The GPI and GPO ports are connected to the SD15-8 and XD7-0. The configuration is determined in the GPIO4_CFG and CPIO3_CFG bits of the PIN_CFG register:

GPIO4_CFG: default to 1 to define pin 136 as GPIO4; set to 0 to redefine the pin as GPO_WE latch enable.

GPIO3_CFG: default to 1 to define pin 92 as GPIO3; set to 0 to redefine the pin as GPI_RE# buffer enable.

Power Management Events

Three types of power management events are supported:

1) **ACPI-required Fixed Events** defined in the PM1a_STS and PM1a_EN registers. These events can trigger either SCI or SMI depending on the SCI_EN bit:
   - PWRBTN# Triggering
   - RTC Alarm
   - ACPI Power Management Timer Carry (always SCI)
   - BIOS Release (always SCI)
2) **ACPI-aware General Purpose Function Events** defined in the GP_STS and GP_SCI_EN, and GP_SMI_EN registers. These events can trigger either SCI or SMI depending on the setting of individual SMI and SCI enable bits:
   - EXTSMI triggering (refer to Table 2)
   - USB Resume
   - RI# Indicator
3) **Generic Global Events** defined in the GBL_STS and GBL_EN registers. These registers are mainly used for SMI:
   - GP0 and GP1 Timer Time Out
   - Secondary Event Timer Time Out
   - Occurrence of Primary Events (defined in register PACT_STS and PACT_EN)
   - Legacy USB accesses (keyboard and mouse).

Once enabled, each of the EXTSMI inputs triggers an SCI or SMI at either the rising or the falling transition of the corresponding input pin signal. Software can check the status of the input pins via register EXTSMI_VAL and take proper actions.

Among many possible actions, the SCI and SMI routine can change the processor state by programming the P_BLK registers. The routine can also set the SLP_EN bit to put the system into one of the two suspend states:

1) **Suspend to Disk (or Soft-Off):** The VDD-5V power plane is turned off while VDD-5VSB and VDD-RTC planes remain on.
2) **Power-On-Suspend:** All power planes remain on but the processor is put in the C3 state.

In either suspend state, there is minimal interface between powered and non-powered planes.

The VT82C586B allows the following events to wake up the system from the two suspend states and from the C2 state to the normal working state (processor in C0 state):

- **Activation of External Inputs:** PWRBTN#, RI#, GPIO0 and other EXTSMI pins (see table below)
- **RTC Alarm and ACPI Power Management Timer** (see table below)
- **USB Resume Event** (see table below)
- **Interrupt Events** (always resume independent of any register setting)
- **ISA Master or DMA Events** (always resume independent of any register setting)

The VT82C586B also provides very flexible SCI/SMI steering and the PWRON control for these events:

Table 6. SCI/SMI/Resume Control for PM Events

Event	Global SCI/SMI Control	Individual Enable Bits for SCI & SMI	Separate Control for PWRON Resume
PWRBTN#	SCI_EN bit	N	**Y**
RI#	N	**Y**	**Y**
RTC Alarm	N	**Y**	N
GPIO0 (EXTSMI0)	N	**Y**	**Y**
External SCI/SMI (non-GPIO0)	N	**Y**	N
ACPI PM Timer	Always SCI	N	N
USB Resume	N	N	**Y**

Please refer to the table below on the availability of resume events in each type of suspend state.

Table 7. Suspend Resume Events and Conditions

Input Trigger	Power Plane	Soft Off	Power-On Suspend
PWRBTN#	VDD-5VSB	Y	Y
RI#	VDD-5VSB	Y	Y
RTC Alarm	VBAT	Y	Y
GPIO0 (EXTSMI0)	VDD-5VSB	Y	Y
External SCI/SMI (non-GPIO0)	VDD-5V	**N**	Y
ACPI PM Timer	VDD-5V	**N**	Y
USB Resume	VDD-5V	**N**	Y
PCI/ISA Interrupts	VDD-5V	**N**	**N**
PCI/ISA Master/DMA	VDD-5V	**N**	**N**

Legacy Power Management Timers

In addition to the ACPI power management timer, the VT82C586B includes the following four legacy power management timers:

GP0 Timer: general purpose timer with primary event

GP1 Timer: general purpose timer with peripheral event reload

Secondary Event Timer: to monitor secondary events

Conserve Mode Timer: not used in desktop applications

The normal sequence of operations for a general purpose timer (GP0 or GP1) is to

1) First program the time base and timer value of the initial count (register GP_TIM_CNT).
2) Then activate counting by setting the GP0_START or GP1_START bit to one: the timer will start with the initial count and count down towards 0.
3) When the timer counts down to zero, an SMI will be generated if enabled (GP0TO_EN and GP1TO_EN in the GBL_EN register) with status recorded (GP0TO_STS and GP1TO_STS in the GBL_STS register).
4) Each timer can also be programmed to reload the initial count and restart counting automatically after counting down to 0. This feature is not used in standard VIA BIOS.

The GP0 and GP1 timers can be used just as the general purpose timers described above. However, they can also be programmed to reload the initial count by system primary events or peripheral events thus used as primary event (global standby) timer and peripheral timer, respectively. The secondary event timer is solely used to monitor secondary events.

System Primary and Secondary Events

Primary system events are distinguished in the PRI_ACT_STS and PRI_ACT_EN registers:

Bit	Event	Trigger
7	**Keyboard Access**	I/O port 60h
6	**Serial Port Access**	I/O ports 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, or 2E8h-2EFh
5	**Parallel Port Access**	I/O ports 378h-37Fh or 278h-27Fh
4	**Video Access**	I/O ports 3B0h-3DFh or memory A/B segments
3	**IDE/Floppy Access**	I/O ports 1F0h-1F7h, 170h-177h, or 3F5h
2	**Reserved**	
1	**Primary Interrupts**	Each channel of the interrupt controller can be programmed to be a primary or secondary interrupt
0	**ISA Master/DMA Activity**	

Each category can be enabled as a primary event by setting the corresponding bit of the PRI_ACT_EN register to 1. If enabled, the occurrence of the primary event reloads the GP0 timer if the PACT_GP0_EN bit is also set to 1. The cause of the timer reload is recorded in the corresponding bit of PRI_ACT_STS register while the timer is reloaded. If no enabled primary event occurs during the count down, the GP0 timer will time out (count down to 0) and the system can be programmed (setting the GP0TO_EN bit in the GBL_EN register to one) to trigger an SMI to switch the system to a power down mode.

The VT82C586B distinguishes two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary events, the occurrence of a primary interrupt demands that the system be restored to full processing capability. Secondary interrupts, however, are typically used for housekeeping tasks in the background unnoticeable to the user. The VT82C586B allows each channel of interrupt request to be declared as either primary, secondary, or ignorable in the PIRQ_CH and SIRQ_CH registers. Secondary interrupts are the only system secondary events defined in the VT82C586B.

Like primary events, primary interrupts can be made to reload the GP0 timer by setting the PIRQ_EN bit to 1. Secondary interrupts do not reload the GP0 timer. Therefore the GP0 timer will time out and the SMI routine can put the system into power down mode if no events other than secondary interrupts are happening periodically in the background.

Primary events can be programmed to trigger an SMI (setting of the PACT_EN bit). Typically, this SMI triggering is turned off during normal system operation to avoid degrading system performance. Triggering is turned on by the SMI routine before entering the power down mode so that the system may be returned to normal operation at the occurrence of primary events. At the same time, the GP0 timer is reloaded and the count down process is restarted.

Peripheral Events

Primary and secondary events define system events in general and the response is typically expressed in terms of system events. Individual peripheral events can also be monitored by the VT82C586B through the GP1 timer. The following four categories of peripheral events are distinguished (via register GP_RLD_EN):

Bit-7 **Keyboard Access**
Bit-6 **Serial Port Access**
Bit-4 **Video Access**
Bit-3 **IDE/Floppy Access**

The four categories are subsets of the primary events as defined in PRI_ACT_EN and the occurrence of these events can be checked through a common register PRI_ACT_STS. As a peripheral timer, GP1 can be used to monitor one (or more than one) of the above four device types by programming the corresponding bit to one and the other bits to zero. Time out of the GP1 timer indicates no activity of the corresponding device type and appropriate action can be taken as a result.

Power Management I/O-Space Registers

Basic Power Management Control and Status

Offset 1-0 - Power Management Status.....RWC

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

15 **Wakeup Status** (WAK_STS) ..... default = 0
This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).

14-12 **Reserved** ..... always reads 0

11 **Power Button Override Status** (PBOR_STS). def=0
This bit is set when the PWRBTN# input pin is continuously asserted for more than 4 seconds. The setting of this bit will reset the PB_STS bit and transition the system into the soft off state.

10 **RTC Status** (RTC_STS) ..... default = 0
This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).

9 **Reserved** ..... always reads 0

8 **Power Button Status** (PB_STS)..... default = 0
This bit is set when the PWRBTN# signal is asserted LOW. If the PWRBTN# signal is held LOW for more than four seconds, this bit is cleared, the PBOR_STS bit is set, and the system will transition into the soft off state.

7-6 **Reserved** ..... always reads 0

5 **Global Status** (GBL_STS)..... default = 0
This bit is set by hardware when BIOS_RLS is set (typically by an SMI routine to release control of the SCI/SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS_RLS bit is also cleared at the same time by hardware.

4 **Bus Master Status** (BM_STS) ..... default = 0
This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.

3-1 **Reserved** ..... always reads 0

0 **Timer Carry Status** (TMR_STS)..... default = 0
The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

Offset 3-2 - Power Management Enable ..... RW

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

15 **Reserved** .....always reads 0

14-12 **Reserved** .....always reads 0

11 **Reserved** .....always reads 0

10 **RTC Enable** (RTC_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the RTC_STS bit is set.

9 **Reserved** .....always reads 0

8 **Power Button Enable** (PB_EN) .....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the PB_STS bit is set.

7-6 **Reserved** .....always reads 0

5 **Global Enable** (GBL_EN).....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the GBL_STS bit is set.

4 **Reserved** .....always reads 0

3-1 **Reserved** .....always reads 0

0 **ACPI Timer Enable** (TMR_EN) .....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI_EN bit) to be generated when the TMR_STS bit is set.

Offset 5-4 - Power Management Control .....RW

15-14 Reserved ..... always reads 0

13 Sleep Enable (SLP_EN)..... always reads 0
This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the SLP_TYP field.

12-10 Sleep Type (SLP_TYP)
- 000 Soft Off (also called Suspend to Disk). The VDD5 power plane is turned off while the VDD-5VSB and VDD-RTC (VBAT) planes remain on.
- 010 Power On Suspend. All power planes remain on but the processor is put into the C3 state.
- 0x1 Reserved
- 1xx Reserved

In either sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.

9-3 Reserved ..... always reads 0

2 Global Release (GBL_RLS) ..... default = 0
This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS_STS bit. The bit is cleared by hardware when the BIOS_STS bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS_EN bit is set (bit-5 of the Global Enable register at offset 2Ah).

1 Bus Master Reload (BMS_RLD)..... default = 0
This bit is used to enable the occurrence of a bus master request to transition the processor from the C3 state to the C0 state.

0 SCI Enable (SCI_EN)..... default = 0
Selects the power management event to generate either an SCI or SMI:
- 0 Generate SMI
- 1 Generate SCI

Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24). Also, TMR_STS & GBL_STS always generate SCI and BIOS_STS always generates SMI.

Offset 0B-08 - Power Management Timer..... RW

31-24 Extended Timer Value (ETM_VAL)
This field reads back 0 if the 24-bit timer option is selected (Rx41 bit-3).

23-0 Timer Value (TMR_VAL)
This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers

Offset 13-10 - Processor Control.....RW

31-5 Reserved ..... always reads 0

4 Throttling Enable (THT_EN).

3040 Silicon: This bit determines the effect of reading the "Processor Level 2" (P_LVL2) port:

0 No clock throttling. Reads from the Processor Level 2 register are ignored.

1 Reading the "Processor Level 2" port enables clock throttling by modulating the STPCLK# signal with a duty cycle determined bits 3-1 of this register.

3041 Silicon: Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state (i.e., it is not necessary to read the "Processor Level 2" port to start clock throttling). The throttling duty cycle is determined by bits 3-1 of this register.

3-1 Throttling Duty Cycle (THT_DTY)

This 3-bit field determines the duty cycle of the STPCLK# signal when the system is in throttling mode (the "Throttling Enable" bit is set to one and, in 3040 silicon, the "Processor Level 2" register is read). The duty cycle indicates the percentage of time the STPCLK# signal is asserted while the Throttling Enable bit is set. The field is decoded as follows:

000 Reserved
001 0-12.5%
010 12.5-25%
011 25-37.5%
100 37.5-50%
101 50-62.5%
110 62.5-75%
111 75-87.5%

0 Reserved ..... always reads 0

Offset 14 - Processor Level 2 (P_LVL2) ..... RO

7-0 Level 2 ..... always reads 0

3040 Silicon: Reads from this register put the processor in the C2 clock state if the Throttling Enable bit (Function 3 Rx10 bit-4) is set.

3041 Silicon: Reads from this register put the processor into the Stop Clock state (the VT82C586B asserts STPCLK# to suspend the processor). Wake up from Stop Clock state is by interrupt (INTR, SMI, PWRBTN#, RTC wakeup, or pin toggle SCI).

Reads from this register return all zeros; writes to this register have no effect.

Offset 15 - Processor Level 3 (P_LVL3) ..... RO

7-0 Level 3 ..... always reads 0

Reads from this register put the processor in the C3 clock state with the STPCLK# signal asserted. **3041 silicon:** wake up from Stop Clock state is by interrupt (INTR, SMI, PWRBTN#, RTC wakeup, or pin toggle SCI).

Reads from this register return all zeros; writes to this register have no effect.

General Purpose Power Management Registers

Offset 21-20 - General Purpose Status (GP_STS) .....RWC

15-10 Reserved ..... always reads 0

9 USB Resume Status (USB_STS)
This bit is set when a USB peripheral generates a resume event.

8 Ring Status (RI_STS)
This bit is set when the RI# input is asserted low.

7 EXTSMI7 Toggle Status (EXT7_STS)
This bit is set when the EXTSMI7# pin is toggled.

6 EXTSMI6 Toggle Status (EXT6_STS)
This bit is set when the EXTSMI6# pin is toggled.

5 EXTSMI5 Toggle Status (EXT5_STS)
This bit is set when the EXTSMI5# pin is toggled.

4 EXTSMI4 Toggle Status (EXT4_STS)
This bit is set when the EXTSMI4# pin is toggled.

3 EXTSMI3 Toggle Status (EXT3_STS)
This bit is set when the EXTSMI3# pin is toggled.

2 EXTSMI2 Toggle Status (EXT2_STS)
This bit is set when the EXTSMI2# pin is toggled.

1 EXTSMI1 Toggle Status (EXT1_STS)
This bit is set when the EXTSMI1# pin is toggled.

0 EXTSMI0 Toggle Status (EXT0_STS)
This bit is set when the EXTSMI0# pin is toggled.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one.

The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

Offset 23-22 - General Purpose SCI Enable ..... RW

15-10 Reserved .....always reads 0

9 Enable SCI on setting of the USB_STS bit ....def=0

8 Enable SCI on setting of the RI_STS bit .....def=0

7 Enable SCI on setting of the EXT7_STS bit ..def=0

6 Enable SCI on setting of the EXT6_STS bit ..def=0

5 Enable SCI on setting of the EXT5_STS bit ..def=0

4 Enable SCI on setting of the EXT4_STS bit ..def=0

3 Enable SCI on setting of the EXT3_STS bit ..def=0

2 Enable SCI on setting of the EXT2_STS bit ..def=0

1 Enable SCI on setting of the EXT1_STS bit ..def=0

0 Enable SCI on setting of the EXT0_STS bit ..def=0

These bits allow generation of an SCI using a separate set of conditions from those used for generating an SMI.

Offset 25-24 - General Purpose SMI Enable ..... RW

15-10 Reserved .....always reads 0

9 Enable SMI on setting of the USB_STS bit ...def=0

8 Enable SMI on setting of the RI_STS bit .....def=0

7 Enable SMI on setting of the EXT7_STS bit..def=0

6 Enable SMI on setting of the EXT6_STS bit..def=0

5 Enable SMI on setting of the EXT5_STS bit..def=0

4 Enable SMI on setting of the EXT4_STS bit..def=0

3 Enable SMI on setting of the EXT3_STS bit..def=0

2 Enable SMI on setting of the EXT2_STS bit..def=0

1 Enable SMI on setting of the EXT1_STS bit..def=0

0 Enable SMI on setting of the EXT0_STS bit..def=0

These bits allow generation of an SMI using a separate set of conditions from those used for generating an SCI.

Offset 27-26 - Power Supply Control..... RW

15-11 Reserved .....always reads 0

10 Ring PS Control (RI_PS_CTL) .....def=0
This bit enables the setting of the RI_STS bit to turn on the VDD_5V power plane by setting PWRON = 1.

9 Power Button Control (PB_CTL) .....def=1
This bit is used to control the setting of the PB_STS bit to resume the system from suspend (turn on the VDD_5V power plane by setting PWRON = 1).

8 RTC PS Control (RTC_PS_CTL) .....def=0
This bit enables the setting of the RTC_STS bit to resume the system from suspend (turn on the VDD_5V power plane by setting PWRON = 1).

7-1 Reserved .....always reads 0

0 EXTSMI0 Toggle PS Control (E0_PS_CTL) def=0
This bit enables the setting of the EXT0_STS bit to resume the system from suspend (turn on the VDD_5V power plane by setting PWRON = 1).

Generic Power Management Registers

Offset 29-28 - Global Status .....RWC

15-7 Reserved ..... always reads 0

6 Software SMI Status (SW_SMI_STS)..... def=0
This bit is set when the SMI_CMD port (offset 2F) is written.

5 BIOS Status (BIOS_STS)..... def=0
This bit is set when the GBL_RLS bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the GBL_RLS bit is reset at the same time by hardware.

4 Legacy USB Status (LEG_USB_STS)..... def=0
This bit is set when a legacy USB event occurs.

3 GP1 Timer Time Out Status (GP1TO_STS).. def=0
This bit is set when the GP1 timer times out.

2 GP0 Timer Time Out Status (GP0TO_STS).. def=0
This bit is set when the GP0 timer times out.

1 Secondary Event Timer Time Out Status (STTO_STS)..... def=0
This bit is set when the secondary event timer times out.

0 Primary Activity Status (PACT_STS)..... def=0
This bit is set at the occurrence of any enabled primary system activity (see the Primary Activity Detect Status register at offset 30h and the Primary Activity Detect Enable register at offset 34h). After checking this bit, software can check the status bits in the Primary Activity Detect Status register at offset 30h to identify the specific source of the primary event. Note that setting this bit can be enabled to reload the GP0 timer (see bit-0 of the GP Timer Reload Enable register at offset 38).

Note that SMI can be generated based on the setting of any of the above bits (see the offset 2Ah Global Enable register bit descriptions in the right hand column of this page).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.

Offset 2B-2A - Global Enable ..... RW

15-7 Reserved ..... always reads 0

6 Software SMI Enable (SW_SMI_EN)..... def=0
This bit may be set to trigger an SMI to be generated when the SW_SMI_STS bit is set.

5 BIOS Enable (BIOS_EN)..... def=0
This bit may be set to trigger an SMI to be generated when the BIOS_STS bit is set.

4 Legacy USB Enable (LEG_USB_EN)..... def=0
This bit may be set to trigger an SMI to be generated when the LEG_USB_STS bit is set.

3 GP1 Timer Time Out Enable (GP1TO_EN) .. def=0
This bit may be set to trigger an SMI to be generated when the GP1TO_STS bit is set.

2 GP0 Timer Time Out Enable (GP0TO_EN) .. def=0
This bit may be set to trigger an SMI to be generated when the GP0TO_STS bit is set.

1 Secondary Event Timer Time Out Enable (STTO_EN) ..... def=0
This bit may be set to trigger an SMI to be generated when the STTO_STS bit is set.

0 Primary Activity Enable (PACT_EN)..... def=0
This bit may be set to trigger an SMI to be generated when the PACT_STS bit is set.

Offset 2D-2C - Global Control (GBL_CTL).....RW

15-9 Reserved ..... always reads 0

8 SMI Active (INSMI)

0 SMI Inactive.....default

1 SMI Active. If the SMIIG bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.

7-5 Reserved ..... always reads 0

4 SMI Lock (SMIIG)

0 Disable SMI Lock .....default

1 Enable SMI Lock (SMI low to gate for the next SMI).

3 Reserved ..... always reads 0

2 Power Button Triggering

0 SCI/SMI generated by PWRBTN# low level

1 SCI/SMI generated by PWRBTN# rising edge

Set to one to avoid the situation where PB_STS is set to wake up the system then reset again by PBOR_STS to switch the system into the soft-off state. Must be set to 0 for ACPI v0.9 compliance.

1 BIOS Release (BIOS_RLS)

This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the GBL_STS bit. This bit is cleared by hardware when the GBL_STS bit cleared by software.

Note that if the GBL_EN bit is set (bit-5 of the Power Management Enable register at offset 2), then setting this bit causes an SCI to be generated (because setting this bit causes the GBL_STS bit to be set).

0 SMI Enable (SMI_EN)

0 Disable all SMI generation

1 Enable SMI generation

Offset 2F - SMI Command (SMI_CMD).....3041: RW .....3040: WO, always reads 0 (Read at Func 3 Rx47)

7-0 SMI Command

Writing to this port sets the SW_SMI_STS bit. Note that if the SW_SMI_EN bit is set (see bit-6 of the Global Enable register at offset 2Ah), then an SMI is generated.

Offset 33-30 - Primary Activity Detect Status .....RWC

These bits correspond to the Primary Activity Detect Enable bits in offset 37-34.

31-8 Reserved .....always read 0

7 Keyboard Controller Access Status..... (KBC_STS)
Set if the keyboard controller is accessed via I/O port 60h.

6 Serial Port Access Status..... (SER_STS)
Set if the serial port is accessed via I/O ports 3F8-3FFh, 2F8-2FFh, 3E8-3EFh, or 2E8-2Efh (COM1-4, respectively).

5 Parallel Port Access Status.....(PAR_STS)
Set if the parallel port is accessed via I/.O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).

4 Video Access Status.....(VID_STS)
Set if the video port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.

3 IDE / Floppy Access Status .....(IDE_STS)
Set if the IDE or floppy devices are accessed via I/O ports 1F0-1F7h, 170-177h or 3F5h.

2 Reserved ..... default=0

1 Primary Interrupt Activity Status..... (PIRQ_STS)
Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Function 3 PCI configuration register offset 44h).

0 ISA Master / DMA Activity Status..... (DRQ_STS)
Set on the occurrence of ISA master or DMA activity.

Note: The bits above correspond to the bits of the Primary Activity Detect Enable register at offset 34 (see right hand column of this page): if the corresponding bit is set in that register, setting of the above bits will cause the PACT_STS bit to be set (bit-0 of the Global Status register at offset 28). Setting of PACT_STS may be set up to enable a "Primary Activity Event": an SMI will be generated if PACT_EN is set (bit-0 of the Global Enable register at offset 2Ah) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (bit-0 of the GP Timer Reload Enable register at offset 38 on this page).

Note: Bits 3-7 above also correspond to bits 3-7 of the GP Timer Reload Enable register at offset 38 (see right hand column of this page): if the corresponding bit is set in that register, setting the bit in this register will cause the GP1 timer to be reloaded.

All bits of this register are set by hardware only and may only be cleared by writing a one to the desired bit. All bits default to 0.

Offset 37-34 - Primary Activity Detect Enable..... RW

These bits correspond to the Primary Activity Detect Status bits in offset 33-30.

31-8 Reserved ..... always read 0

7 Keyboard Controller Status Enable ..... (KBC_EN)
0 Don't set PACT_STS if KBC_STS is set..... def
1 Set PACT_STS if KBC_STS is set

6 Serial Port Status Enable..... (SER_EN)
0 Don't set PACT_STS if SER_STS is set..... def
1 Set PACT_STS if SER_STS is set

5 Parallel Port Status Enable .....(PAR_EN)
0 Don't set PACT_STS if PAR_STS is set ..... def
1 Set PACT_STS if PAR_STS is set

4 Video Status Enable .....(VID_EN)
0 Don't set PACT_STS if VID_STS is set..... def
1 Set PACT_STS if VID_STS is set

3 IDE / Floppy Status Enable .....(IDE_EN)
0 Don't set PACT_STS if IDE_STS is set ..... def
1 Set PACT_STS if IDE_STS is set

2 Reserved ..... default

1 Primary INTR Status Enable ..... (PIRQ_EN)
0 Don't set PACT_STS if PIRQ_STS is set.... def
1 Set PACT_STS if PIRQ_STS is set

0 ISA Master / DMA Status Enable..... (DRQ_EN)
0 Don't set PACT_STS if DRQ_STS is set .... def
1 Set PACT_STS if DRQ_STS is set

Note: Setting of any of the above bits also sets the PACT_STS bit (bit-0 of offset 28) which causes the GP0 timer to be reloaded (if PACT_GP0_EN is set) or generates an SMI (if PACT_EN is set).

Offset 3B-38 - GP Timer Reload Enable..... RW

All bits in this register default to 0 on power up.

31-8 Reserved ..... always read 0

7 Enable GP1 Timer Reload on KBC Access
1 = setting of KBC_STS causes GP1 timer to reload.

6 Enable GP1 Timer Reload on Serial Port Access
1 = setting of SER_STS causes GP1 timer to reload.

5 Reserved ..... always read 0

4 Enable GP1 Timer Reload on Video Access
1 = setting of VID_STS causes GP1 timer to reload.

3 Enable GP1 Timer Reload on IDE/Floppy Access
1 = setting of IDE_STS causes GP1 timer to reload.

2-1 Reserved ..... always read 0

0 Enable GP0 Timer Reload on Primary Activity
1 = setting of PACT_STS causes GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

General Purpose I/O Registers

Offset 40 - GPIO Direction Control (GPIO_DIR).....RW

7 Reserved .....always read 0

6 SMI/SCI Event Disable on GPIO3/GPIO4
- 0 Enable GPIO3/GPIO4 to cause SCI/SMI Events.....default
- 1 GPIO3/GPIO4 will only cause SCI/SMI Events during Power-On-Suspend (POS) mode

5 Interrupt Resume from Power-On Suspend
- 0 Enable (resume on interrupt from POS)..... def
- 1 Disable (ignore interrupts during POS)

4 GPIO4_DIR
- 0 Pin 136 is GPIO4 input .....default
- 1 Pin 136 is GPIO4 output (if Rx40 bit-7 = 1)

If Rx40[7]=0 (PCI Configuration function 3 offset 40h GPIO4_CFG bit), pin 136 is the GPO_WE output, independent of the state of this bit.

3 GPIO3_DIR
- 0 Pin 92 is GPIO3 input .....default
- 1 Pin 92 is GPIO3 output (if Rx40 bit-6 = 1)

If Rx40[6]=0 (PCI Configuration function 3 offset 40h GPIO3_CFG bit), pin 92 is the GPI_RE# output, independent of the state of this bit.

2 GPIO2_DIR
- 0 Pin 88 is GPIO2 / I2CD1 input .....default
- 1 Pin 88 is GPIO2 / I2CD1 output

1 GPIO1_DIR
- 0 Pin 87 is GPIO1 / I2CD2 input .....default
- 1 Pin 87 is GPIO1 / I2CD2 output

0 GPIO0_DIR
- 0 Pin 94 is GPIO0 input .....default
- 1 Pin 94 is GPIO0 output

Offset 42 - GPIO Port Output Value (GPIO_VAL) ..... RW

7-5 Reserved .....always reads 0

4 GPIO4_VAL
Write output value for the GPIO4 pin if the port is available (GPIO4_CFG = 1 in PCI Config Register function 3 offset 40h). The input state of the GPIO4 pin may be read from register EXTSMI_VAL bit-4.

3 GPIO3_VAL
Write output value for the GPIO3 pin if the port is available (GPIO3_CFG = 1 in PCI Config Register function 3 offset 40h). The input state of the GPIO3 pin may be read from register EXTSMI_VAL bit-3.

2 GPIO2_VAL
Write output value for the GPIO2 (I2CD2) pin. The input state of the GPIO2 pin may be read from register EXTSMI_VAL bit-2.

1 GPIO1_VAL
Write output value for the GPIO1 (I2CD1) pin. The input state of the GPIO1 pin may be read from register EXTSMI_VAL bit-1.

0 GPIO0_VAL
Write output value for the GPIO0 pin. The input state of the GPIO0 pin may be read from register EXTSMI_VAL bit-0.

Offset 44 - GPIO Port Input Value (EXTSMI_VAL)..... RO

Depending on the configuration, up to 8 external SCI/SMI ports are available as indicated below. The state of these inputs may be read in this register.

7 EXTSMI7# Input Value
GPIO3_CFG=0: EXTSMI7# on XD7 (pin 122)
GPIO3_CFG=1: EXTSMI7# function not available

6 EXTSMI6# Input Value
GPIO3_CFG=0: EXTSMI6# on XD6 (pin 121)
GPIO3_CFG=1: EXTSMI6# function not available

5 EXTSMI5# Input Value
GPIO3_CFG=0: EXTSMI5# on XD5 (pin 119)
GPIO3_CFG=1: EXTSMI5# function not available

4 EXTSMI4# Input Value
GPIO4_CFG=0:
GPIO3_CFG=0: EXTSMI4# on XD4 (pin 118)
GPIO3_CFG=1: EXTSMI4# function not avail
GPIO4_CFG=1: EXTSMI4# on GPIO4 (pin 136)

3 EXTSMI3# Input Value
GPIO3_CFG=0: EXTSMI3# on XD3 (pin 117)
GPIO3_CFG=1: EXTSMI3# on GPIO3 (pin 92)

2 EXTSMI2# Input Value (on GPIO2 pin 88)

1 EXTSMI1# Input Value (on GPIO1 pin 87)

0 EXTSMI0# Input Value (on GPIO0 pin 94)

Note: GPIO3_CFG and GPIO4_CFG are located in PCI Configuration Register function 3 offset 40h.

Offset 47-46 - GPO Port Output Value (GPO_VAL).....RW

Reads from this register return the last value written (held on chip).

15-8 GPO15-8 Value. Output port value for the external GPO port connected to SD15-8. This port is available only if the GPIO4_CFG bit is zero to define pin 136 as GPO_WE.

7-0 GPO7-0 Value. Output port value for the external GPO port connected to XD7-0. This port is available only if the GPIO4_CFG bit is zero to define pin 136 as GPO_WE.

GPIO4_CFG is in PCI Config Register function 3 offset 40h.

Offset 49-48 - GPI Port Input Value (GPI_VAL) ..... RO

Reads from this register are ignored (and return a value of 0).

15-8 GPI15-8 Value. Input port value for the external GPI port connected to SD15-8. This port is available only if the GPIO3_CFG bit is zero to define pin 92 as GPI_RE#.

7-0 GPI7-0 Value. Input port value for the external GPI port connected to XD7-0. This port is available only if the GPIO3_CFG bit is zero to define pin 92 as GPI_RE#.

GPIO3_CFG is in PCI Config Register function 3 offset 40h.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storage temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	Volts
Output voltage (V_{DD} = 5V)	-0.5	5.5	Volts
Output voltage (V_{DD} = 3.1 - 3.6V)	-0.5	V_{DD} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{o}C, V_{DD}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-	80	mA	

AC Timing Specifications

Table 8. AC Characteristics - PCI Cycle Timing

	Parameter	Min	Max	Unit	Notes
T_S	AD[31:0] Setup Time to PCLK Rising	7		ns	
T_S	FRAME#,TRDY#,IRDY# Setup Time to PCLK Rising	7		ns	
T_S	CBE[3:0]#, STOP#,DEVSEL# Setup Time to PCLK Rising	7		ns	
T_S	PGNT# Setup Time to PCLK Rising	12		ns	
T_H	AD[31:0] Hold Time from PCLK Rising	0		ns	
T_H	FRAME#,TRDY#,IRDY# Hold Time from PCLK Rising	0		ns	
T_H	CBE[3:0]#, STOP#,DEVSEL# Hold Time from PCLK Rising	0		ns	
T_H	PGNT# Hold Time from PCLK Rising	0		ns	
T_{VD}	AD[31:0] Valid Delay from PCLK Rising (address phase)	2	11	ns	0pf on min, 50pf on max
T_{VD}	AD[31:0] Valid Delay from PCLK Rising (data phase)	2	11	ns	0pf on min, 50pf on max
T_{VD}	FRAME#,TRDY#,IRDY# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T_{VD}	CBE[3:0]#, STOP#,DEVSEL# Valid Delay from PCLK Rising	2	11	ns	0pf on min, 50pf on max
T_{VD}	PREQ# Valid Delay from PCLK Rising	2	12	ns	0pf on min, 50pf on max
T_{FD}	FRAME#,TRDY#,IRDY# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max
T_{FD}	CBE[3:0]#, STOP#,DEVSEL# Float Delay from PCLK Rising		28	ns	0pf on min, 50pf on max

Table 9. AC Characteristics - UltraDMA-33 IDE Bus Interface Timing

Symbol	Description	Timing	Unit
T_{ENV1}	Envelope time for read initial	29.3	ns
T_{DS1}	Data setup time for read initial	1.1	ns
T_{DH1}	Data hold time for read initial (rise)	2.3	ns
T_{ENV2}	Envelope time for write initial (rise)	29.3	ns
T_{DVS2}	Data setup time for write initial (fall)	42.2	ns
T_{DVH2}	Data hold time for write initial (fall)	17.8	ns
T_{DVS2}	Data setup time for write initial	42.0	ns
T_{DVH2}	Data hold time for write initial	17.2	ns
T_{RFS}	READY to final STROBE time	21.3	ns
T_{RP}	READY to Pause time	180.0	ns
T_{LI4}	Limited interlock time (to STOP)	95.1	ns
T_{LI4}	Limited interlock time (to Host DMARDY)	125.3	ns
T_{ZA4}	Delay time required for output drives turning on	102.0	ns
T_{DVS4}	Data setup time for read terminating	55.3	ns
T_{DVH4}	Data hold time for read terminating	31.6	ns
T_{LI5}	Limited interlock time (to STOP)	125.3	ns
T_{LI5}	Limited interlock time (to Host STROBE)	95.2	ns
T_{MIL5}	Limited interlock time with minimum	120.6	ns
T_{DVS5}	Data setup time for write terminating	57.7	ns
T_{DVH5}	Data hold time for write terminating	31.8	ns
T_{MIL6}	Limited interlock time with minimum	155.8	ns
T_{ZA6}	Delay time required for output drives turning on	68.5	ns
T_{LI5}	Limited interlock time	65.2	ns
T_{MIL5}	Limited interlock time with minimum	90.6	ns
T_2	Delay time of PCLK to DCS3,1#	4.8	ns
T_3	Delay time of PCLK to DA[2:0]	5.3	ns
T_4	Delay time of PCLK to DIOW#	9.3	ns
T_5	Delay time of PCLK to DIOR#	9.2	ns
T_{WDS}	Data setup time during PIO write	85.5	ns
T_{WDH}	Data hold time during PIO write	31.7	ns
T_{RDS}	Data setup time during PIO read	0.4	ns
T_{RDH}	Data hold time during PIO read	2.1	ns

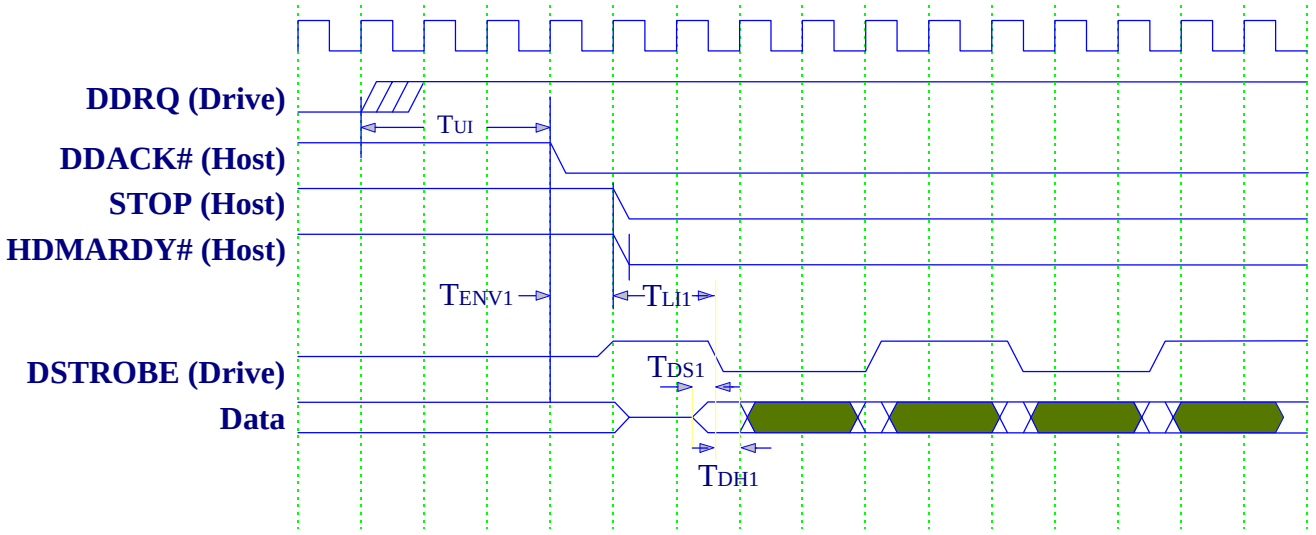

Figure 5. UltraDMA-33 IDE Timing - Drive Initiating DMA Burst for Read Command

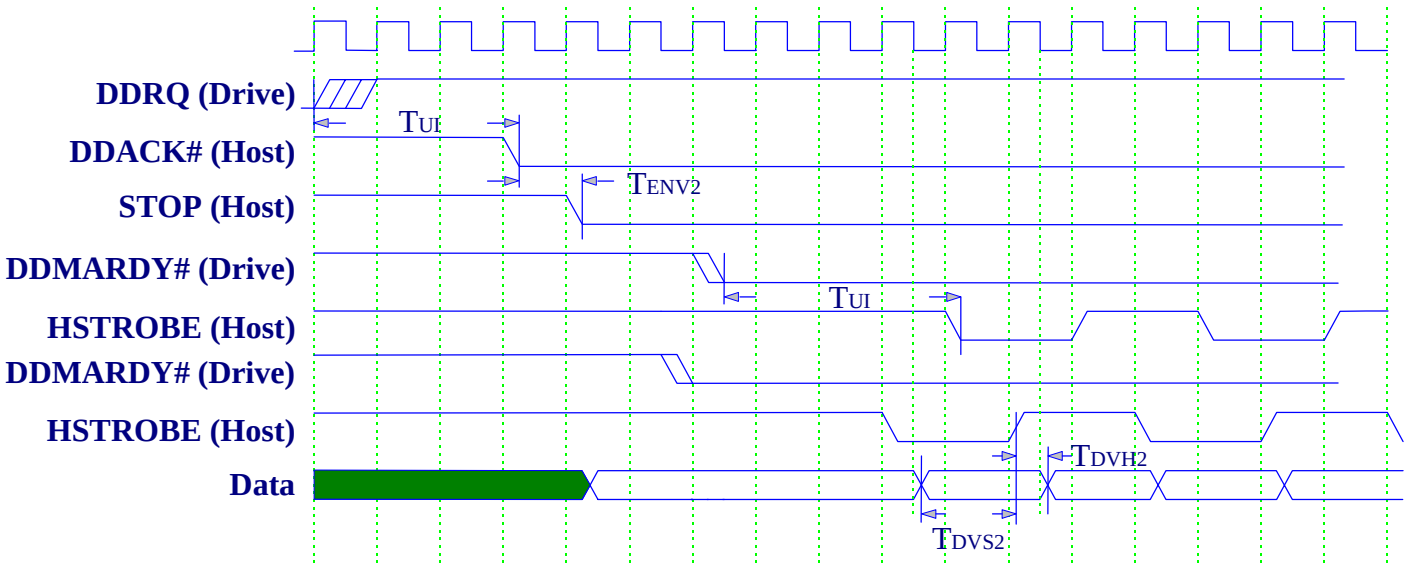

Figure 6. UltraDMA-33 IDE Timing - Drive Initiating Burst for Write Command

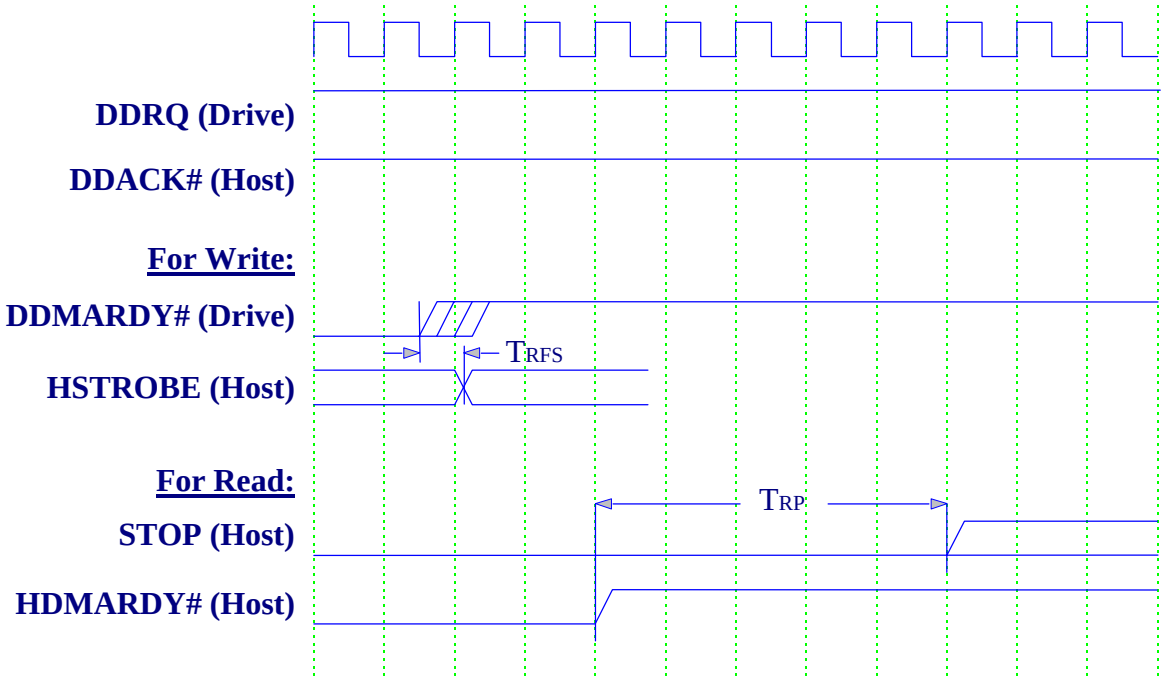

Figure 7. UltraDMA-33 IDE Timing - Pausing a DMA Burst

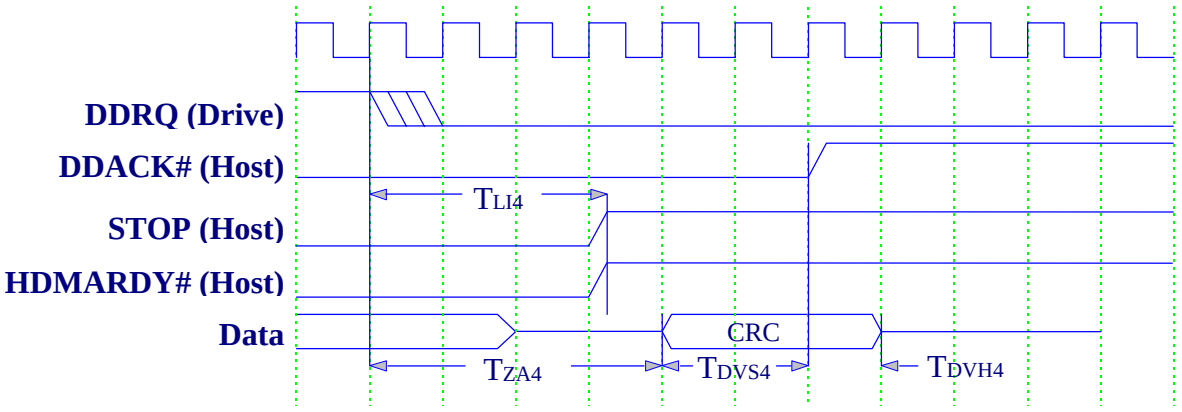

Figure 8. UltraDMA-33 IDE Timing - Drive Terminating DMA Burst During Read Command

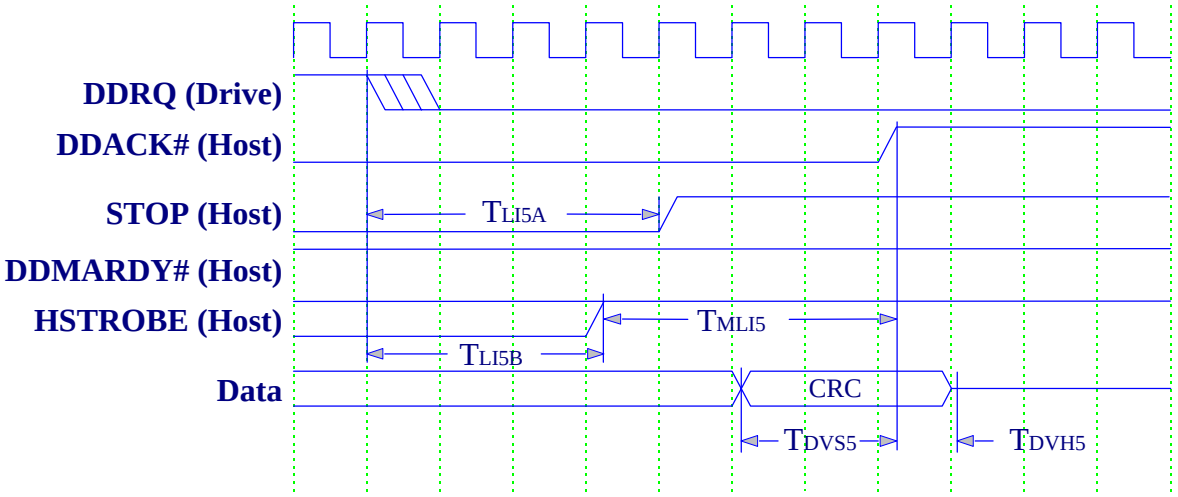

Figure 9. UltraDMA-33 IDE Timing - Drive Terminating DMA Burst During Write Command

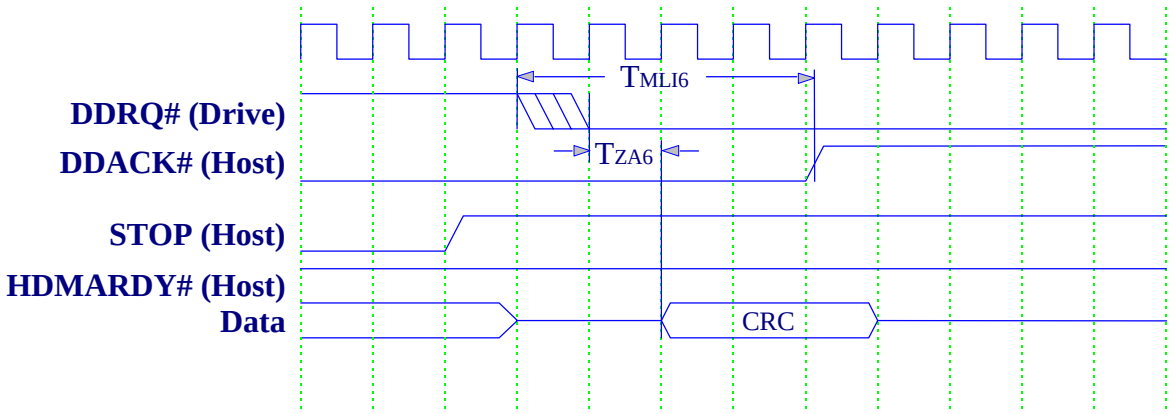

Figure 10. UltraDMA-33 IDE Timing - Host Terminating DMA Burst During Read Command

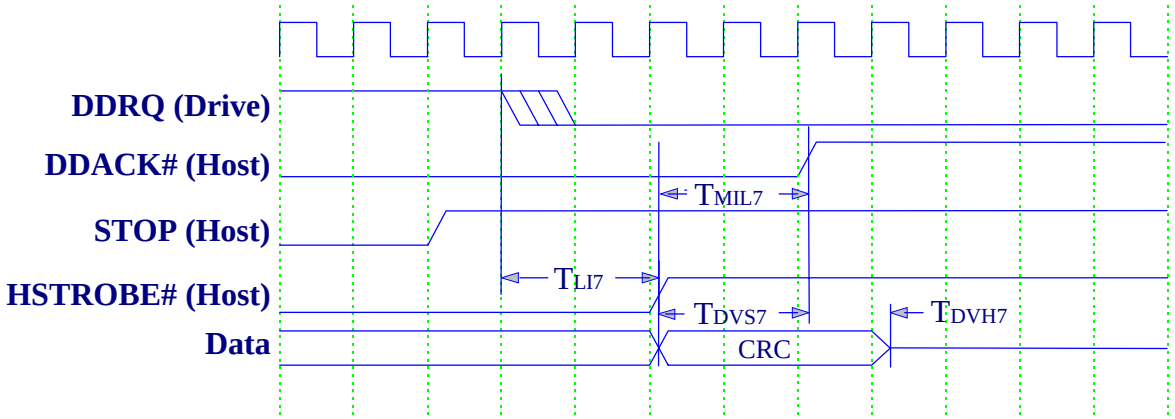

Figure 11. UltraDMA-33 IDE Timing - Host Terminating DMA Burst During Write Command

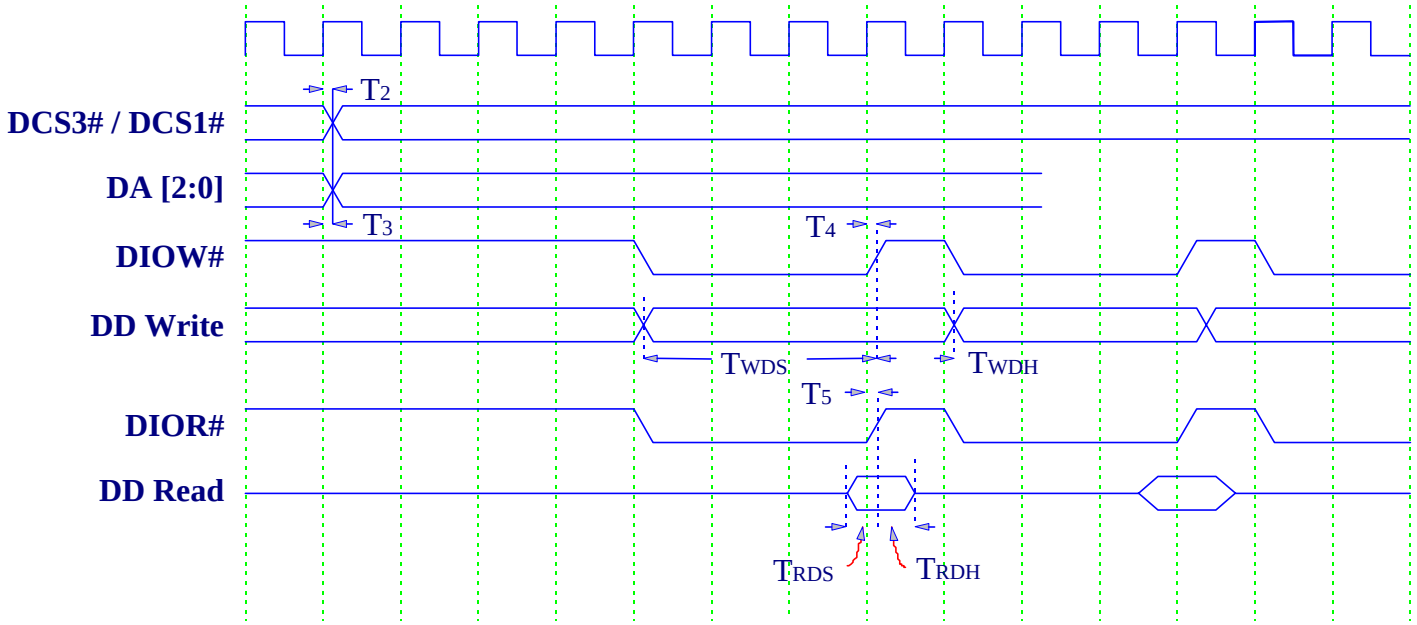

Figure 12. UltraDMA-33 IDE Timing - PIO Cycle

PACKAGE MECHANICAL SPECIFICATIONS

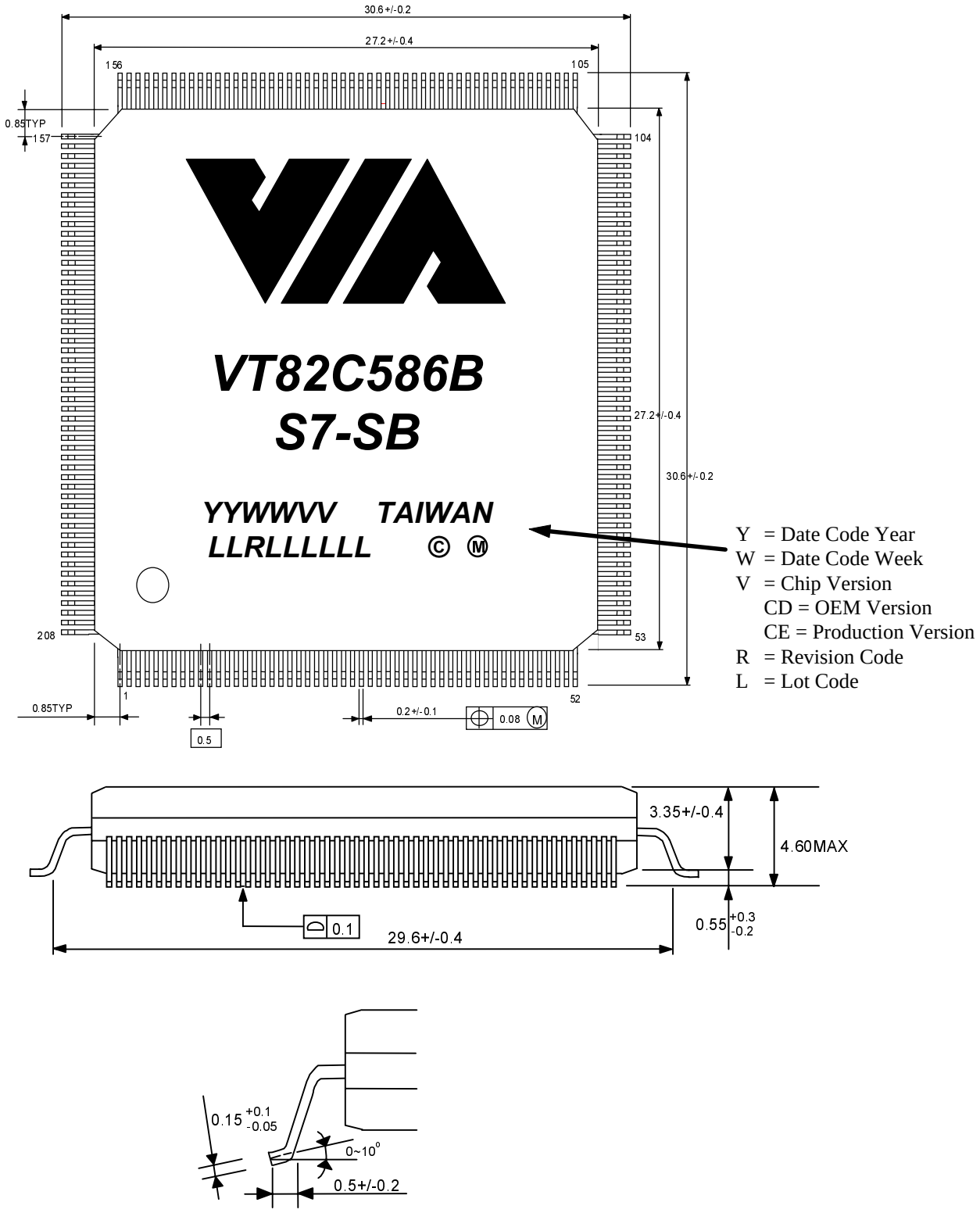

Figure 13. Mechanical Specifications - 208-Pin Plastic Flat Package