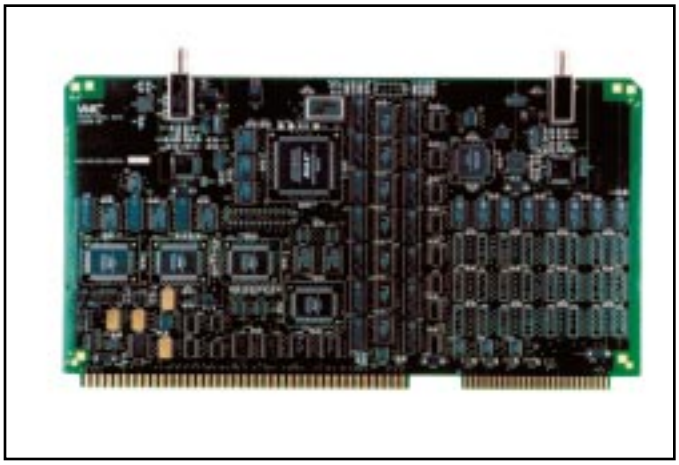
VMIMB1-5576
Multibus I Fiber-Optic Reflective Memory

- High-speed, easy-to-use fiber-optic network (170 Mbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Data transferred at 6.2 Mbyte/s without redundant transfer
- Data transferred at 3.2 Mbyte/s with redundant transfer
- Any node on the network can generate an interrupt in any other node with a single command
- Error detection
- Redundant transmission mode for suppressing errors
- No processor overhead
- No processor involvement in the operation of the network
- Up to 1 Mbyte of Reflective Memory
- Byte or word memory access
- Communication link compatible with the VMIVME-5576 and VMIPCI-5576
- ANSI/IEEE standard 796-1983 Multibus I-compliant board
- Also jumper configurable as a Reliance AutoMax Multibus-compatible board



INTRODUCTION — The VMIMB1-5576 is a Multibus I board which may be used with other 5576 family boards to form a high-performance, daisy-chained, fiber-optic network. Data is transferred by writing to on-board global RAM. The data is automatically sent to the same location in memory on all Reflective Memory boards on the network. The network can include Multibus I, VMEbus, and PCI bus systems.

PRODUCT OVERVIEW — The Reflective Memory concept provides a very fast and efficient way of sharing data across distributed computer systems.

VMIC's VMIMB1-5576 Reflective Memory interface allows data to be shared between up to 256 independent systems (nodes) at rates up to 6.2 Mbyte/s. Each VMIMB1-5576 Reflective Memory board may be configured with 256 Kbyte, 512 Kbyte, or 1 Mbyte of on-board SRAM. The local SRAM provides fast Read access times to stored data. Writes are stored in local SRAM and broadcast over a high-speed, fiber-optic data path to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize CPU and bus performance to maintain high data throughput.

The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. Three separate, user-definable interrupts may be used to synchronize a system process, or used to follow any data that may have preceded it. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.

The VMIMB1-5576 requires no initialization unless interrupts are being used. If interrupts are used, both vectored and nonvectored interrupts are supported.

Each node on the system has a unique identification number between 0 and 255. The node number is established during hardware system integration by placement of jumpers on the board. This node number can be read by software by accessing an on-board register. In some applications, this node number would be useful in establishing the function of the node.

VMIMB1-5576 Multibus Reflective Memory has a jumper-selectable *little memory* option, which limits the accessible SRAM to 64 Kbyte. In addition, the little memory option activates several P2 connector inputs, which make the VMIMB1-5576 compatible with the Reliance AutoMax Multibus system.

LINK ARBITRATION — The VMIMB1-5576 system is a fiber-optic daisy chain ring as shown in Figure 1. Each transfer is passed from node to node until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives except those that it had originated. Nodes are allowed to insert transfers between transfers passing through.

INTERRUPT TRANSFERS — In addition to transferring data between nodes, the VMIMB1-5576 will allow any processor in any node to generate an interrupt on any other node. These interrupts would generally be used to indicate to the receiving node that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving node is ready for new data.

Three interrupts are available. The user may define the function, priority, and vector for each interrupt. Any processor can generate an interrupt on any other node on the network. In addition, any processor on the network can generate an interrupt on all nodes on the network. Interrupts are generated by simply writing to a single VMIMB1-5576 register.

Ordering Options								
January 14, 1998 800-335576-000 D	A	B	C	–	D	E	F	
VMIMB1-5576	–				–			

A = Memory Options
0 = 256 Kbyte
1 = 512 Kbyte
2 = 1 Mbyte
B = FIFO Option
0 = 512 Transfer FIFO
1 = 4 K Transfer FIFO
C = Enclosure Options
0 = No Enclosure (Standard Multibus)
1 = AutoMax Enclosure

Connector Data

Compatible Connector	*ST Connector*
PC Board Fiber-Optic Transmitter/Receiver	Fiber-Optic Receiver HFBR-2100 (Hewlett-Packard) Fiber-Optic Transmitter HFBR-1100 (Hewlett-Packard)

Cable Specifications

Fiber-Optic Cable – Multimode; 62.5 Micron core.
Transmitters operate at 1,300 nm at 170 Mbaud.
Maximum attenuation between nodes is 9 dB.
Minimum attenuation between nodes is .5 dB.

Fiber-Optic Cable Assemblies	A	B	C	–	D	E	F
VMICBL-000-F3	–			–			

A = Fiber-Optic Connector Type
0 = Ceramic Ferrule ST Connector
1 = Stainless Steel Ferrule ST Connector
BC = Cable Lengths

00 = Not Used	09 = 1,000 ft (304.8 m)
01 = 5 ft (1.5 m)	10 = 1,500 ft (457.3 m)
02 = 25 ft (7.6 m)	11 = 2,000 ft (609.7 m)
03 = 50 ft (15.2 m)	12 = 2,460 ft (750.0 m)
04 = 100 ft (30.4 m)	13 = 3,280 ft (1,000 m)
05 = 150 ft (45.7 m)	14 = 4,100 ft (1,250 m)
06 = 200 ft (60.9 m)	15 = 4,920 ft (1,500 m)
07 = 350 ft (106.7 m)	16 = 5,740 ft (1,750 m)
08 = 500 ft (152.4 m)	17 = 6,560 ft (2,000 m)

Note

VMIC offers single fiber cable assemblies that are compatible with the VMIVME-5576 in length ranging from 1.5 to 2,000 m. These cable assemblies are U.L./NEC-rated OFNP and have a 2.5 mm ST-style bayonet connector on each end.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

All data and interrupt command transfers contain the node number of the node that originated the transfer. This information is used primarily so the originating node can remove the transfer from the network after the transfer has traversed the ring. The node identification is also used by nodes receiving interrupt commands. When a node receives an interrupt command for itself, it places the identification number of the originating node in a FIFO. Up to 512 interrupts can be stacked in the FIFO. During the interrupt service routine, the identification of the interrupting node can be read from the FIFO.

ERROR MANAGEMENT — Errors are detected by the VMIMB1-5576 with the use of the error detection facilities of the TAXI chipset and additional parity encoding and checking. When a node detects an error, the erroneous transfer is removed from the system and a VMEbus interrupt is generated, if enabled. The error rate of the VMIMB1-5576 is a function of the rate of errors produced in the optical portion of the system. This optical error rate depends on the length and type of fiber-optic cable. Error rates of 10^{-12} are achievable. Assuming an optical error rate of 10^{-12}, the error rate of the VMIMB1-5576 is 10^{-10} transfers/transfer.

The VMIMB1-5576 can be operated in a redundant transfer mode in which each transfer is transmitted twice. In this mode of operation, the first of the two transfers is used unless an error is detected in which case the second transfer is used. In the event that an error is detected in both transfers, the node removes the transfer from the system. The probability of both transfers containing an error is 10^{-20}, or about one error every 3,731,000 years at maximum data rate.

PROTECTION AGAINST LOST DATA — Data received by the node from the fiber-optic cable is error checked and placed in a receive FIFO. Arbitration with accesses from the VMEbus then takes place and the data is written to the node's SRAM and to the node's transmit FIFO. Data written to the board from the VMEbus is placed directly into SRAM and into the transmit FIFO. Data in the transmit FIFO is transmitted by the node over the fiber-optic cable to the next node. Data could be lost if either FIFO were allowed to become full.

The product is designed to prevent either FIFO becoming full and overflowing. It is important to note the only way that data can start to accumulate in FIFOs is for data to enter the node at a rate greater than 6.2 Mbyte/s or 3.2 Mbyte/s in redundant mode. Since data can enter from the fiber and from the VMEbus, it is possible to exceed these rates. If the transmit FIFO becomes half-full, a bit in the Status Register is set and, if enabled, an interrupt is generated. This condition is an indication to the software in the node that writes to the Reflective Memory should be suspended until the FIFO becomes less than half-full. If the half-full indication is ignored and the transmit FIFO becomes full, then writes to the Reflective Memory will result in the VMIMB1-5576 'waiting' the Multibus by not issuing the bus acknowledge signal.

NETWORK MONITOR — There is a bit in a Status Register that can be used to verify that data is traversing the ring (that is, the ring is not broken). This can also be used to measure network latency.

SPECIFICATIONS

Memory Size: Little memory configuration - 64 K
Big memory configuration: 256 Kbyte, 512 Kbyte, or 1 Mbyte

Access Times:
Writes: 150 ns (best-case arbitration)
450 ns (worst-case arbitration)
Reads: 230 ns (best-case arbitration)
480 ns (worst-case arbitration)
Note: The above times are based on a Multibus I system capable of operating at the maximum speed per the specification. The actual access times are highly dependent on the Multibus I system used. The timing of typical Multibus systems vary significantly.

Network Transfer Rate: 6.2 Mbyte/s (longword accesses) without redundant transfer
3.2 Mbyte/s (longword accesses) with redundant transfer

COMPATIBILITY

Multibus: This product complies with the Multibus I specification (ANSI/IEEE STD 796-1983). The compliance levels are (D16) and (M20 or M24) and (V0 or V2). This product complies with the AutoMax Multibus Specification of Reliance, (revision date April 11, 1996).

Big Memory Configuration: Compatible with both the 20 address line (M20) and the 24 address line (M24) Multibus I systems.

Addressable on 256 Kbyte boundaries for the 256 Kbyte memory option.

Addressable on 512 Kbyte boundaries for the 512 Kbyte memory option.

Addressable on 1 Mbyte boundary for the 1 Mbyte memory option.

Little Memory Configuration: On-board jumpers can locate the 64 Kbyte of board memory on 64 Kbyte boundaries with the 1 Mbyte (20 address line) address space. Optionally, the on-board jumpers can be arranged to allow off-board address specification through the P2 connector as indicated by the AutoMax Multibus Specification.

Multibus Data Width: This product complies with the (D16) specification, which permits data transfers in both 8- and 16-bit widths.

Multibus Interrupts: This product is compatible with both the (V0) nonvectored interrupt convention and the (V2) two INTA cycle vectored interrupt convention. This product does not support the three INTA cycle vectored interrupt convention. The activation and modes of each interrupt are controlled through software accessible control registers.

AutoMax Multibus Compatibility: As mentioned above, the memory address can be specified through P2 pins defined by the AutoMax Multibus Specification. In addition, while in the little memory configuration, the unique AutoMax P2 signals MPRO/, WDOK/, and BDRST/ are also implemented. Also, the -xx1 option includes an AutoMax enclosure around the board.

Byte Swapping: The VMIMB1-5576 can be used in systems that incorporate *big-endian* CPUs such as the 680x0 processor family or *little-endian* CPUs such as the 80x86 processor family. The VMIMB1-5576 provides a byte-swapping feature for endian conversion.

INTERCONNECTION

Cable Requirements: Two fiber-optic cables

Cable Length: 2,000 m maximum between nodes

Configuration: Daisy chain ring up to 256 nodes

PHYSICAL/ENVIRONMENTAL

Temperature Range: 0 to 55 °C, operating
-40 to 85 °C, storage

Relative Humidity: 20 to 80 percent, noncondensing

Power Requirements: 2.1 A maximum at +5 VDC ±5 percent

DATA TRANSFERS

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the VMIMB1-5576 is shown in Figure 2.

TRADEMARKS

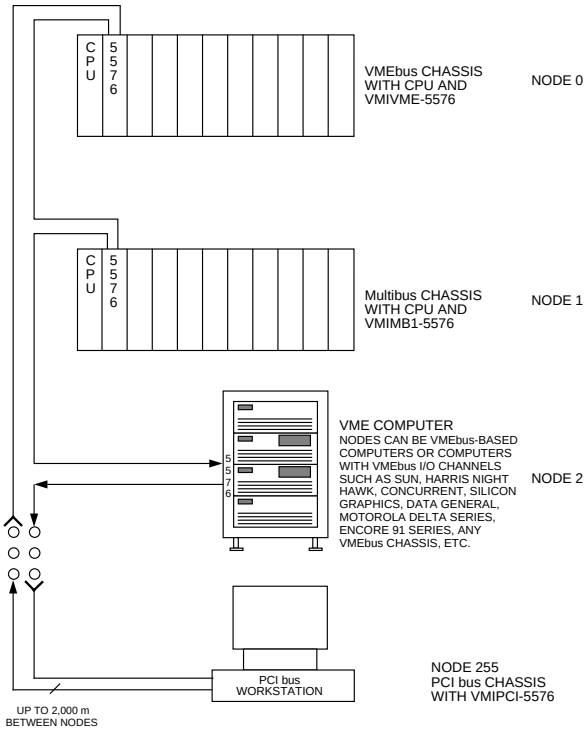


Figure 1. Network Example Using Reflective Memory System

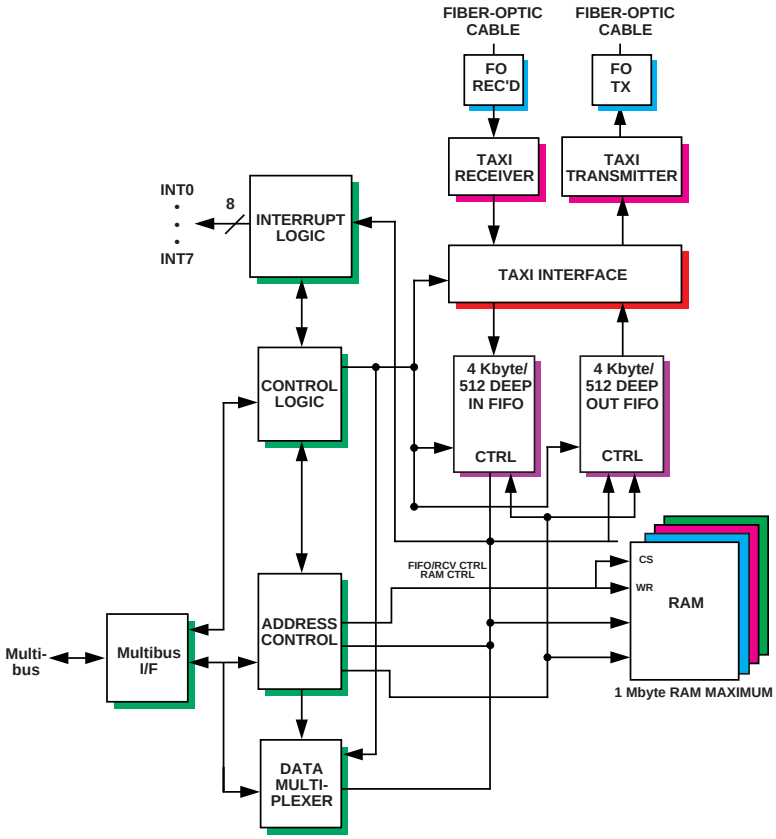


Figure 2. VMIMB1-5576 Functional Block Diagram