# IP MEZZANINE MODULES (ANSI/VITA 4)

# AVME9670/75 VME64, Nonintelligent, IP Carrier Cards

The AVME9670 and AVME9675 are nonintelligent slave boards that interface up to four IP modules to the VMEbus. The only difference is that the AVME9675 adds fully implemented geographical addressing. Both are full-height (6U) IP carrier cards that use VME64-compliant connectors to increase the quantity of rear I/O connections beyond that of standard VME. Although the rear connectors are VME64, the electrical interface is standard VME A24/A16. This means that nearly all CPU products (VME64 or not) can still enjoy full access to the IP modules.

When used with a VME64 backplane, the AVME9670 brings all 200 I/O points out the rear PO and P2 connectors. This convenience eliminates messy cables from hanging out the front of the cage. In addition to a cleaner cage design, it is also much easier to insert and replace boards into the system.

### **Features**

- Four industry-standard IP module slots
- 200 I/O points with rear access
- VME64x high-density rear connectors
- Full geographical addressing (AVME9675 only)
- Compatibility with most CPUs (VME A24/A16)
- Two interrupts per IP module
- Individually filtered and fused power to each IP
- Front panel LEDs

# **Benefits**

- Clean system cabling.
- Easy board replacement.
- Simplified debugging with status LEDs.



Mix and match plug-in modules with different I/O functions to quickly create custom I/O boards with hundreds of channels.

### Operation

Acromag's carrier boards provide full data access to the IP module's I/O, ID and memory spaces. With full access to the programmable registers, you can easily configure and control the operation of the IP modules from the VMEbus.

Up to two interrupt requests are supported for each IP module. The VMEbus interrupt level is software programmable.

Individual passive filters on each IP module power supply line provide optimum filtering and isolation between the IP modules and the carrier board.

# **Specifications**

### **IP Compliance (ANSI/VITA 4)**

Meets IP specifications per ANSI/VITA 4-1995 and ANSI/VITA 4.1-1996 for I/O mapping.

Electrical/mechanical interface: Supports single or double size IP modules. 32-bit IP modules are not supported.

- I/O space and ID space supported.
- Memory space: Supports 1MB to 8MB per IP module.
- Interrupts: Supports two interrupt requests per IP module and interrupt acknowledge cycles, D16/D08(0).

#### **VMEbus Compliance**

- Meets VME64 specifications per ANSI/VITA 1-1994 and VME64x specifications per ANSI/VITA 1.1-1997.
- Data transfer bus: A24/A16:D16/D08(EO) DTB slave; supports Read-Modify-Write cycles.
- VMEbus access time: 500nS typical (all carrier board registers); measured from the falling edge of DSx\* to the falling edge of DTACK\*. 500nS typical (IP registers with no wait states). IP register access time will increase by the number of wait states multiplied by 125nS (the period of the 8MHz clock).

Interrupts: Creates I(1-7) programmable request levels (up to two requests sourced from each IP module). Supports D16/D08(0) round-robin hardware interrupt prioritization of IP sources. Carrier registers supportinterrupt control and status monitoring. Interrupt release mechanism is Release on Register Access (RORA) type.

#### Environmental

Operating temperature: O to 70°C (AVME9670/75) or -40 to 85°C (AVME9670E/75E models).

Storage temperature: -55 to 100°C (all models). Relative humidity: 5 to 95% noncondensing.

# **Ordering Information**

- **AVME9670:** VME64x 6U carrier. Holds four IP modules. **AVME9670E:** Same as AVME9670 above plus extended temperature range.
- **AVME9675-4:** Same as AVME9670 plus geographical addressing. Holds four IP modules.
- **AVME9675-4E:** Same as AVME9675-4 above plus extended temperature range.
- **AVME9675-2:** Same as AVME9675-4 except it holds two IP modules.
- **AVME9675-2E:** Same as AVME9675-2 above plus extended temperature range.
- TRANS-200: Transition module.

For software, see Pages 32, 34. Termination products, see Page 38. Signal conditioning, see Page 66.

