General Standards Corporation

High Performance Bus Interface Solutions

PC104P-16AO2-MF

Two-Channel 16-Bit High-Speed Analog Output PMC Board

With 400,000 Samples per Second per Channel, and Independent Clocking

Features:

- Two Precision Differential 2-Wire High-Speed Analog Output Channels;
- 16-Bit Resolution; D/A Converter per Channel
- Data Rates to 400K Samples per Second per Channel; 800 KSPS Aggregate Rate
- Output Ranges of ±10V, ±5V or ±2.5V
- Two Independent 32 K-Sample Analog Output FIFO Buffers
- Output Data Buffer Sizes Adjustable from Four Samples to up to 32 K-Samples
- Continuous and Periodic-Function Buffer Modes
- Synchronous and Independent Clocking Modes
- Seamless Waveform Sequencing
- Data Rates Controlled by Independent Internal Clocks, or by an External Clock
- Supports Multiboard Synchronization;
- Software-Selectable TTL or Differential External Clock I/O
- Internal Autocalibration of Both Channels
- High Accuracy; 0.017% FSR max error on ±10V Range, INL = 0.007%
- Fast Settling; 5 us to 0.1%; 8 us to 0.01%;with No-filter Option
- Integral Shield Assures Minimum Susceptibility to Radiated Noise in PMC Environments
- VxWorks™ and NT Drivers™

Applications:

- ✓ Precision Voltage Source
- ✓ Industrial Robotics
- ✓ Audio Synthesis
- ✓ Acoustic Research
- ✓ Process Monitoring
- ✓ Arbitrary Functions
- ✓ Waveform Synthesis
- ✓ Acoustic Research
- ✓ Environmental Test

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Functional Description:

The PC104P-16AO2-MF board provides two independent 2-wire differential 16-bit D/A converter channels, and all supporting functions necessary for adding precision high-speed analog output capability to a PMC host. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and supports the "plug-n-play" initialization concept. Unique FIFO buffer controls support the seamless sequencing of successive waveforms. In less demanding applications, the outputs can be updated individually. Both TTL and differential I/O ports support multiboard synchronization.

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 16-bit local bus (Figure 1). Two analog output channels are controlled through independent analog output FIFO buffers, and can be updated either simultaneously or sequentially. The clocking rate for each output channel can be controlled either by a dedicated internal rate generator, or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including autocalibration. Analog output levels are initialized to zero (midrange).

Internal autocalibration networks permit calibration to be performed without removing the board or host from the system. This feature produces the optimum calibration situation, in which the board is calibrated in its actual operating environment

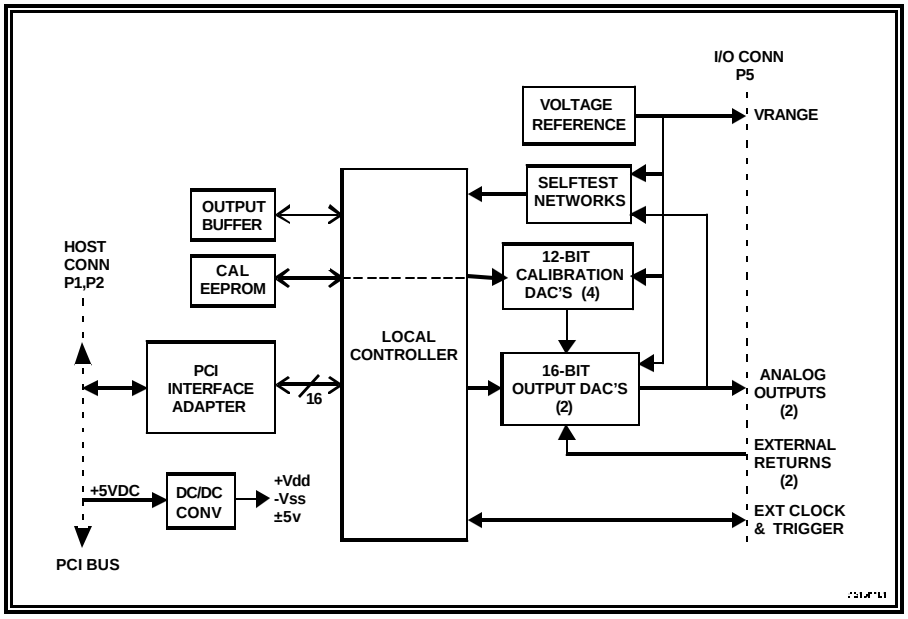

Figure 1. PC104P-16AO2-MF Board; Functional Organization

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All input and output system connections are made through a single metal-shrouded I/O connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

❑ Output Characteristics:

Configuration:	Two differential 2-wire analog output channels, with a dedicated 16-Bit DAC per channel
Voltage Ranges:	Factory configured as ±10 Volts, ±5 Volts or ±2.5 Volts
Output Resistance:	Output: 1.0 Ohm maximum; Return input resistance: 3 Kohms minimum.
Output protection:	Withstands sustained short-circuiting to ground without damage
Load Current:	±5 ma maximum
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Settling Time:	No Filter : 5 us to 0.1%, 8 us to 0.01% 10 kHz Filter: 130 us to 0.1%, 160 us to 0.01%
Noise:	No Filter: 4 mVRMS, 10Hz-10KHz 10 kHz Filter: 2 mVRMS, 10Hz-10KHz
Glitch Impulse:	±2.5V Range: 3 nV-Sec max. ±5V Range: 5 nV-Sec ±10V Range: 8 nV-Sec

❑ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Clocking Rate:	Internal Rate Clock: 460 to 400,000 samples per second per channel External Rate Clock: 0 to 400,000 samples per second per channel

DC Accuracy:
(Max error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±2.4mv	±3.3mv
±5V	±1.7mv	±2.2mv
±2.5V	±1.4mv	±1.6mv

Bandwidth, -3dB:	No output filter option: 300 kHz typical 10 kHz filter option: 10 kHz typical (Single-pole lowpass)
Crosstalk Rejection:	80 dB, DC-10 kHz
Common Mode Rejection:	60 dB minimum, DC-1 kHz (return signal ±2V).
Output Voltage Limits:	Signal HI: ±12V relative to output return; Signal LO: ±2V
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

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❑ Operating Modes and Controls

Sample Clock Source:	Internal rate generators, external hardware clock input, or software clock. The external clock output can be used for synchronization of multiple PC104P-16AO2-MF boards. Each output channel can be clocked from an independent internal rate generator, or both channels can be clocked synchronously. Rate generator frequencies are independently adjustable from 16MHz to 32MHz with 0.2 percent resolution and 0.08 percent accuracy, and are derived from the local crystal-controlled master clock. Rate generator outputs are divided by two independent 16-bit counters to provide the output channel clocks. External sync I/O is software-selectable as either TTL-compatible, or as 2-wire LVDS differential pairs. The Sync I/O signals can be operated either as output clocks, or as burst triggers. In addition to the basic rate generator frequencies that are adjustable with 0.2 percent resolution, up to eight custom frequencies can be specified in the 16-32 MHz range as a factory option.
Burst Trigger:	Software control bit, or external sync input.
Update Mode:	Simultaneous or channel-sequential output updating
Active Buffer Size:	From 4 output values to 32K-values in 2:1 steps; both buffers.
Buffer Modes:	Circular (closed) for periodic waveforms, or Open for continuous functions
Data Format:	Software selected as offset binary or as Two's complement

AUTOCALIBRATION

During auto calibration, all analog channels are calibrated to a single precision internal voltage reference that is adjustable with a single trimmer. Auto calibration has a typical duration of 1-2 seconds, and can be invoked at any time after initialization by asserting a single control bit

PCI INTERFACE

❑ Analog Output Buffers

Analog output data is written to the board through two registers that serve as FIFO buffer ports. Each buffer is 17 bits wide, has a software-controlled capacity of from 4 values to 32K output values, and is right justified to the LSB in the D32 PCI data path. Output data is a 16-bit field that is software-configurable in either Two's complement or offset binary format. The 17th bit is used as an end-of-frame (EOF) flag for tracking functions through the buffer.

❑ **Compatibility:** Conforms to PCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers to the output buffers as bus master.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5VDC ±0.2 VDC at 1.5 Amps, maximum

Maximum Power Dissipation: 6.0 Watts, Side 1
1.5 Watts, Side 2

❑ Physical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side 1 is protected by an EMI shield.

❑ Environmental Specifications

Ambient Temperature Range: Operating: 0 to +55 degrees Celsius
Storage: -40 to +85 degrees Celsius

Relative Humidity: Operating: 0 to 80%, non-condensing
Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

Cooling: Conventional convection cooling.

ORDERING INFORMATION

Specify the basic product model number (PC104P-16AO2-MF), followed by an option suffix "-A-B-C" as indicated in the table below. For example, model number PC104P-16AO2-MF-5V-NF-4CF describes a board with a ±5 Volt output range, no output filters, and four custom frequencies.

Optional Parameter	Value	Specify Option As:
Output Range:	±2.5 Volts	A = 2.5V
	±5 Volts	A = 5V
	±10 Volts	A = 10V
Output Lowpass Filter:	No output Filter	B = NF
	10 kHz Output Filter	B = F
Custom Rate-Generator Frequencies: * (8 Maximum)	No custom frequencies	C = NCF
	Custom frequencies	C = (1-8)CF

* Specify required frequencies and accuracies (±0.004-0.100 percent). Contact factory for availability.

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SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

P5A	
PIN	SIGNAL
1	ANA OUTPUT 00 LO
2	ANA OUTPUT 00 HI
3	OUTPUT RETURN
4	OUTPUT RETURN
5	ANA OUTPUT 00 LO
6	ANA OUTPUT 00 HI
7	OUTPUT RETURN
8	OUTPUT RETURN
9	OUTPUT RETURN
10	OUTPUT RETURN
11	DIGITAL RTN
12	TTL SYNC INP
13	DIGITAL RTN
14	DIFF SYNC INP LO
15	DIFF SYNC INP HI
16	DIGITAL RTN
17	DIGITAL RTN

P5B	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT RETURN
3	OUTPUT RETURN
4	OUTPUT RETURN
5	OUTPUT RETURN
6	OUTPUT RETURN
7	VRANGE RETURN
8	VRANGE OUTPUT
9	VRANGE RETURN
10	OUTPUT RETURN
11	DIGITAL RTN
12	TTL SYNC OUT
13	DIGITAL RTN
14	DIFF SYNC OUT LO
15	DIFF SYNC OUT HI
16	DIGITAL RTN
17	DIGITAL RTN

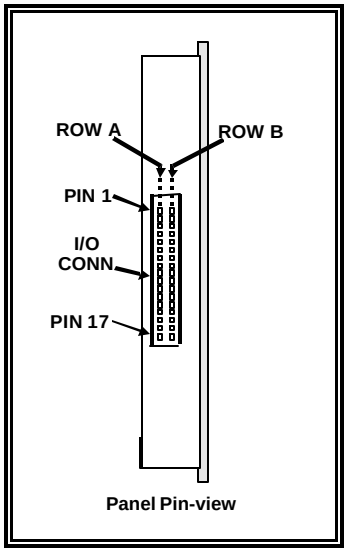

Figure 2. System Input/Output Connector

System Mating Connector:
Rugged 34-pin 0.050" dual-row connector with metal shell:
Robinson Nugent # P50-034-DDS-TG.
Backshell, Straight: # P50-034-STR-BSK.

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