INNOVATION and EXCELLENCE

DTL5A-LC

100 Watt, Serial-Input Electronic Load Low Compliance Version

Features

- Serial-input controlled
- 100 watts maximum load capacity
- 0.6 to 50V, 0 to 2.0A capability
- Parallel load capability for higher current and power applications
- Dynamic loading to 20 kHz
- Compliance Voltage down to 0.6 Volts

Applications

- Power supply test and characterization
- Dynamic power supply burn-in
- Battery capacity testing
- Current source testing
- Capacitor discharge testing
- Power resistor substitution
- Real-time load simulation

DATEL's DTL5A-LC is a serial-input controlled electronic loads featuring a low compliance voltage operation (down to 0.6 Volts)! Similar to DATEL's DTL3A, the DTL5A-LC also offers a loading current range of 0 to 2.0A full scale range with a loading voltage to 50V. The DTL5A-LC's ability to operate down to 0.6 Volts, allows this device to be used with next-generation, low-voltage output power supplies. The DTL3A's compliance voltage operates from 2.5 Volts to 50 Volts, sufficient for today's 2.5V, 3.3V, 5 Volt, etc., power product voltages, with improved gain specifications.

The small but efficient heat transfer package allows up to 100W of power dissipation by using external heatsinking. The devices are packaged in a small 2" x 2" x 0.4" metal package, providing easy mounting capability for external heatsinks. A monitor circuit makes sure a compliance voltage is present, before biasing the DTL5A-LC's output stage. A Fault line goes active, should the device-under-test go below its compliance voltage.

These loads feature fast current step response times, settling a full scale step in 100 µsec to ±1% Full Scale Range (FSR). Dynamic loading is up to 20kHz, and a current resolution of ±0.025% is achieved. Opto-isolators are utilized on the digital input lines, with 500 Volts of isolation provided from the load outputs to input ground. The opto-isolators are internally buffered, making the DTL5A-LC easy to drive, with any digital I/O board. Isolation from any pin to case is 500 Volts.

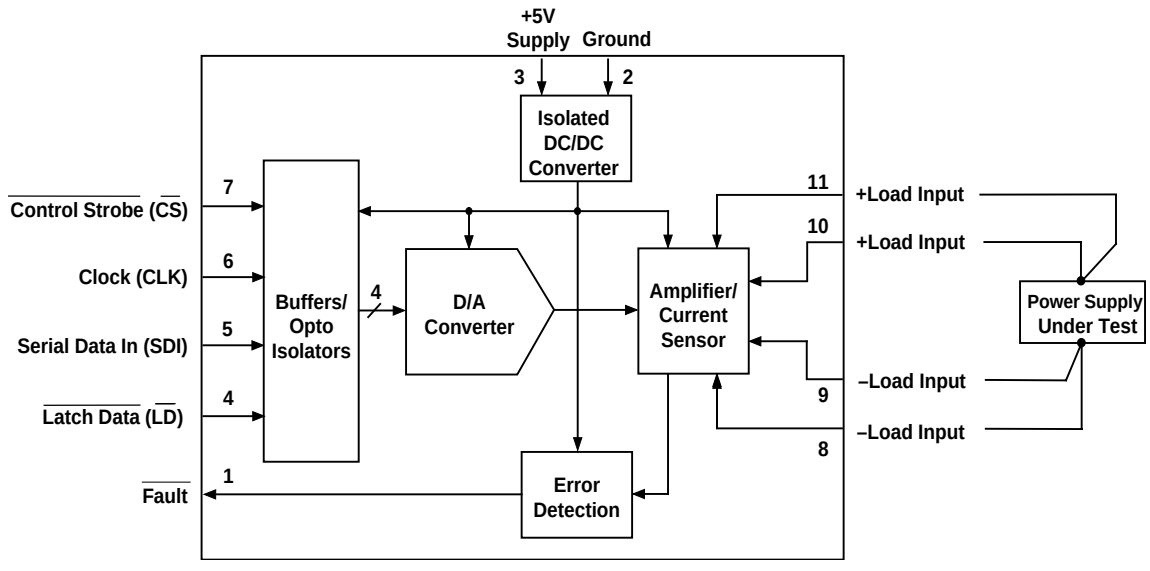


Figure 1. Simplified Schematic

Performance Specifications and Ordering Guide ①

Model	Output							Package (Case Pinout)
	Compliance Voltage (Volts)	Loading Curent (Amperes)	Current Resolution mA	Accuracy (%FSR)	Offset Error (%FSR)	Gain Error (mA)	Gain Error (% of Setting)	
DTL5A-LC	0.6 to 50	0 to 2.0	0.5	±3	±0.05	50	±0.25	C1

① Typical at T_A = +25°C under nominal line voltage and full-load conditions unless otherwise noted.

Part Number Structure

DTL 5 A - LC

Prefix:
DTL = DATEL product

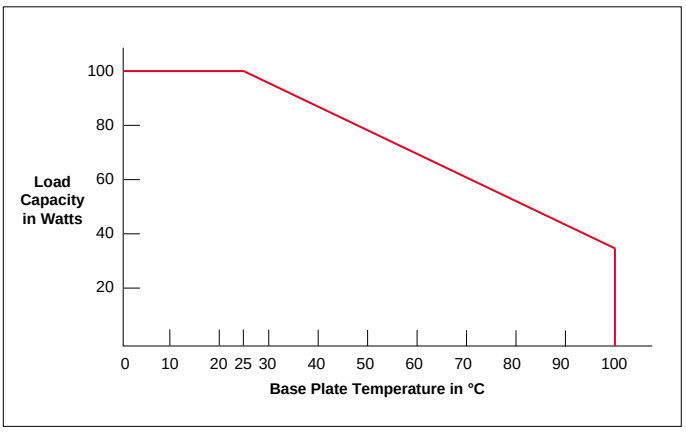
A-Series
High Reliability

Voltage Range/Current:
5 = 2.5 to 50V, 0 to 2A

LC = Low Compliance:
Voltage Range of 0.6 to 50V
DTL5A-LC model only

The warranty period is one year

Temperature Derating

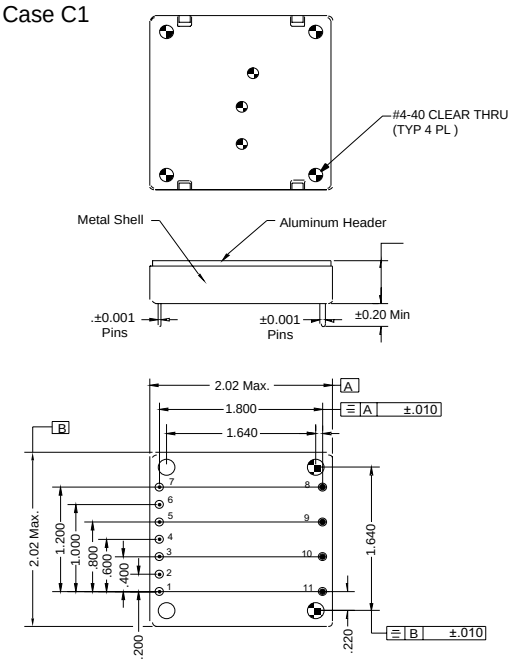


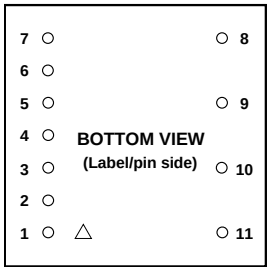
Note:
The DTL5A-LC electronic load packaging has been designed to allow for use with external heatsinking for high wattage applications. The DTL5A-LC can dissipate up to 100 Watts with external cooling (heatsink or fan) observing the base plate temperature requirements above. The loads are capable of dissipating 5 Watts at room temperature without any external cooling.

The devices can also be connected in parallel for additional loading capability.

Mechanical Specifications

Case C1





I/O Connections			
Pin	**Function**	**Pin**	**Function**
1	$\overline{\text{Fault}}$	**8**	- Load Input
2	Ground	**9**	- Load Input
3	+5 Volts Supply	**10**	+ Load Input
4	$\overline{\text{Latch Data}}$ ($\overline{\text{LD}}$)	11	+ Load Input
5	Serial Data In (SDI)		
6	Clock (CLK)		
7	$\overline{\text{Control Strobe}}$ ($\overline{\text{CS}}$)		

Performance/Functional Specifications

Typical @ T_A = +25°C under nominal line voltage and full-load conditions unless noted.

Input	Min.	Typ.	Max.	Units
Digital Inputs (pins 4, 5, 6, 7):				
V_{IL}			0.8	Volts
V_{IH}	2.0			Volts
I_{IL}			-0.6	mA
I_{IH}			20	µA
Output				
Loading Current	See Ordering Guide			
Current Resolution			±0.025	%FSR
Offset Error			±0.05	%FSR
Gain Error DTL5A-LC			±0.3	%FSR
Compliance Voltage Range	See Ordering Guide			
Output Impedance	10			Mohm
Dynamic Characteristics				
Dynamic Loading to:		20		kHz
Settling Time (Full Scale Step)		100		usec
Slew Rate		10		A/µsec
Power				
+5 Volts Supply (pin 3)	+4.75	+5.0	+5.25	Volts
Current (pin 3)		+110	+150	mA
Environmental				
Operating Ambient Temperature Ta, where no de-rating required. Natural Convection, vertical mount				
Storage Temperature	–40		+105	℃
Humidity (Non-condensing)			95	**%**
Altitude Above Sea Level		10,000		feet
Physical				
Dimensions	2" x 2" x 0.52" (51 x 51 x 12.7mm)			
Pin Length	0.2			inches
Shielding	6-sided			
Case Material	Tin-plated Steel Shell Heat-sink side: Aluminum			
Pin Material	Brass, solder coated			
Isolation, ± Load to Input Ground	500			Volts
Isolation, any pin to case	500			Volts
Isolation, resistance	100			Mohm
Mounting	Through-hole spacer, #4-40 clearance			
Weight	1.9 ounces (55 grams)			

Timing	Min.	Typ.	Max.	Units
Refer to timing diagram: CLK			200	kHz
$t_{cl} = t_{ch}$		1		µsec
t_{css}		1		µsec
t_{csh}		1		µsec
t_{ld1}		2		µsec
t_{ld2}		2		µsec
t_{ldw}		2		µsec
t_{ds}		0.5		µsec
t_{dh}		0.5		µsec

Absolute Maximum Ratings

These are stress ratings. Exposure of devices to any of these conditions may adversely affect long-term reliability. Proper operation under conditions other than those listed in the Performance/Functional Specifications Table is not implied.

Power Supply Voltage (pin3):	5.5 Volts
Digital Input Voltage (pins 4,5,6,7):	5.5 Volts
Output Reverse-Polarity Protection:	No protection
Output Overvoltage Protection:	No protection
Storage Temperature	–40 to +105°C
Lead Temperature (soldering, 10 sec.)	+300°C

Overview

The DTL5A-LC is a serial-input controlled current sink. Powered by a single +5V power supply, the DTL5A-LC provides a compliance voltage range from 0.6 Volts to 50 Volts, with loading currents to 2.0 Amperes. Refer to the Table of the basic "Mapping of the Serial-Input Data Word to the Loading Current for the devices transfer function. Utilizing external heatsinking, the device handles loads to 100 watts with a base-plate temperature of 25°C, derating thereafter (only 5 Watts without external heatsink/cooling. Refer to the "Temperature Derating" curve figure herein that illustrates the load capacity in Watts, as a function of the base plate temperature.

The Device Under Test (DUT) outputs are hooked up to the +Load Input (pins 10 & 11) and the - Load Input (pins 8 & 9). An input serial data stream (Pin 5) and clock (Pin 6) are opto-isolated internally. These isolated inputs are gated through to a 12-bit serial input D/A, where the input word can be latched using the *Latch Data* input (Pin 4). A Fault ouput pin (Pin 1) indicates excessive heat or operation outside the compliance range.

Operation Overview

Programming is easily accomplished by utilizing four lines of a parallel digital I/O port. The four digital outputs will be used to control the *Control Strobe* (CS, pin7), the *Latch Data* (LD, pin 4), the *Serial Data In* (SDI, pin 5) and the *Clock* (CLK, pin 6) functions of the DTL5A-LC Series.

Initialization

Initialization of the device is accomplished by first setting the *Control Strobe*, *Clock* and *Latch Data* pins to a Logic High ("1") state. The *Serial Data In* state at this time is "Don't Care". Next, bring the *Control Strobe* pin to a Logic Low ("0") state. The load is now prepared to accept a serial input word.

Input of Serial Data

After initialization, a serial-input data word representing the desired load current is input to the load. This is accomplished with a data stream that begins with the Most Significant Bit (MSB). With the MSB present on the *Serial Data In* (pin 5), toggle the *Clock* (pin 6) through a High-Low-High state sequence. Similarly, proceed from the MSB to the LSB bits, toggling the *Clock* (pin 6) through a High-Low-High state for each bit. The timing specifications shown in the "Timing Diagram" should be observed in transitioning the clock states.

Latching the Data Word

Upon entering the final, Least Significant Bit (LSB), the serial-input data word is latched, by bringing the *Control Strobe* (pin 7) high and then toggling the *Latch Data* (pin 4) through a High-Low-High state sequence.

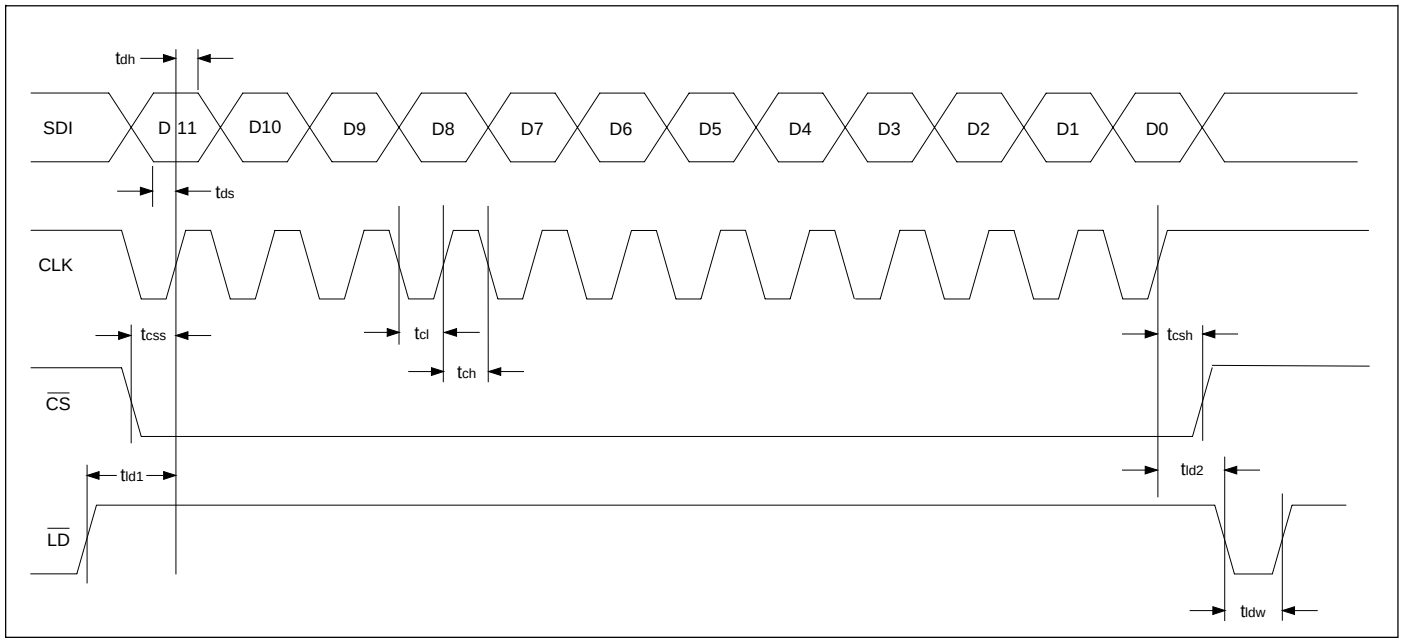
Software: C Language

The following steps describe a typical timing sequence when using four lines of a parallel digital I/O port and a programming language such as C. Using 4 bits of an 8-bit port, assign BIT_0 (LSB) to the *Control Strobe* (CS, pin 7), BIT_1 to *Latch Data* (LD, pin 4), BIT_2 to *Serial Data In* (SDI, pin 5) and BIT_3 to the *Clock* (CLK, pin 6).

1. Initialize with *Latch Data, Clock,* and *Control Strobe* HIGH.
   BIT_0 = 1, BIT_1 = 1, BIT_2 = X (don't care), BIT _3 = 1
2. Place the *Control Strobe* LOW.
   BIT_0 = 0
3. Place D11 (MSB) of the Data Word into *Serial Data* In.
   BIT_2 = 0 or 1
4. Toggle the *Clock* HIGH-LOW-HIGH
   BIT_3 =1-to-0-to-1
5. Place D10 of the Data Word into *Serial Data* In.
   BIT_2 = 0 or 1
6. Toggle the *Clock* High-LOW-HIGH.
   BIT_3 = 1-to-0-to-1
7. REPEAT this process (steps 5 and 6) for the remaining data bits (D9-D0).
8. Set the *Control Strobe* High.
   Bit_0 = 1
9. Toggle the *Latch Data* High-LOW-HIGH
   BIT_1 = 1-to-0-to-1

Serial-Input Data Word			Load Current (Amperes)
MSB		LSB	DTL5A-LC
1111	1111	1111	1.9995
1100	0000	0000	1.5000
1000	0000	0000	1.000
0111	1111	1111	0.9995
0100	0000	0000	0.5000
0010	0000	0000	0.2500
0000	0000	0001	0.0005
0000	000	0000	0.000

Mapping of the Serial-Input Data Word to Load Current



Timing Diagram

Quality and Reliability

The DTL5A-LC is one of the first Electronic Loads to emerge from DATEL's new, company-wide approach to designing and manufacturing the most reliable power products available. The five-pronged program draws our Quality Assurance function into all aspects of new-product design, development, characterization, qualification and manufacturing.

Design for Reliability

Design for Reliability is woven throughout our multi-phased, new-product-development process. Design-for-reliability practices are fully documented and begin early in the new-product development cycle with the following goals:

1. To work from an approved components/vendors list ensuring the use of reliable components and the rigorous qualification of new components.
2. To design with safety margins by adhering to a strict set of derating guidelines and performing theoretical worst-case analyses.
3. To locate potential design weaknesses early in the product-development cycle by using extensive HALT (Highly Accelerated Life Testing).
4. To prove that early design improvements are effective by employing a thorough FRACA (Failure Reporting Analysis and Corrective Action) system.

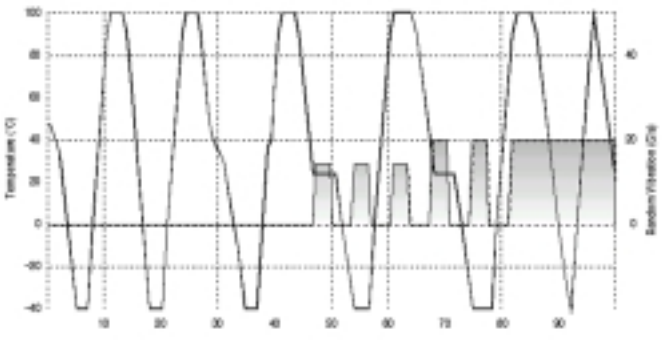
HALT Testing

The goal of the accelerated-stress techniques used by DATEL is to force device maturity, in a short period of time, by exposing devices to excessive levels of "every stimulus of potential value." We use HALT (Highly Accelerated Life Testing) repeatedly during the design and early manufacturing phases to detect potential electrical and mechanical design weaknesses that could result in possible future field failures.

During HALT, prototype and pre-production electronic loads are subjected to progressively higher stress levels induced by thermal cycling, rate of temperature change, vibration, power cycling, product-specific stresses (such as dc voltage variation) and combined environments. The stresses are not meant to simulate field environments but to expose any weaknesses in a product's electro/mechanical design and/or assembly processes. The goal of HALT is to make products fail so that device weaknesses can be analyzed and strengthened as appropriate. Applied stresses are continually stepped up until products eventually fail. After corrective actions and/or design changes, stresses are stepped up again and the cycle is repeated until the "fundamental limit of the technology" is determined.

DATEL has invested in a Qualmark OVS-1 HALT tester capable of applying voltage and temperature extremes as well as 6-axis, linear and rotational, random vibration. A typical HALT profile (shown above) consists of thermal cycling (–55 to +125°C, 30°C/minute) and simultaneous, gradually increasing, random longitudinal and rotational vibration up to 20G's with load cycling and applied-voltage extremes added as desired. Many devices in DATEL's new A-Series could not be made to fail prior to reaching either the limits of the HALT chamber or some previously known physical limit of the device. We also use the HALT chamber and its ability to rapidly cool devices to verify their "cold-start" capabilities.

Typical HALT Profile



Test Time (minutes)

Qualification

For each new product, electrical performance is verified via a comprehensive characterization process and long-term reliability is confirmed via a rigorous qualification procedure. The qual procedure includes such strenuous tests as thermal shock and 500 hour life. Qual testing is summarized below.

Qualification Testing

Qualification Test	Method/Comments
HALT	DATEL in-house procedure
High Temperature Storage	Max. rated temp., 1,000 hours
Thermal Shock	10 cycles, –55 to +125°C
Temperature/Humidity	+85°C, 85% humidity, 48 hours
Lead Integrity	DATEL in-house procedure
Life Test	+70°C, 500 hours*
Marking Permanency	DATEL in-house procedure
End Point Electrical Tests	Per product specification

* Interim electrical test at 200 hours.

In-Line Process Controls and Screening

A combination of statistical sampling and 100% inspection techniques keeps our assembly line under constant control. Parameters such as solder-paste thickness, component placement, cleanliness, etc. are statistically sampled, charted and fine tuned as necessary. Visual inspections are performed by trained operators after pick-and-place, soldering and cleaning operations. Units are 100% electrically tested prior to potting. All devices are temperature cycled, burned-in, hi-pot tested and final-electrical tested prior to external visual examination, packing and shipping.

Rapid Response to Problems

DATEL employs an outstanding corrective-action system to immediately address any detected shortcomings in either products or processes. Whenever our assembly, quality or engineering personnel spot a product/process problem, or if a product is returned with a potential defect, we immediately perform a detailed failure analysis and, if necessary, undertake corrective actions. Over time, this system has helped refine our assembly operation to yield one of the lowest product defect rates in the industry.

DATEL® INNOVATION and EXCELLENCE

ISO 9001

DS-DTL005 Rev_A 1/2000

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1151
Tel: (508) 339-3000 (800) 233-2765 Fax: (508) 339-6356
Internet: www.datel.com Email: sales@datel.com
Data Sheet Fax Back: (508) 261-2857

DATEL (UK) LTD. Tadley, England Tel: (01256)-880444
DATEL S.A.R.L. Montigny Le Bretonneux, France Tel: 01-34-60-01-01
DATEL GmbH München, Germany Tel: 89-544334-0
DATEL KK Tokyo, Japan Tel: 3-3779-1031, Osaka Tel: 6-354-2025