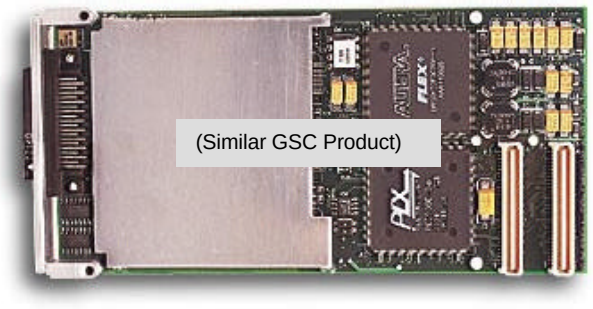
General Standards Corporation

High Performance Bus Interface Solutions

PMC-16HSDI

16-Bit, Six-Channel Sigma-Delta Analog Input PMC Board

With 1.1 MSPS Sample Rate per Channel, and Two Independent Clocks



PRELIMINARY

Features Include:

- Sigma-Delta Conversion; No External Antialiasing Filters Required
- High Effective Sampling Rate; 16-32 Times the Effective Rate of Successive Approximation Converters Operating at the Same Conversion Rate
- Integral Antialiasing Input Filters Reject Out-of-Band Interference Components
- Software-Selectable Ranges: ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
- Six 16-Bit Analog Input Channels; Dedicated Sigma-Delta Converter per Channel
- Sample Rates Adjustable up to 1,100 K-Samples per Second per Channel
- Two Independent Sample-Rate Generators; Adjustable with 0.2 Percent Resolution
- Low Noise; Typically Less than 0.4mVRMS RTI
- 64K-Sample FIFO Buffer. All Data is Channel-Tagged.
- Harmonic Sampling Supported, with Clocking Ratios Between Channels from 1 to 20
- Auto calibration Uses Hardware Correction; No missing Codes Introduced
- Integral Shield Assures Minimum Susceptibility to Radiated Noise in PMC Environments
- Single-width PMC Form Factor
- VxWorks™ and WinNT™ Drivers are available

Applications Include:

- ✓ Acoustics Analysis
- ✓ Analog Inputs
- ✓ Data Acquisition Systems
- ✓ Voltage Measurement
- ✓ Process Monitoring
- ✓ Industrial Robotics
- ✓ Automatic Test Equipment
- ✓ Audio Waveform Analysis
- ✓ Environmental Test Systems

REV 091701

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256)880-8787 or (800)653-9970
FAX: (256)880-8788
Email: sales@generalstandards.com

Overview:

The 6-channel PMC-16HSDI analog input board provides high-density precision 16-bit analog input resources in a single-width PMC form factor. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from precision voltage measurements, to the analysis of complex audio signals and waveforms. Each of the six sigma-delta analog input channels can be controlled by either of two independent sample clocks, and multiple channels can be harmonically locked together. Sample rates are adjustable from 30 KSPS to 1.1 MSPS, and the input range is software selectable as ±1.25V, ±2.5V, ±5V or ±10V. Internal auto calibration networks permit periodic calibration to be performed without removing the board from the system.

Functional Description:

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1). Each of the six input channels contains an input buffer, an adaptive digital-image filter, and a dedicated sigma-delta A/D converter (ADC). The inputs can be configured for either differential or single-ended operation, or an internal voltage reference can be applied to all channels to support selftest operations and auto calibration. Gain and offset trimming of the input channels is performed by calibration DAC's that are loaded with channel correction values during auto calibration. The use of calibration DAC's eliminates the missing codes that occur when analog input channels are calibrated exclusively in the digital domain.

Each ADC contains a digital antialiasing filter that rejects out-of-band signals above approximately 48 percent of the selected sample rate. Conversion data from all active channels is transferred to the PCI bus through a 64K-sample data buffer that has a software-controlled threshold for generating interrupt requests. Multiple channels can be synchronized to perform synchronous sampling, either by a software command, or by external hardware sync and clock input signals.

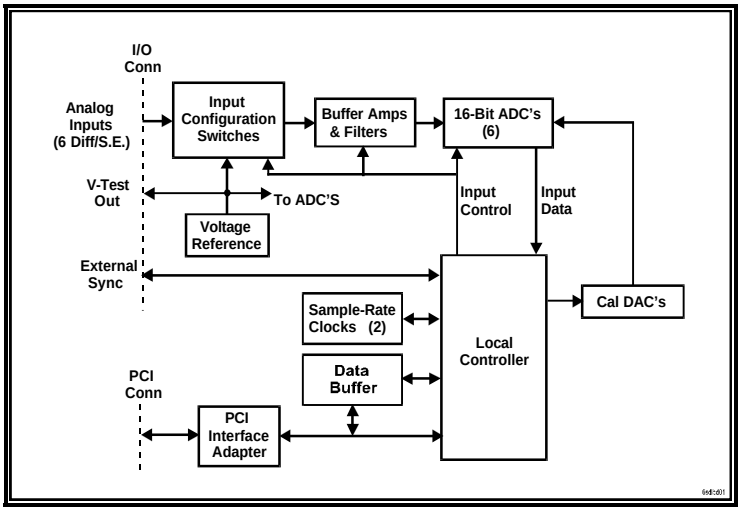


Figure 1. PMC-16HSDI; Functional Organization

The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and supports the "plug-n-play" initialization concept. System input/output connections are made at the front panel through a high-density metal-shrouded 50-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages.

❑ Input Channel Characteristics:

Configuration:	6 input channels, software controlled as differential or single-ended. Optional 2-channel and 4-channel configurations available.
Voltage Range:	Software Configurable as ±1.25 Volts, ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2 Megohms line-line.
Common Mode Rejection:	80 dB, DC-60 Hz (Differential mode)
Common Mode Range:	±10 Volts with zero normal-mode input
Offset Voltage:	±0.6 millivolts, maximum
Input Noise:	0.4mVRMS, typical.
Overvoltage Protection:	±30-Volt transient with power applied; ±15 Volts with power removed

❑ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	30,000 to 1,100,000 samples per second per channel
Oversampling Factor:	DC-500KSPS: x32, 500KSPS-1100KSPS: x16.

DC Accuracy:
(Maximum composite error)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±1.2mV	±5.2mV
±5V	±1.1mV	±3.1mV
±2.5V	±0.9mV	±2.2mV
±1.25V	±0.8mV	±1.5mV

Small Signal Bandwidth:	DC to approximately 48 percent of the selected sample rate
Power Bandwidth:	DC to 2*10^{6} Hz-Vpp minimum. Accepts 100kHz input at 20 VPP.
Crosstalk Rejection:	84 dB typical, DC-10 kHz; 70dB DC-400kHz.
Antialias Filtering:	Each ADC provides internal digital antialias filtering at approximately 48 percent of the selected sample rate. This digital filter is supported by a multi-pole analog filter that rejects interference at the harmonic images of the digital filter. The cutoff frequency of the analog filter in each channel is optimized automatically in response to the selected sample rate.
Integral Nonlinearity:	±0.003 percent of FSR, typical
Differential Nonlinearity:	±0.0015 percent of FSR, maximum
Total Harmonic Distortion:	84 dB typical, from DC to 40 percent of sample rate

❑ Operating Modes and Controls

Organization:	Two 3-channel analog input groups, and two sample rate generators. Each channel group can operate from either rate generator. The sample rate for each individual channel is selected by dividing the frequency of the assigned rate generator by any integer from 1 through 20.
Sample Rate Generators:	Either of two independent internal rate generators can be assigned to any input channel group. Each generator is adjustable from 19.2 MHz to 38.4 MHz, and provides sample rates from 600 KSPS to 1200 KSPS after division by 32 (x16 oversampling), or from 300 KSPS to 600 KSPS after division by 64 (x32 oversampling). Subsequent division by an integer from 1 to 20 for each channel provides sample rates from 15 KSPS to 1200 KSPS. (Specified performance is guaranteed only within the range from 30 KSPS to 1100 KSPS). Settling time when changing frequencies is approximately 20 ms, and settling completion is selectable as an interrupt event. Setting resolution is 0.2 percent or less; accuracy is ±0.08 percent.
External Clock I/O:	An LVDS hardware output clock can be derived either from a 16-32 MHz LVDS external hardware input clock or from an internal rate generator. The external clock input can be selected as the rate generator for any or all channels. . Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. This requires a split I/O cable. As many as six boards can be daisy-chained together.
Synchronization:	Sampling can be synchronized within each channel group through software, or each group can be synchronized to an external LVDS hardware sync input. By using the daisy-chain configuration described for External Clock I/O, hardware sync inputs and outputs can be used to synchronize the sampling among multiple boards.
Harmonic Sampling:	Harmonic sampling ratios are implemented by adjusting the sample rates of channels within a group to specific fractions of the assigned rate generator frequency. (See Sample Rate Generators).
Data Format:	Software selected as either offset binary or two's complement
Channel Tags:	Each input data value is appended with a 3-bit channel identification tag.
Buffer Size Register:	Contains the total number of samples present in the input data buffer.
Buffer Threshold Flags:	A threshold flag is asserted when the number of samples in the input data buffer equals or exceeds the selected threshold. The buffer threshold can be any integer from 0000 to FFFEh.

PCI INTERFACE

❑ Compatibility:

Conforms to PCI Specification 2.2, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides a single multifunction interrupt.
Supports FIFO DMA transfers as bus master.

❑ Board Control and Data Registers (D32 Access)

Board Control/Status Register:	Determines the principal operating mode.
Rate Generator Registers:	Select rate generator frequencies.
Channel Control Registers:	Control the clock sources and sample rates for all input channels.
Input Data Buffer:	64K by 19-Bit FIFO buffer.
Buffer Threshold:	Selects the input data buffer threshold.
Interrupt Control:	Interrupt source control and status.

❑ Analog Input Buffer

Analog input data is read through a 64K-sample FIFO buffer as a 19-Bit data field for each input sample. The data field contains a 16-Bit conversion value and a 2-Bit channel tag. A threshold flag occurs when the associated buffer contains a number of data samples that exceeds a software-selected threshold from 0000h to FFFEh, and can be used to generate empty and full flags.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5VDC ±0.2 VDC at 1.5 Amps maximum

Power Dissipation:	6.0 Watts,	Side 1
	1.5 Watts,	Side 2

❑ Physical Characteristics

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side 1 is protected by an EMI shield.

❑ Environmental Specifications

Ambient Temperature Range:	Operating:	0 to +55 degrees Celsius
	Storage:	-40 to +85 degrees Celsius
Relative Humidity:	Operating:	0 to 80%, non-condensing
	Storage:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.	

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❑ Cooling Requirements

Conventional air cooling; 200 LPFM (typical mezzanine environment).

ORDERING INFORMATION

Specify the basic product model number (PMC-16HSDI), followed by an option suffix "-A", as indicated below. For example, model number PMC-16HSDI-6 describes a board with 6 input channels.

Optional Parameter	Value	Specify Option As:
Number of Input Channels:	2 Channels	A = 2
	4 Channels	A = 4
	6 Channels	A = 6

SYSTEM I/O CONNECTIONS

Table 1. System Connector Pin Functions

PIN	SIGNAL	PIN	SIGNAL
A1	INPUT CHAN 05 LO	B1	CLOCK INPUT LO
A2	INPUT CHAN 05 HI	B2	CLOCK INPUT HI
A3	INPUT RETURN	B3	DIGITAL RETURN
A4	INPUT RETURN	B4	DIGITAL RETURN
A5	INPUT CHAN 04 LO	B5	CLOCK OUTPUT LO
A6	INPUT CHAN 04 HI	B6	CLOCK OUTPUT HI
A7	INPUT RETURN	B7	DIGITAL RETURN
A8	INPUT RETURN	B8	DIGITAL RETURN
A9	INPUT CHAN 03 LO	B9	SYNC INPUT LO
A10	INPUT CHAN 03 HI	B10	SYNC INPUT HI
A11	INPUT RETURN	B11	DIGITAL RETURN
A12	INPUT RETURN	B12	DIGITAL RETURN
A13	INPUT CHAN 02 LO	B13	SYNC OUTPUT LO
A14	INPUT CHAN 02 HI	B14	SYNC OUTPUT HI
A15	INPUT RETURN	B15	DIGITAL RETURN
A16	INPUT RETURN	B16	DIGITAL RETURN
A17	INPUT CHAN 01 LO	B17	DIGITAL RETURN
A18	INPUT CHAN 01 HI	B18	DIGITAL RETURN
A19	INPUT RETURN	B19	DIGITAL RETURN
A20	INPUT RETURN	B20	INPUT RETURN
A21	INPUT CHAN 00 LO	B21	INPUT RETURN
A22	INPUT CHAN 00 HI	B22	INPUT RETURN
A23	INPUT RETURN	B23	VTEST RETURN
A24	INPUT RETURN	B24	VTEST
A25	INPUT RETURN	B25	INPUT RETURN

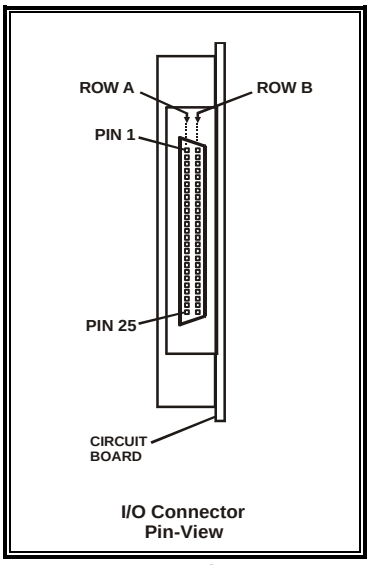

Figure 2. System Input/Output Connector

System Mating Connector:

Rugged 50-pin 0.050" dual-row connector with metal shell. Board connector mates with dual-cable connector type:

AMP #750913-5 or equivalent.

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