

AK58256AG / AK58256AS 262,144 x 8 bit CMOS Dynamic Random Access Memory

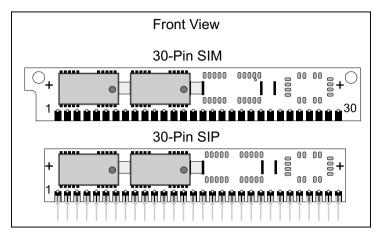
DESCRIPTION

The Accutek AK58256AG/AS high density memory module is a random access memory organized in 256K x 8 bit words. The assembly consists of two 256K x 4 DRAMs in surface mount packages mounted to the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. This packaging approach provides a better than 6 to 1 density increase over standard DIP packaging.

The operation of the AK58256 is identical to two 256K x 4 DRAMs. The data input/output is brought out separately for each 256K x 4 device, with common RAS, CAS and WE control. The \overline{OE} pins are tied to Vss which dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable (\overline{WE}) signal must always go low before \overline{CAS} in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

FEATURES

- 262,144 x 8 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- · JEDEC standard pinout
- Common CAS, RAS and WE control for eight DQ lines
- Separate CAS control for one separate pair of D and Q lines
- 1024 refresh cycles/16ms, A₀ to A₈



- Power:
 - .99 Watt Max Active (60 nS)
 - .88 Watt Max Active (70 nS)
- .77 Watt Max Active (80 nS)
- .65 Watt Max Active (100 nS) 11 mWatt standby (max)
- Operating free air temperature: 00 to 700 C
- Upward compatible with AK581024, AK584096 and AK5816384

FUNCTIONAL DIAGRAM

- · Functionally and Pin compatible with AK48256
- · Available with access times of 60 to 100 nS

PIN NOMENCLATURE

PIN ASSIGNMENT

SYMBOL	PIN#	SYMBOL
Vcc	16	DQ5
CAS	17	A8
DQ1	18	NC

DQ ₁ - DQ ₈	Data In / Data Out
A ₀ - A ₈	Address Inputs
CAS	Column Address Strobe
RAS	Row Address Strobe
WE	Write Enable
Vcc	5v Supply
Vss	Ground
NC	No Connect

MODULE OPTIONS

Leadless SIM	1: AK58256AS
Leaded SIP:	AK58256AG

1	Vcc	16	DQ5
2	CAS	17	A8
3	DQ1	18	NC
4	A0	19	NC
5	A1	20	DQ6
6	DQ2	21	WE
7	A2	22	Vss
8	А3	23	DQ7
9	Vss	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	RAS
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	Vcc

A0 - A8 + RAS + RA	A0 - A8 RAS CAS WE DQ1 DQ2 DQ3 DQ4	ŌE 🌣
DQ5 + DQ6 + DQ7 + DQ8 +	A0 - A8 RAS CAS WE DQ1 DQ2 DQ3 DQ4	ŌĒ Þ

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8

1 Product

AK = Accutek Memory

- 2 Type
 - 4 = Dynamic RAM
 - 5 = CMOS Dynamic RAM
 - 6 = Static RAM

3 Organization/Word Width

- 1 = by 1 16 = by 16
- 4 = by 4 32 = by 32
- $8 = by 8 \quad 36 = by 36$
- 9 = by 9
- 4 Size/Bits Depth
 - 64 = 64K 4096 = 4 MEG 256 = 256K 8192 = 8 MEG 1024 = 1 MEG 16384 = 16 MEG
- 5 Package Type
 - G = Single In-Line Package (SIP)
 - S = Single In-Line Module (SIM)
 - D = Dual In-Line Package (DIP)
 - W = .050 inch Pitch Edge Connect
 - Z = Zig-Zag In-Line Package (ZIP)
- 6 Special Designation
 - P = Page Mode
 - N = Nibble Mode
 - K = Static Column Mode
 - W = Write Per Bit Mode
 - V = Video Ram

7 Separator

- = Commercial 0° C to + 70° C
- M = Military Equivalent Screened
 - (-55⁰C to +125⁰C)
- I = Industrial Temperature Tested
- (-45⁰C to +85⁰C)
- X = Burned In

 $15 = 150 \, \text{nS}$

8 Speed (first two significant digits)

DRAMS			SRAMS		
60	=	60 nS	8	= 8 nS	
70	=	70 nS	12	= 12 nS	
80	=	80 nS	15	= 15 nS	
10	=	100 nS	20	= 20 nS	
12	=	120 nS	70	= 70 nS	

The numbers and coding on this page do not include all variations available, but are shown as examples of the most widely used variations. Contact Accutek if other information is required.

 $85 = 85 \, \text{nS}$



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EXAMPLES:

AK58256ASP-60

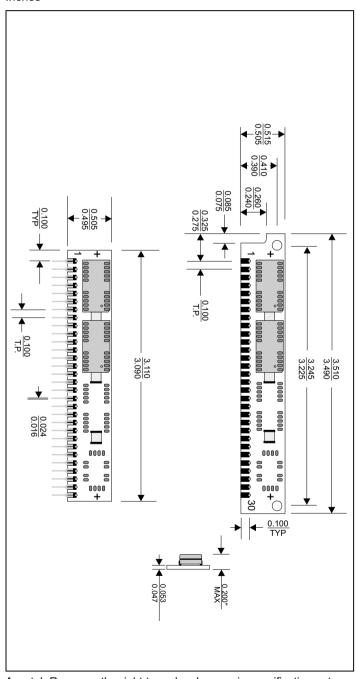
256K x 8, Dynamic RAM, Leadless SIM, Page Mode, Commercial, 60 nSEC Access Time

AK58256AGK-70

256K x 8, Dynamic RAM, Leaded SIP, Static Column Mode Commercial, 70 nSEC AccessTime

MECHANICAL DIMENSIONS

Inches



Accutek Reserves the right to make changes in specifications at any time and without notice. Accutek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.