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VL-FS-MDLS40466D-07 REV. A

(MDLS40466D-LV-LED04 YG)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

ITEM NO.: MDLS40466D-07

APPROVALS: EFFECTIVE DATE

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VARITRONIX LIMITED

Specification
of
LCD Module Type
Item No.: MDLS40466D-07

1. General Description

- 40 characters(5 x 8 dots)x 2 lines STN Positive Yellow Transflective Dot Matrix LCD module.
- Viewing Angle: 6 O'clock direction.
- Driving duty: 1/16 Duty, 1/5 bias.
- 'SAMSUNG' KS0066UP-10BCC(die form) LCD Controller & Driver or equivalent.
- 'SAMSUNG' KS0065B-PCC (die form) or equivalent 40-Channel Segment/Common Drivers for Dot Matrix LCD.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	196.0(W) x 56.0(H) x 14.0 MAX.(D)	mm
Effective viewing area	154.4(W) x 27.6(H)	mm
Display format	40 characters x 4 lines	-
Character size	3.15(W) x 5.50(H) (5 x 8 dots)	mm
Character spacing	0.60(W) x 0.40(H)	mm
Character pitch	3.75(W) x 5.90(H)	mm
Dot size	0.55(W) x 0.60(H)	mm
Dot spacing	0.10(W) x 0.10(H)	mm
Dot pitch	0.65(W) x 0.70(H)	mm
Weight	TBD	grams

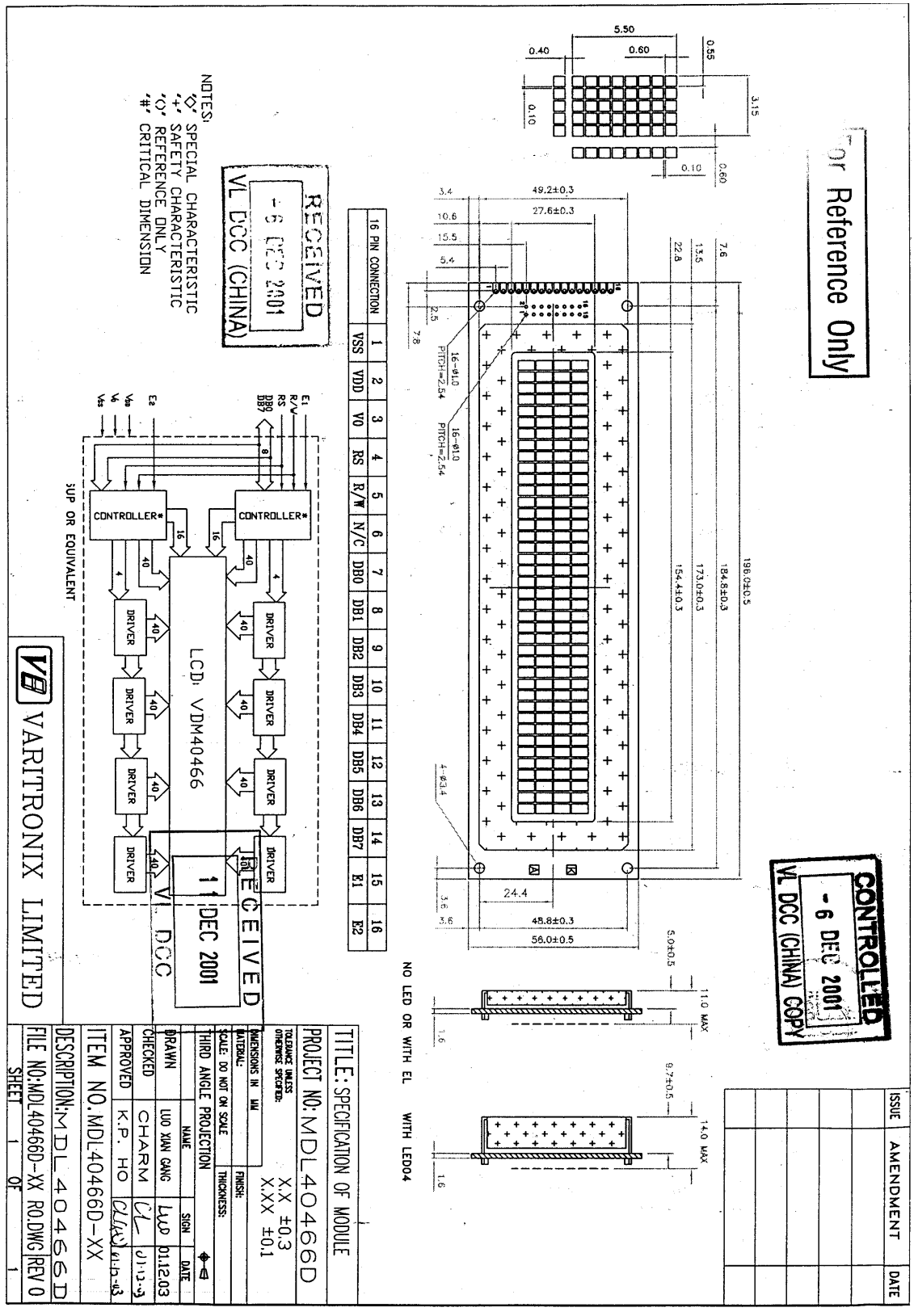

Figure 1: Outline Drawing

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	VSS	Ground(0V).
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	RS	Register Select Input: “High” for Data register (for read and write) ”Low” for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: ” High” for Read mode. “Low” for Write mode.
6	NC	No connection.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	E1	Enable 1. Start signal for data read /write.
16	E2	Enable 2. Start signal for data read /write.
A	LED(+)	Anode of LED backlight
K	LED(-)	Cathode of LED backlight

4.2 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.00	5.25	V
Supply voltage (LCD) (External input)	VLCD =VDD-V0	VDD =5.0V, Note1.	4.2	4.6	5.0	V
Input signal voltage 1 for E,DB0-DB7,R/W,RS.	V_{IH1}	”H” level	2.2	-	VCC	V
	V_{IL1}	” L” level	-0.3	-	0.6	V
Input signal voltage 2 for OSC1.	V_{IH2}	” H” level	VCC –1	-	VCC	V
	V_{IL2}	” L” level	-0.2	-	1.0	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	2.0	3.0	mA
		Checker board mode, Note 1	-	2.2	3.3	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	0.4	0.6	mA
		Checker board mode, Note 1	-	0.4	0.6	mA
Supply Voltage of yellow-green LED04 Backlight	V_{LED04}	Supply Current =360mA No. of LED chips = 72	3.9	4.1	4.3	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

4.3 Timing Specifications

At Ta = 0 °C To +50 °C , VDD = +5V±5%, VSS = 0V.

Refer to Fig. 2, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	tc	500	-	ns
E Rise/Fall Time	t_R,t_F	-	20	ns
E Pulse Width(high, low)	t_W	230	-	ns
R/W and RS Setup Time	t_{SU1}	40	-	ns
R/W and RS Hold Time	t_{H1}	10	-	ns
Data Set-up Time	t_{SU2}	80	-	ns
Data Hold Time	t_{H2}	10	-	ns

Refer to Fig. 3, the bus timing diagram for read mode.

Table 7

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	tc	500	-	ns
E Rise/Fall Time	t_R,t_F	-	20	ns
E Pulse Width(high, low)	t_W	230	-	ns
R/W and RS Setup Time	t_{SU}	40	-	ns
R/W and RS Hold Time	t_H	10	-	ns
Data Output Delay Time	t_D	-	120	ns
Data Hold Time	t_{DH}	5	-	ns

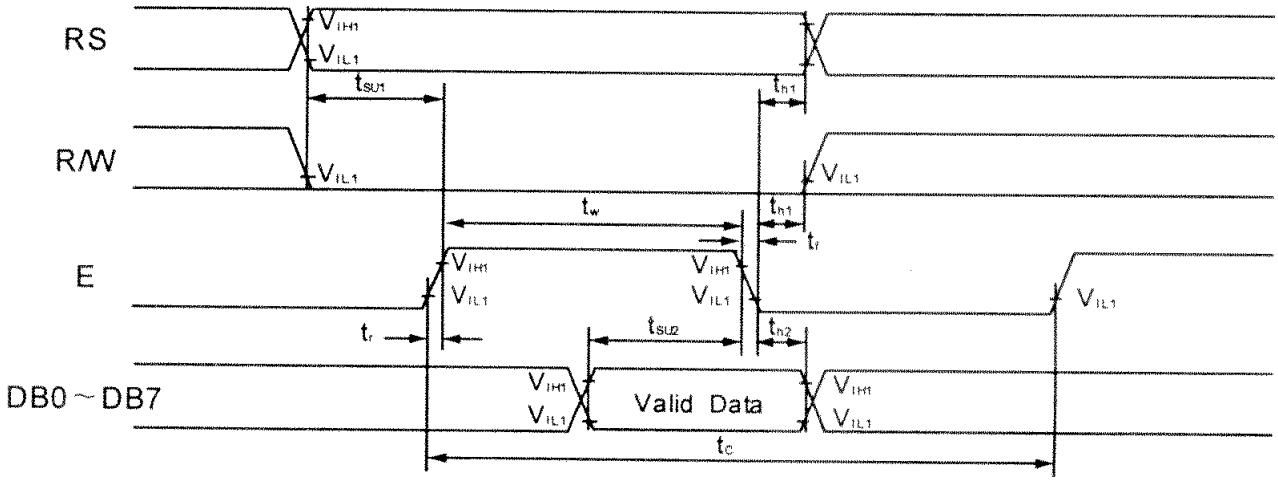

Figure 2: Write Mode Timing Diagram

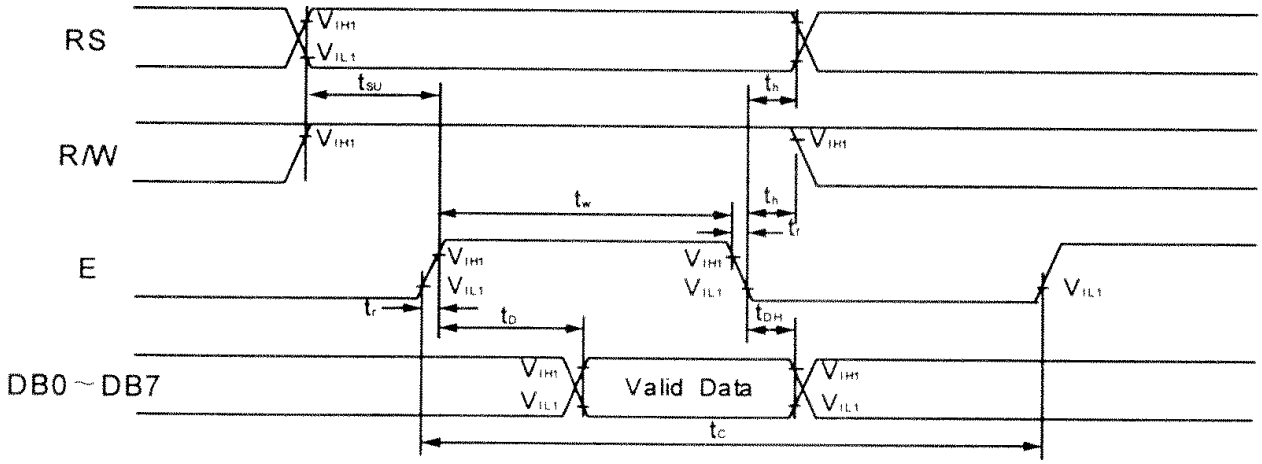

Figure 3: Read Mode Timing Diagram

4.4 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

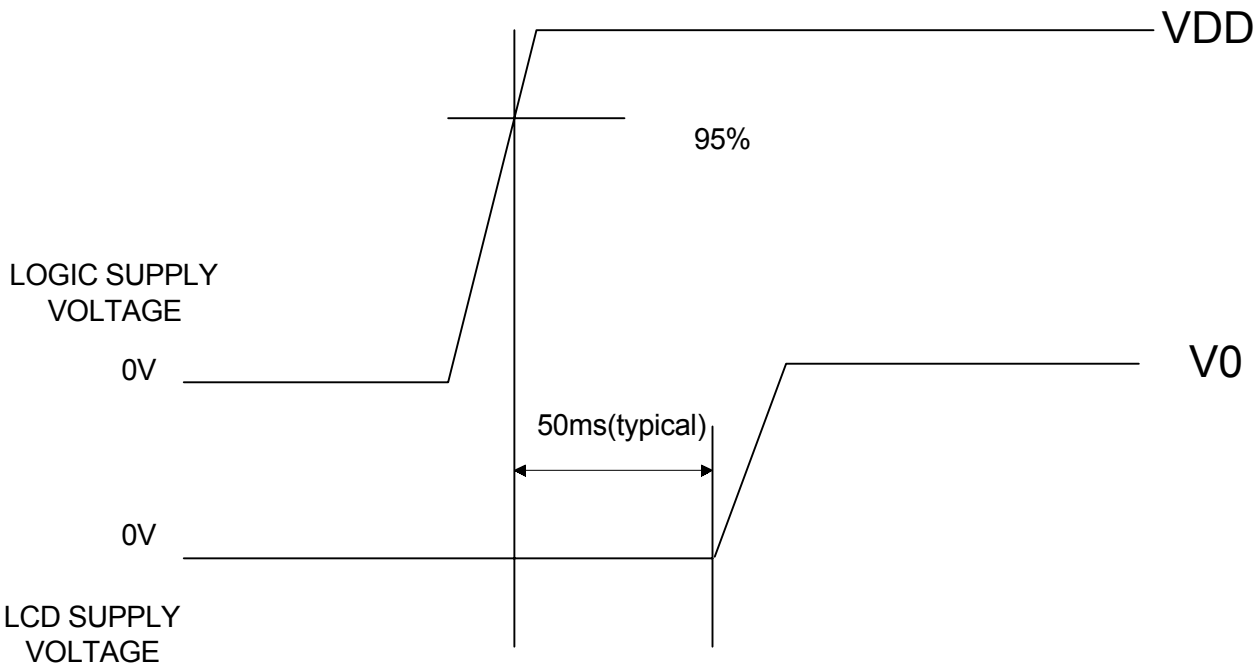

Figure 4: Timing diagram of VDD against V0.

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