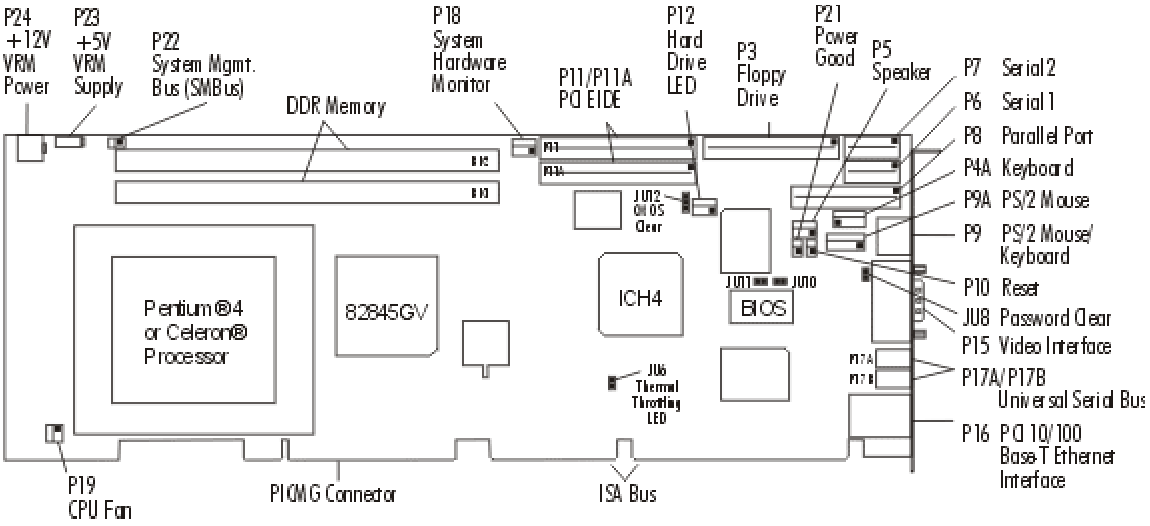
TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales (800) 875-6031 • Phone (770) 287-3100 • Fax (770) 287-3150

Technical Information – Jumpers, Connectors and Memory
T4G (6130-xxx) System Host Board

Layout Diagram



Jumpers & LEDs

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "TOP" is toward the memory sockets; “BOTTOM” is toward the edge fingers.

JU6 Thermal Throttling LED

If the processor core gets to a critical temperature, it slows itself down to half its normal speed. This jumper sets the way in which the LED displays in response to this self-limiting mode.

NOTE: Critical temperature is determined by the processor and cannot be altered by the end user.

Install for real-time activity. The LED lights only when the processor is operating in slow-power mode.*
Remove for latched activity. The LED lights and stays on once the processor has gone into slow- power mode.

JU8 Password Clear

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU9 SCSI Termination

This jumper may be used to enable or disable on-board active termination for the Ultra160 SCSI interface.

Install on the TOP to enable active termination *
Install on the BOTTOM to allow the AIC-7892 to control termination.
Remove to disable active termination.

JU10/11 System Flash ROM Operational Modes

The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales (800) 875-6031 • Phone (770) 287-3100 • Fax (770) 287-3150

	JU10	JU11
All Blocks Write Enabled	Remove *	Remove *
Boot Block Write Protected	Install	Remove
Block 2-16 Write Protected	Remove	Install

JU12 CMOS Clear

Install on the TOP to operate. *
Install on the BOTTOM to clear.

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. CMOS is cleared during the POST routines. Wait for AMIBIOS to display a "CMOS Settings Wrong" message; then power down the system again and remove the jumper before the next power-up.

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales (800) 875-6031 • Phone (770) 287-3100 • Fax (770) 287-3150

Connectors

NOTE:
Pin 1 on the connectors is indicated by the square pad on the PCB.

P3 - FLOPPY DRIVE CONNECTOR

34 pin dual row header, Amp #103308-7

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

P4A - KEYBOARD HEADER

5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

P11A - Secondary IDE Hard Drive Connector

40 pin dual row header, 3M #30340-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 1	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDS
29	DACK 1	30	Gnd
31	IRQ 15	32	NC
33	Add 1	34	SCBL DET*
35	Add 0	36	Add 2
37	CS 1S	38	CS 3S
39	IDEACTS	40	Gnd

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other Drives are detected, pin definition is Gnd.

P12 - HARD DRIVE LED CONNECTOR

4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	LED +
2	LED -
3	LED -
4	LED +

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales (800) 875-6031 • Phone (770) 287-3100 • Fax (770) 287-3150

Connectors (Continued)

P5 - SPEAKER PORT CONNECTOR
4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	Speaker Data
2	Key
3	Gnd
4	+5V

P6 - SERIAL PORT 1 CONNECTOR
10 pin dual row header, Amp #103308-1

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-0	6	Clear to Send-I
7	Data Terminal Ready-0	8	Ring Indicator-I
9	Signal Gnd	10	NC

P7 - SERIAL PORT 2 CONNECTOR
10 pin dual row header, Amp #103308-1

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-0	6	Clear to Send-I
7	Data Terminal Ready-0	8	Ring Indicator-I
9	Signal Gnd	10	NC

P8 - PARALLEL PORT CONNECTOR
26 pin dual row header, Amp #103308-6

PIN	SIGNAL	PIN	SIGNAL
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd

P15 - VIDEO INTERFACE CONNECTOR
15 pin HD15 connector, Amp #1-1470250-3

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	Red	6	Gnd	11	NC
2	Green	7	Gnd	12	EEDI
3	Blue	8	Gnd	13	HSYNC
4	NC	9	+5V	14	VSYNC
5	Gnd	10	Gnd	15	EECS

P16 - 10/100BASE-T ETHERNET CONNECTOR
8 pin shielded RJ-45 connector, Pulse #J0035D21B

PIN	SIGNAL	PIN	SIGNAL
1	TD+	5	NC
2	TD-	6	RX-
3	RX+	7	NC
4	NC	8	NC

P17A - UNIVERSAL SERIAL BUS (USB) CONNECTOR
4 USB vertical connector, Molex #67329-0000
(+5V over current protection)

PIN	SIGNAL
1	+5V - USB0
2	USB0-
3	USB0+
4	Gnd - USB0

P17B - UNIVERSAL SERIAL BUS (USB) CONNECTOR
4 USB vertical connector, Molex #67329-0000
(+5V over current protection)

PIN	SIGNAL
1	+5V - USB1
2	USB1-
3	USB1+
4	Gnd - USB1

11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

Connectors (Continued)

P9 - PS/2 MOUSE AND KEYBOARD CONNECTOR

6 pin mini DIN, Kycon #KMDG-6S-B4T

PIN	SIGNAL
1	Ms Data
2	Kbd Data
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P9A - PS/2 MOUSE HEADER

6 pin single row header, Amp #640456-6

PIN	SIGNAL
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P10 - External Reset Connector

2 pin single row header, Amp #640456-2

PIN	SIGNAL
1	External Reset In (Low Active)
2	Gnd

P18 - SYSTEM HARDWARE MONITOR CONNECTOR

4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	Gnd
2	GPO (General Purpose Output)
3	CI (Chassis Intrusion Input)
4	OVT (Over Temperature)

P19 - CPU FAN

3 pin single row header, Molex #22-23-2031

PIN	SIGNAL
1	Gnd
2	+12V
3	Fan Tach

P21 - POWER GOOD LED

2 pin single row header, Amp #640456-2

PIN	SIGNAL
1	LED -
2	LED +

P22 - SYSTEM MANAGEMENT BUS CONNECTOR

2 pin single row header, Amp #640456-2

PIN	SIGNAL
1	SMB Clock
2	SMB Data

P23 - +5V VRM Supply

2 pin header, Amp #1586037-2

PIN	SIGNAL
1	+5V
2	+5V

P24 - +12V VRM POWER INPUT

4 pin header, Molex #39-29-3046

PIN	SIGNAL
1	GND

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales (800) 875-6031 • Phone (770) 287-3100 • Fax (770) 287-3150

Connectors (Continued)

P11 - Primary IDE Hard Drive Connector

40 pin dual row header, 3M #30340-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDP
29	DACK 0	30	Gnd
31	IRQ 14	32	NC
33	Add 1	34	PCBL DET*
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other Drives are detected, pin definition is Gnd.

2	GND
3	+12V
4	+12V

Memory

The Double Data Rate (DDR) memory interface consists of a single channel which terminates in two dual-in-line memory module (DIMM) sockets and supports auto detection of up to 2GB of memory. The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 64-bit wide gold finger PC1600 or PC2100 memory modules in 184-pin DIMM sockets.

NOTE: Memory modules can be installed in one or both DIMM sockets. If only one DIMM module is used, it should be populated in the top DIMM socket (Bank 2 - Bk2). If two modules of different speeds are used, the 845GV chipset sets the memory interface speed to the speed of the slower DIMM module. Registered DIMMs are *not* supported. All memory modules must have gold contacts.

The SBC supports DIMMs which are PC1600/PC2100 compliant and have the following features:

- 184-pin with gold-plated contacts
- Non-ECC (64-bit) DDR memory
- Unbuffered configuration
- X8, x16 construction
- Non-stacked (NS)

NOTE: Intel's DDR memory interface design guidelines for the 845GV chipset validate the use of *non-stacked* DIMM modules. Therefore, the T4G, which uses the 845GV chipset, supports *only* non-stacked DIMMs in its standard system BIOS.

DIMM Size	**DIMM Type**	Non-ECC	Component Construction
64 MB	Unbuffered	8M x 64	x8, x16, NS
128 MB	Unbuffered	16M x 64	x8, x16, NS
256 MB	Unbuffered	32M x 64	x8, x16, NS
512 MB	Unbuffered	64M x 64	x8, x16, NS
1 GB	Unbuffered	128M x 64	x8, x16, NS