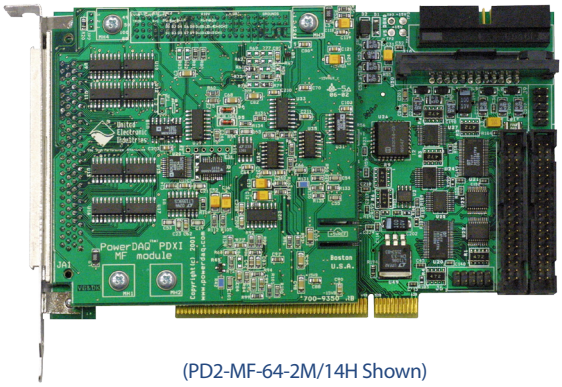
PD2-MF

PowerDAQ II PCI Multifunction Boards

- 16/64 single-ended or 8/32 differential A/D channels
- 150 kS/s – 2.2 MS/s sampling rate
- 12-, 14-, 16-bit resolution
- Gains 1,10,100,1000 or 1,2,4,8
- Two 12-bit analog outputs; 32 digital I/O lines; three 16-bit counter/timers
- Simultaneous operation of all subsystems
- Stream-to-disk capability
- Multiple boards operate in one PC
- Full PCI-bus implementation



(PD2-MF-64-2M/14H Shown)

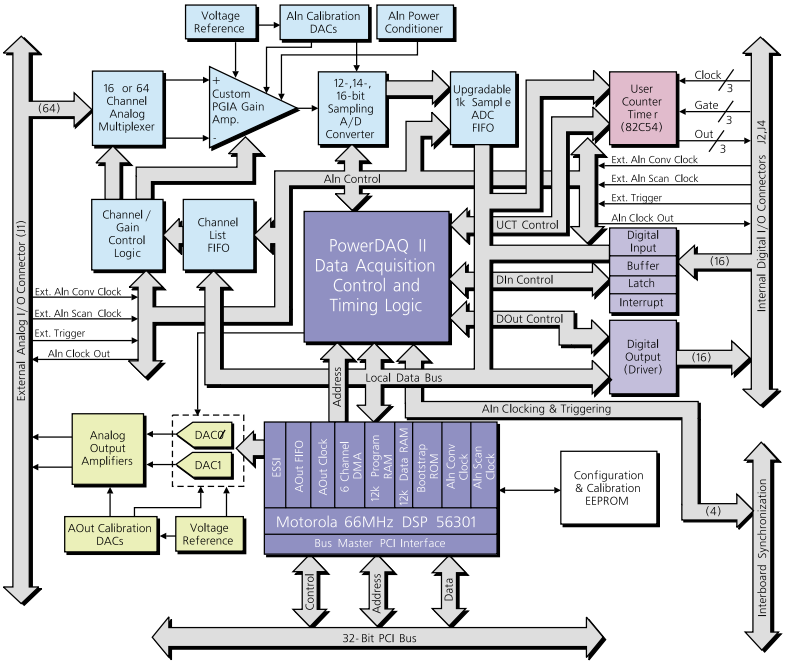
Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description:

When you know you'll be setting up a stimulus/response test, when you know you'll be implementing a closed-loop system or if you just want to be ready for any kind of testing situation, a multifunction board is the logical choice. Our PD2-MF Series boards pack everything you'll likely need: as many as 64 single-ended/32 differential analog inputs running at speeds to 2.2 MS/s, dual analog outputs, 32 digital I/O lines plus three counter/timers available to users.

To allow all these I/O subsystems to run simultaneously without loading down the host CPU, MF Series cards run under control of a Motorola DSP. Thus you can collect analog samples while generating waveforms yet have the resources to perform digital I/O and run the counter/ timers – all at the same time. Operating in this fashion presents no constraints on setup parameters, either: a custom PGIA (programmable-gain instrumentation amplifier) design runs any or all channels at different gains without the need to trade off peak throughput rate or accuracy.

Block Diagram:



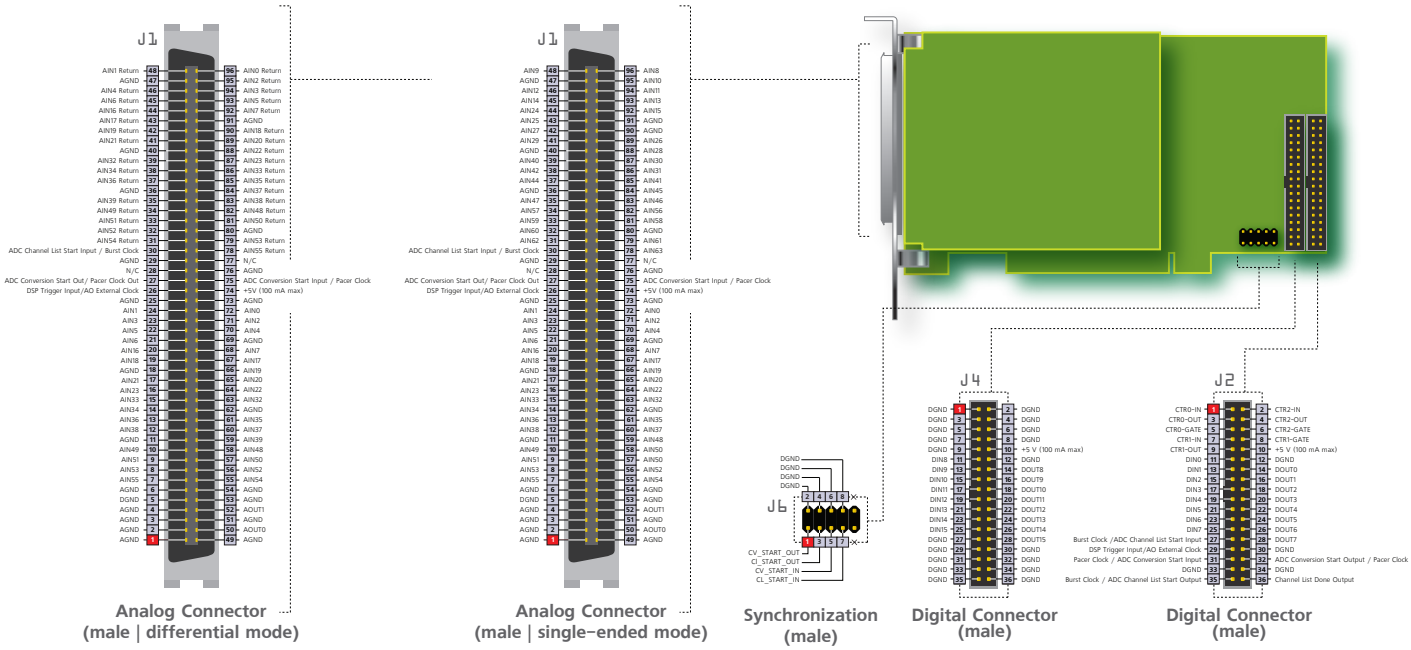
We supply a complete set of drivers for all popular programming languages and third-party applications including LabVIEW and Agilent VEE -- and at no additional charge! The support package also comes with example programs, complete with source code, that are so extensive that some of them might be enough to solve your problem straight out of the box.

To achieve optimum performance under Windows, we wrote the boards' 32-bit driver from scratch without relying on any legacy code. This advanced protocol-based driver works with shareable buffers in system RAM and makes obsolete traditional register-based drivers and double-buffering schemes. MF Series boards can stream data to disk continuously, gapfree, at the hardware?s peak acquisition rates!

Technical Specifications:

Model: PD2-MFS-xx-	2M/14H	1M/12x	500/16x	400/16x	333/16x	150/16x
Resolution	14 bits	12 bits	16 bits	14 bits	16 bits	16 bits
Number of Channels Single-Ended Differential	16 or 64 8 or 32					16 8
Maximum Sampling Rate (multiple channels)	2.2 MS/s	1 MS/s	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Onboard FIFO Size (upgradeable to 16k, 32k, 64k)	4k samples		2k samples	1k samples		
Input Ranges	0-5 V, ±5 V, 0-8 V, ±8 V @ 10 V ranges	0-5 V, 0-10 V ±5 V, ±10 V (software selectable)				
Channel-Gain List	256 entries					
Programmable Gains (by channel)	H=1, 2, 4, 8	L=1,10,100,1000 H=1, 2, 4, 8				
Drift Zero Gain	±30 µV/°C ±30 ppm/°C					
Input Impedance	10 MΩ					
Input Bias Current	±20 nA					
Input Overvoltage	±20V,2000V ESD 10 mA max	±35V cont.				
A/D Conversion Time	0.45 µs	0.8 µs	2 µs	2.5 µs	2.0 µs	6 µs
A/D Settling Time	0.37 µs	0.6 µs	1.2 µs	2.0 µs	1.2 µs	5 µs
DC Accuracy						
Nonlinearity (no missing codes)	±2 LSB	±0.5 LSB	±1 LSB	±0.5 LSB	±1 LSB	±1 LSB
System Noise	1.2 LSB	0.3 LSB	1.3 LSB	0.8 LSB	1.3 LSB	1.2 LSB
AC Accuracy						
Effective Number of Bits	12.2	11.63	14.5	13.1	14.5	14.8
Total Harmonic Distortion + Nonliearity + Noise	76 dB	71.8 dB	88 dB	81 dB	89 dB	91 dB
Channel Crosstalk	-80 dB @ 1 kS/s					
Clocking and Trigger Input						
Maximum A/D Pacer Clock	2200 kS/s @ 1 ch, 1800 kS/s @ all	1250 kS/s	500 kS/s	400 kS/s	333 kS/s	150 kS/s
External A/D Sample Clock Maximum Frequency	2200 kS/s @ 1 ch, 1800 kS/s @ all	1250 kS/s	500 kS/s	400 kS/s	333 kS/s	150 kS/s
Minimum Pulse Width	20 ns					
External Digital (TTL)Trigger High-level Input Voltage Low-level Input Voltage Minimum Pulse Width	2.0V min 0.8V min 20 ns					

Pinout Diagrams:



Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J1	PD-CBL-96	PD2-AO-STP-16	Carries analog output lines to 16-channel terminal panel
J2	PD-CBL-37	PD2-AO-STP-16	Carries 8 digital input and 8 digital output lines to 16-channel terminal panel
J1	PD-CBL-96	PD-BNC-64*	Carries analog output lines to 64-channel BNC terminal panel
J2	PD-CBL-37	PD-BNC-64	Carries 8 digital input and 8 digital output lines to 64-channel BNC terminal panel
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines
J1	PD-CBL-96	PD-AO-AMP-100	Amplifies analog outputs to ±100V per channel
J1	PD-CBL-96	PD-AO-AMP-115	Amplifies analog outputs to ±115V per channel

* PD-BNC-64 was initially designed for analog input subsytem of UEI's multifunction boards. Thus the analog output signals transfered via PD-CBL-96 will not match the signal designations on PD-BNC-64's J1 connector. See PowerDAQ Analog Output Manual for more details and remapping diagram.

Specifications: (PD2-MF-all models)

Digital I/O	
Input Bits (8 can generate IRQ)	16
Output Bits	16
Inputs High-level Input Voltage Low-level Input Voltage High-level Input Current Low-level Input Current	 2.0 V (min) 0.8 V (max) 20 µA -20 µA
Outputs	
Output Driver High Voltage Output Driver Low voltage:	2.5 V min, 3.0 V typ (I_{OH} = -32 mA) 0.55V max (I_{OL} = 64 mA)
Current Sink	-32/64 mA max, 250 mA per port
Pulse Width	20 ns min, interrupt bit latched on rising, falling or either edge
Power-on Voltage	Logic Zero
Counter/Timer	
Number of channels	3 available to user (Intel 82C54)
Resolution	16 bits on each counter
Clock Inputs Software configurable High-level Input voltage Low-level Input voltage High-level Input current Low-level Input current	 Internal 1 MS/s, External ≤ 10 MS/s 2.0V min 0.8V max 20 µA -20 µA
Gate Inputs Maximum Pulse Width	 100 ns (High) 100 ns (Low)
Counter Outputs Output Driver High Voltage Output Driver Low Voltage	Inverted 2.5V min (I_{OH} = 24 mA) 0.55V max (I_{OH} = 48 mA)

Analog Outputs	
Number of channels	2
Resolution	12 bits
Update Rate	200 kS/s each
Onboard FIFO Size	2k samples (on DSP)
Analog Output Range	±10 V
Error Gain Zero	 ±1 LSB Calibrated to 0
Current Output	±20 mA max
Output Impedance	0.3Ω typ
Capacitive Drive Capability	1000 pF
Nonlinearity	±1 LSB
Protection	Short circuit to analog ground
Power-on Voltage	0 V ±10 mV
Setting Time to 0.01% of FSR	10 µs, 20 V step 1 µs, 100 mV step
Slew Rate	30 V/µs
General Specifications	
Power Requirements	+5V or +3.3V
Physical Dimensions	10.5 x 3.8" (262 x 98 mm)
Environmental Operating Temperature Range Storage Temperature Range Relative Humidity	 0 to 70 °C -25 to 85 °C to 95%, noncondensing
Connector J1	96-pin high-density Fujitsu connector (male) (Fujitsu PN#FCN-245P096-G/U)
Connector J2	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J4	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J6	8-pin male connector (Adam-Tech PN#PH2-SMT-8-SGA

Ordering Guide:

Part Number	Description
PD2-MF-16-2M/14H	2.2 MS/s, 14-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-2M/14H	2.2 MS/s, 14-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-1M/12L	1.25 MS/s, 12-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-1M/12H	1.25 MS/s, 12-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 Digital I/O
PD2-MF-64-1M/12L	1.25 MS/s, 12-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-1M/12H	1.25 MS/s, 12-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-500/16L	500 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-500/16H	500 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-500/16L	500 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-500/16H	500 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-400/14L	400 kS/s, 14-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-400/14H	400 kS/s, 14-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-400/14L	400 kS/s, 14-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-400/14H	400 kS/s, 14-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-333/16L	333 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-333/16H	333 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-333/16L	333 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-64-333/16H	333 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-150/16L	150 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PD2-MF-16-50/16H	150 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
Upgrade FIFO	
PD-16KFIFO	Upgrade 1K FIFO to 16K FIFO
PD-32KFIFO	Upgrade 1K FIFO to 32K FIFO
PD-64KFIFO	Upgrade 1K FIFO to 64K FIFO