VPX6-COP

V 0.92 5/9/11

3U OpenVPX Coprocessor with Virtex6 FPGA computing core and FMC IO site

FEATURES

- 3U OpenVPX FPGA coprocessor card
- FMC I/O site (VITA 57) with 8x 5 Gbps MGT lanes, 80 LVDS pairs (LA, HA, HB full support)
- FPGA Computing Core
  - Xilinx Virtex6 SX315T, SX475T, LX240T or LX550T
  - 2 Banks of 1GB DRAM (2GB total)
  - 2 banks of 9MB QDRII+ SRAM (18MB total)
  - 128MB DDR3 DRAM
- VPXI system-timing features
  - Integrates with VPXI backplane timing
  - VPX backplane timing clock and trigger
  - VPX backplane shared triggers and flags
  - PLL with 10-1000 MHz range with 10 MHz 0.5 ppm reference or VPX timing clock
- System communications
  - x12 lanes, 5 Gbps
  - Dual PCIe or up to four Aurora ports
  - PCIe x8 Gen2 PCIe supports 2 GB/s sustained transfer rates
- < 15W typical excluding FMC
- Ruggedization Levels up to L4
  - forced air or conduction cooling
  - 40g shock, 9g sine, 0.1 g2/Hz random vibe
- IPMI health monitoring

APPLICATIONS

- Wireless Receivers – LTE, WiMAX, SATCOM
- RADAR, SIGINT, ECM, Medical Imaging
- High Speed Data Recording and Playback

SOFTWARE

- MATLAB/VHDL FrameWork Logic
- VxWorks, Linux, or Windows Drivers
- C++ Host Tools
- Andale Data Logging Support - record/play at 2 GB/s from 48TB RAID systems

DESCRIPTION

The VPX6-COP is a flexible FPGA co-processor card that integrates a Virtex6 FPGA computing core with an industry-standard FMC IO module on a 3U OpenVPX card.

The FPGA computing core features the Xilinx Virtex 6 FPGA family, in densities up to LX550 and SX475. The SX475 provides over 2000 DSP MAC elements operating at up to 500 MHz. The FPGA core has two 9MB QDRII+ SRAM banks, two 256MB LPDDR2 DRAM banks, and a 128MB DDR3 bank. Each memory is directly connected to the FPGA and is fully independent.

For system communications, the VPX6-COP has a x12 lanes supporting 5 Gbps full duplex per lane. The Framework logic implements a x8 Gen2 PCI Express and a x4 Aurora interface using the x12 lanes, although other configurations are possible. The primary PCIe port is a x8, Gen2 (5 Gbps) interface capable of up to 2 GB/s sustained operation with 4 GB/s burst rate. The secondary port is x4 lanes and supports PCIe, Aurora or custom protocols with bit rates up to 5 Gbps.

An FMC site, conforming to VITA 57, provides configurable IO for the VPX6-COP. The FMC site has full support for the high pin count connector, with over 80 LVDS pairs directly connected to the FPGA and x8 lanes at up to 5 Gbps per lane. FMC also is readily adapted to application-specific custom modules.

The VPX-COP family power is less than 15W for typical operation. The card is available in conduction or air cooled versions. Ruggedization levels for wide-temperature (-40 to 85C), humidity, and vibration (up to 40 g shock, 0.1g2/Hz) may be specified (see table). REDI covers are available for 2-level maintenance.

The FPGA logic can be fully customized using the Frame Work Logic tool set. The toolset provides support for both MATLAB and RTL designs. The MATLAB BSP supports real-time hardware-in-the-loop development using the graphical, block diagram Simulink environment with Xilinx System Generator. IP cores for a range of signal processing cores for applications such as wireless, RADAR and SIGINT such as DDC, demodulation, and FFT are also available.

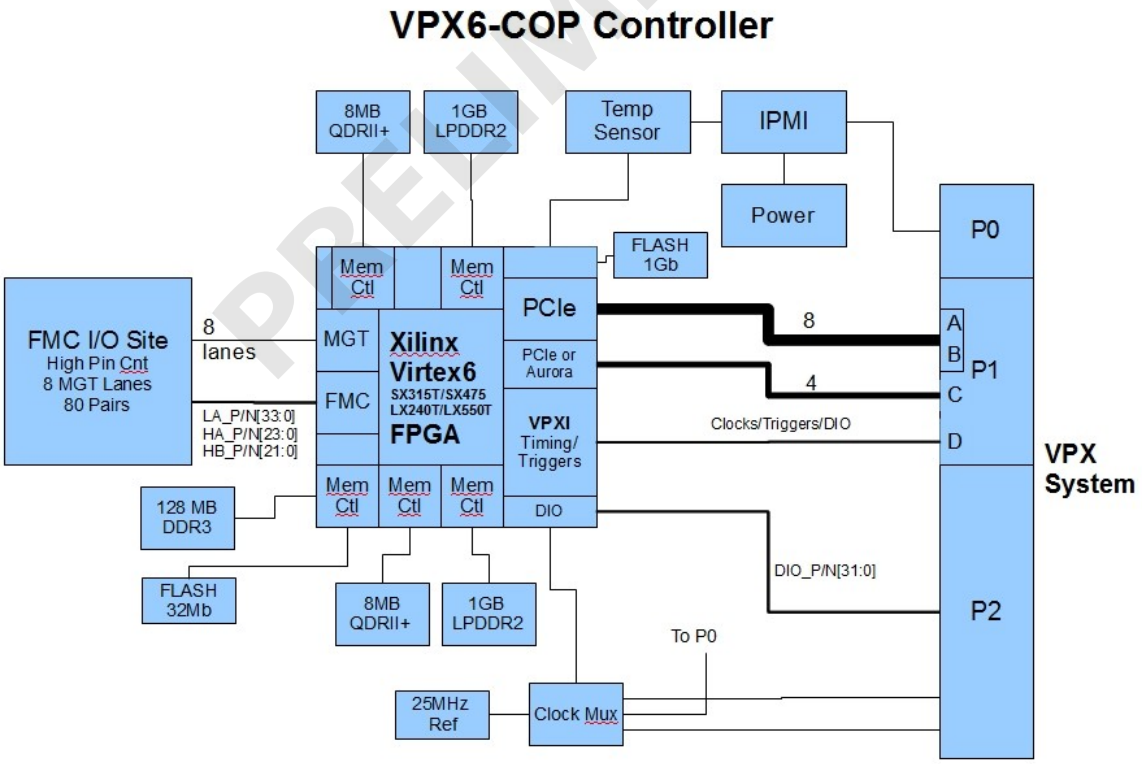
Software tools for host development include C++ libraries and drivers for VxWorks, Windows and Linux. Application examples demonstrating the module features are provided.

VPX6-COP

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
VPX6-COP	80262-2-<ER>	FPGA coprocessor for 3U VPX with FMC IO site; Xilinx SX315T FPGA, -1 speed grade; Does NOT support x8 Gen2 PCIe . <ER> is environmental rating (see following table) ** For alternate FPGAs or speed grades (LX240, LX550, SX475, contact sales)
VPX6-COP REDI Covers	61208	VITA48 REDI covers for VPX6-COP assembly.
VPX-COP FrameWork Logic	55033	VPX-COP FrameWork Logic board support package for RTL and MATLAB. Includes technical support for one year.
Software	57001	Malibu software installation DVD including drivers for Windows and Linux.



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Operating Environment Ratings

VPX6-COP rated for operating environment temperature, shock and vibration are offered. The card is qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

VPX6-COP

Standard Features

FMC Site	
Specification	VITA 57 FMC
Type	High Pin Count
High Speed Pairs	8 lanes (Tx/Rx pair) 5 Gbps max rate
Signal Pairs	80 pairs total LA: 34 pairs (Vcco = 2.5V, Vref from FMC) HA: 24 pairs (Vcco = 2.5V, Vref from FMC) HB: 22 pairs (Vcco and Vref from FMC)
IO Standards	LA, HA : LVCMOS25, LVDS25, LVDCI2, SSTL25, HSTL25 HB: all IO standards supported
Power	3.3V @ 3A (supplied by bus) 12V @ 1A (supplied by bus) 3.3V AUX @ 0.5A (supplied by bus) Vadj = 2.5V @ 4A

FPGA	
Device	Xilinx Virtex6
Speed Grades	-1 (commercial), -2 special order
Sizes	SX315T = ~ 31M gates equivalent SX475T = ~ 47.5M gates equivalent LX240T = ~ 24M gates equivalent LX550T = ~ 55M gates equivalent
Flip-Flops /Slices	SX315T: 393K /49K SX475T: 595K / 74K LX240T: 301K / 37K LX550T: 687K /85K
DSP48E1 elements/ BlockRAMs	SX315T: 1344 / 704 SX475T: 2016 /1064 LX240T: 768 /416 LX550T: 864 /632
GTH Ports	16 lanes @ 5 Gbps (-1 speed)
Configuration	JTAG or FLASH In-system reprogrammable

Memories	
LPDDR2 DRAM s	LPDDR2: 256Mx32 2GB; 2 banks of 1GB 333 MHz clock rate (up to 500 MHz) 5.2GB/s sustained transfer rate (sequential read/writes)
DDR3 DRAM	DDR3: 128Mx16 256MB total (one device) Up to 512MB available 333 MHz clock rate (up to 500 MHz) 2.6 GB/S burst transfer rate
Program FLASH	Serial FLASH 8MB SPI interface
Configuration FLASH	Parallel FLASH 128 MB configures FPGA through CPLD loader

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Host Interfaces	
Lanes	x12 lanes, 5 Gbps (-1 FPGA speed)
PCI Express	x8, x4 or x1 port configurations on VPX ports A, B, C Gen2 (5 Gbps) x8 port REQUIRES -2 speed FPGA Up to 2GB/s sustained transfer rate Up to 4 GB/s burst transfer rate Gen 1 supported for x1, x4, x8 ports
Aurora Ports	x8, x4, x2, or x1 port configurations on VPX ports A,B, C 5 Gbps for all configurations Up to 3.5 GB/s sustained transfer rates
VPX Module Profiles per ANSI/VITA 65	MOD3-PAY-1D-16.2.6-1 (PCIe x8 Gen1) MOD3-PAY-1D-16.2.6-2 (PCIe x8 Gen2) MOD3-PAY-2F-16.2.7-1 (Two PCIe x4 ports Gen1) MOD3-PAY-2F-16.2.7-2 (Two PCIe x4 ports Gen2)

VPXI Clocks and Triggering	
Clock Sources	6 total: 2 global, 4 local LVDS pairs
Trigger Sources	8 total: 2 global, 4 local, 2 FPGA LVDS pairs
Timing Synchronization	2 multi-drop LVDS pairs 2 open-collector system-wide flags
Clock References	25 MHz reference from VPX bus 10 MHz, 0.5 PPM reference clock 1 PPS from VPX bus
Sample Clock Generation	Programmable PLL with 10-945, 970-1134, 1213-1417 MHz range 100 kHz tuning resolution 2 clock to FMC, 4 to VPXI bus, 2 to FPGA

Monitoring	
Alerts	Temperature Warning, Temperature Failure, Power Faults
Alert Timestamping	5 ns resolution, 32-bit counter

Application IO (P2)	
DIO Bits	32, arranged as 16 pairs
Signal Standards	LVTTL (2.5V) – NOT 3.3 compatible LVDS

Power	
Consumption	15W typical
Temperature Monitor	Software with programmable alarms
Over-temp Monitor	Disables power supplies
Power Control	LPDDR2 deep sleep mode QDR shutdown FMC power controls
Heat Sinking	Conduction cooling supported (VITA20 subset)

Physicals	
Form Factor	3U VPX, 0.8in pitch
Size	160 x 100 mm (6.3 x 3.9in)
Weight	250 g
Hazardous Materials	Lead-free and RoHS compliant

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Architecture and Features

The VPX6-COP architecture integrates a Xilinx Virtex6 FPGA computing core with an FMC module on a 3U Open VPX card. System communications using x12 lanes supports PCI Express, Aurora or custom protocols. This architecture tightly couples the FPGA to the FMC and enables the module to perform real-time signal processing with low latency and extremely high rates. It is well-suited for front-end signal processing applications in wireless, RADAR and medical imaging.

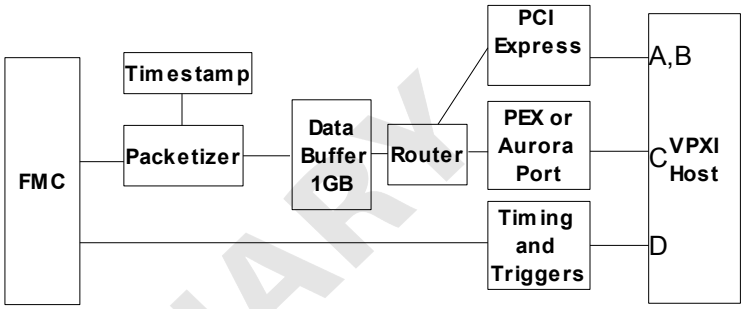
FMC Module

The FMC module (VITA 57) directly connects to the FPGA with 80 pairs of LVDS (160 single-ended) and 8 lanes of 5Gbps serial. The serial lanes connect to the FPGA GTP ports. The logic interface to the FMC is defined by the logic, making it completely flexible for custom designs.

VPXI Timing Support

Support for FMC integration with system devices includes clock and trigger inputs from the VPX bus interface in a suitably equipped backplane. Up to four sample clocks and four trigger inputs are provided, as well as synchronization signals for timing and sampling coordination.

Data flows between the IO and the host using a packet system



Example VPX6-COP Architecture

FPGA Core

The VPX6-COP has a Virtex6 FPGA and memory at its core for DSP and control. The Virtex6 FPGA is capable of over 1 Tera MACs (SX315T operating at 500 MHz internally) with over 1300 DSP elements in the SX315T FPGA. In addition to the raw processing power, the FPGA fabric integrates logic, memory and connectivity features that make the VPX6-COP capable performing very demanding real-time signal processing.

The FPGA has direct access to two banks of 1GB of LPDDR2 DRAM, two banks of 9MB QDRII+ SRAM and a single bank of 128MB DDR3. These memories allow the FPGA working space for computation, required by DSP functions like FFTs, and storage for algorithms involving large arrays or data sets. Memory controller IP implements data buffers and pattern generation for applications. The DDR3 is compatible with embedded processors (uBlaze).

All IO, memory and host interfaces connect directly to the FPGA – providing direct connection to the data and control for maximum flexibility and performance. Logic utilization is typically <10% of the device.

VPX Host Interface

The VPX6-COP host interface has x12 lanes of 5 Gbps serial IO. These lanes may be used as PCI Express, Aurora or custom protocol ports of widths from x1 to x8 lanes per port. These ports allow the VPX6 to be used in many system topologies, including private data channels between cards. The FrameWork Logic implements a x8 PCI Express port on VPX ports A-B, and x4 Aurora port on VPX port C.

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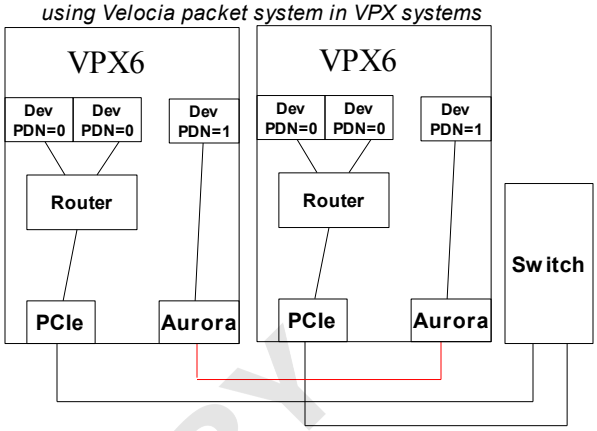
The PCIe and Aurora ports are integrated with the Velocia packet system that efficiently handles data transfers between multiple, independent data sources between the VPX6-COP and the host or other cards.

A set of logic components is provided in the FrameWork Logic to implement the packet system including packetizer, depacketizer, router and buffer memory controls. Packetizing includes timestamping per VITA 49. Data within the packets may be any format.

Real-time system architectures are enabled using Velocia packet system in VPX systems



Example VPX System Topology:
PCIe star with private Aurora channel

IPMI and Card Management Features

The VPX6-COP has IPMI support for system management that monitors power consumption, temperature and other health indicators. Independent monitoring of the FPGA die temperature shuts down the card to prevent damage from overheating. The card also has over-current protection that disconnects system power in case of failure and a watchdog timer to prevent runaway operation.

FPGA Configuration

The modules uses a FLASH memory for the Virtex 6 FPGA image. There are two images in the FLASH: an application image and a "golden" image as a backup.

During development, the JTAG interface to the FPGA is used for development tools such as ChipScope and MATLAB. The FPGA JTAG connector is compatible with Xilinx Platform USB Cable. After development is completed, the FLASH can be programmed in-system using a software applet.

Applications requiring secure storage may configure the FPGA via IPMI, allowing remote secure storage for the logic image.

Software Tools

Software development tools for the module provides comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high speed data acquisition easier to integrate into applications.

Software for data logging and analysis are provided with every module. Data can be logged to system memory at full rate or to disk drives at rates supported by the drive and controller. Triggering and sample rate controls allow you to use the module's performance in your applications without ever writing code. Innovative software applets include *Binview* which provides data viewing, analysis and import to MATLAB for large data files.

Support for the Microsoft, Embarcadero and GNU C++ toolchains is provided. Supported OSes include VxWorks,Windows and Linux. For more information, the software tools User Guide and on-line help may be downloaded.

Logic Tools

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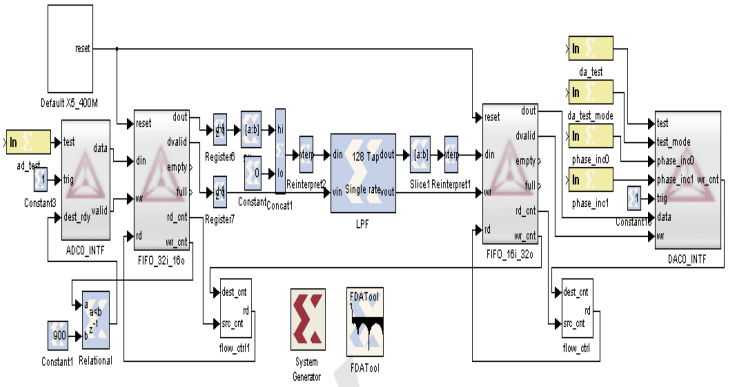
High speed DSP, analysis, customized triggering and other unique features may be added to the module by modifying the logic. The FrameWork Logic tools provide support for VHDL/Verilog and MATLAB developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Innovative components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. Each design is provided as a Xilinx ISE project with source and netlists, and a ModelSim testbench illustrating logic functionality.



Using MATLAB Simulink for Logic Design

The MATLAB Board Support Package (BSP) supports logic development using Simulink and Xilinx System Generator. These tools are a graphical design environment that integrates the logic into MATLAB Simulink for complete hardware-in-the-loop testing and development. This is an extremely power design methodology, since MATLAB can be used to generate, analyze and display the signals in the logic real-time in the system. Once the development is complete, the logic can be embedded in the FrameWork logic using the RTL tools.

IP for Virtex6 FPGA

Innovative provides a range of down-conversion channelizer logic cores for wideband and narrowband receiver applications for the X6 family. The DDC channel densities range from 4 to 256, and include programmable channel filters, decimation rates, tuning and gain controls. An integrated power meter allows the DDC to measure any channel power for AGC controls. Multiple cores can be used for higher channel counts.

Each IP core is provided with a MATLAB simulation model that shows bit-true, cycle-true functionality. Signal processing designers can then use this model for channel design and performance studies. Filter coefficients and other parameters from the MATLAB simulation can be directly loaded to the hardware for verification.

Part Number	IP Core	Channels	Tuning	Decimation	Max Bandwidth	Channel Filter
58014	IP-MDDC4	4	Fs/2^32	16 to 32768	Fs/16	Programmable 100 tap filter
58015	IP-MDDC128	128	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter
58528	IP-DDC256	256	Fs/2^32	512 to 16384	Fs/512	Programmable 100 tap filter

Signal processing cores for communications applications are available for Virtex6.

Part Number	IP Core	Features
58001	PSK Demodulation	N=2,4,8,PI/4. Integrated carrier tracking and bit decision. Data rate to 160 Mbps.
58018	PSK Modulator	N=2,4,8,PI/4. Data rates up to 160 Mbps.
58002	CPFSK Demodulation	MSK and FSK demodulation
58019	CPFSK Modulator	MSK and FSK modulation
58020	QAM Modulator	Quadrature Amplitude Modulator.

58003	TinyDDS	Tiny DDS, 1/3 to ½ size of Xilinx DDS with equal SFDR, clock rates to 400 MHz with flow control
58011	XLFFT	IP core for 64K to 1M FFTs with windowing functions.
58012	Windowing	IP core for Hann, Blackman and uniform data windowing functions.
58013	CORDIC	IP core for sine/cosine generation using CORDIC method, resulting in 1/3 logic size of standard DDS cores.
58030	MDUC128	128-channel digital upconverter.

OFDM and LTE Cores

58029	OFDM Transmitter	OFDM transmit with IFFT, Windowing, Filtering, Cyclic Prefix and Upsample.
58031	OFDM Receiver	OFDM receiver with synchronization, downconversion and channel filtering.
58032	LTE Dowlink Transmitter	LTE downlink transmitter core for FDD mode.
58033	LTE Uplink Receiver	LTE uplink receiver core for FDD mode includes 2K FFT, timing and frame synchronization using ML estimation method, decoding of SSS and PSS signals for cell ID and frame sync.

Deployment

The VPX6-COP is compatible with many VPX system topologies that are built on PCI Express, Aurora, or SRIO. The x12 lanes of high speed serial to the backplane support multiple ports and widths and may be changed as part of the logic design.

OpenVPX (ANSI/VITA 65) defines compatibility codes for several possible host interface configurations.

Core	Ports	Lanes	Bandwidth	VPX Ports	VPX Compatibility
PCI Express Gen1 * standard configuration	1	x8	~1.2GB/s sustained	A-B	MOD3-PAY-1D-16.2.6-1
PCI Express Gen2	1	x8	~2.2GB/s sustained	A-B	MOD3-PAY-1D-16.2.6-2
PCI Express Gen1	2	x4	~800MB/s sustained	A and B	MOD3-PAY-2F-16.2.7-1
PCI Express Gen2	2	x4	~1.2GB/s sustained	A and B	MOD3-PAY-2F-16.2.7-2

Innovative offers a 3U VPX system with integrated timing and Intel CPU compatible with the VPX6-COP. Contact sales for application engineering support for system integration and information on ruggedization.

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3U VPX PC with Four Expansion Slots and Integrated Timing (90271)

3U VPX, air-cooled chassis with backplane
Rns Windows, Linux, VxWorks
Intel Dual Core i5 or i7, 8GB, 256MB SSD
4x USB, GbE, x8 cable PCIe, Displayport, timing expansion
Integrated timing clocks and triggers with GPS option
400 MB/s, 1TB datalogger
AC or DC operation

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