NBC12429

3.3V/5V Programmable PLL Synthesized Clock Generator

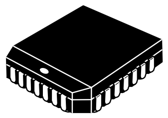
25 MHz to 400 MHz

The NBC12429 is a general purpose, PLL based synthesized clock source. The VCO will operate over a frequency range of 200 MHz to 400 MHz. The VCO frequency is sent to the N-output divider, where it can be configured to provide division ratios of 1, 2, 4, or 8. The VCO and output frequency can be programmed using the parallel or serial interfaces to the configuration logic. Output frequency steps of 1.0 MHz can be achieved using a 16 MHz crystal, depending on the output dividers. The PLL loop filter is fully integrated and does not require any external components.

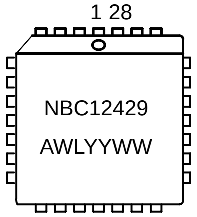
- Best-in-Class Output Jitter Performance, ±20 ps Peak-to-Peak
- 25 MHz to 400 MHz Programmable Differential PECL Outputs
- Fully Integrated Phase-Lock-Loop with Internal Loop Filter
- Parallel Interface for Programming Counter and Output Dividers During Power-Up
- Minimal Frequency Overshoot
- Serial 3-Wire Programming Interface
- Crystal Oscillator Interface
- Operating Range: V_{CC} = 3.135 V to 5.25 V
- CMOS and TTL Compatible Control Inputs
- Drop-in Replacement for Motorola MC12429

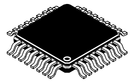
http://onsemi.com

MARKING DIAGRAMS

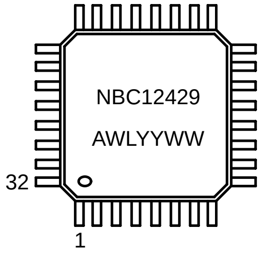


PLCC-28
FN SUFFIX
CASE 776





LQFP-32
FA SUFFIX
CASE 873A



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NBC12429FN	PLCC-28	37 Units/Rail
NBC12429FNR2	PLCC-28	500 Tape & Reel
NBC12429FA	LQFP-32	250 Units/Tray
NBC12429FAR2	LQFP-32	2000 Tape & Reel

January, 2003 - Rev. 2

Publication Order Number:
NBC12429/D

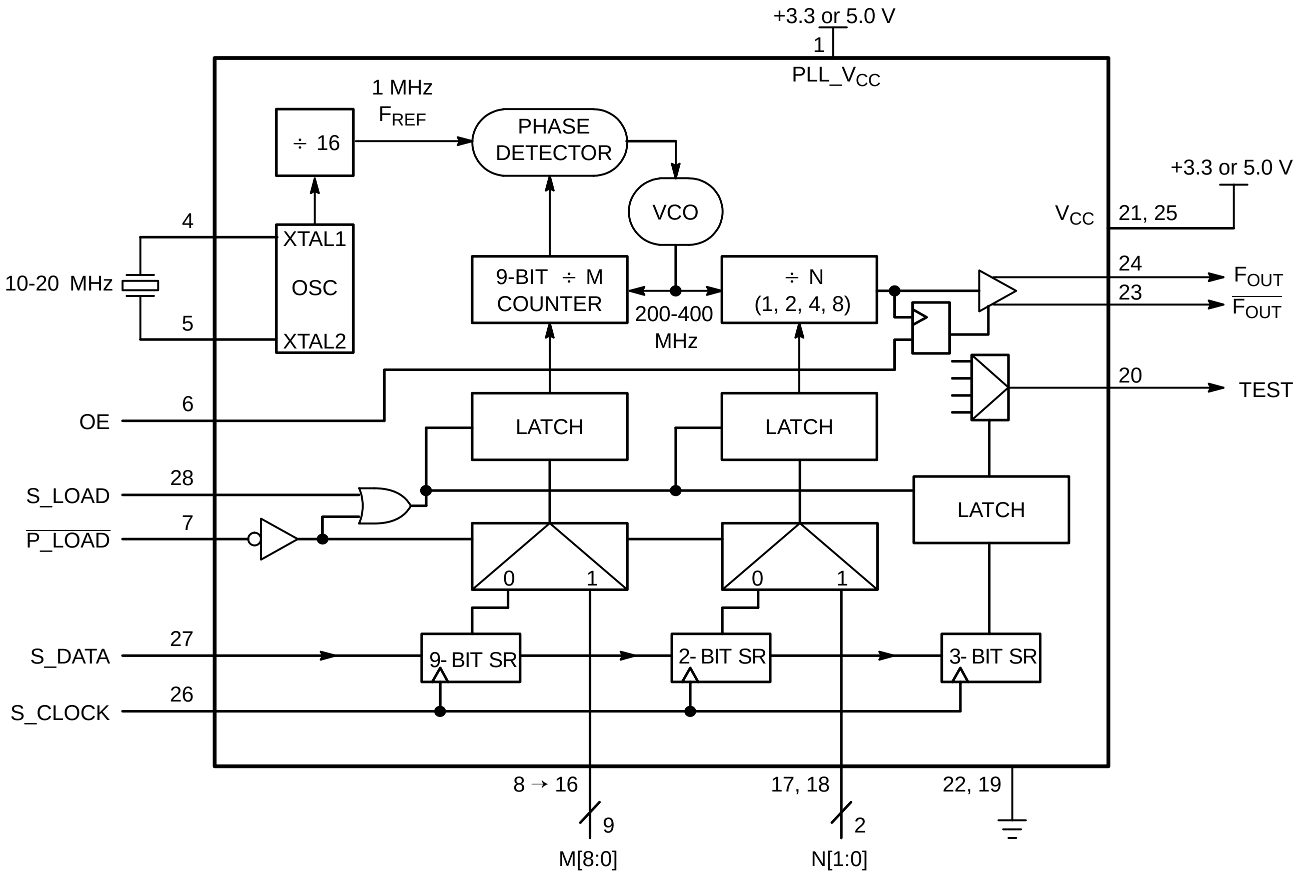


Figure 1. NBC12429 Block Diagram (28-Lead PLCC)

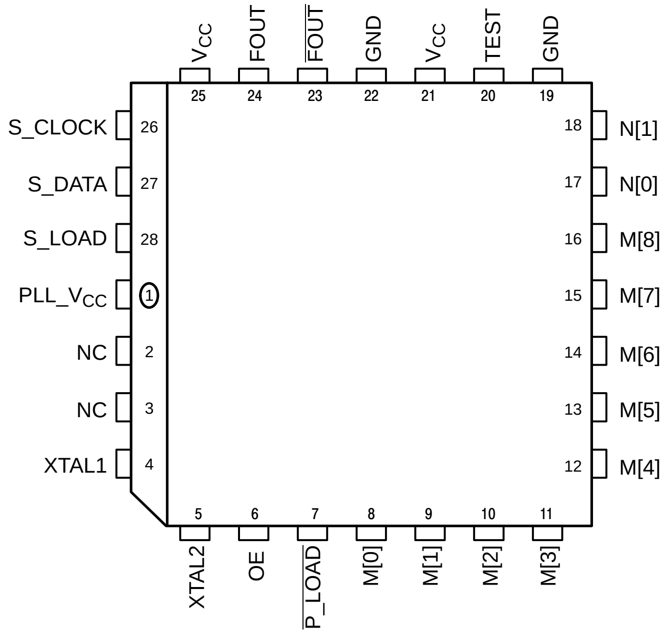


Figure 2. 28-Lead PLCC (Top View)

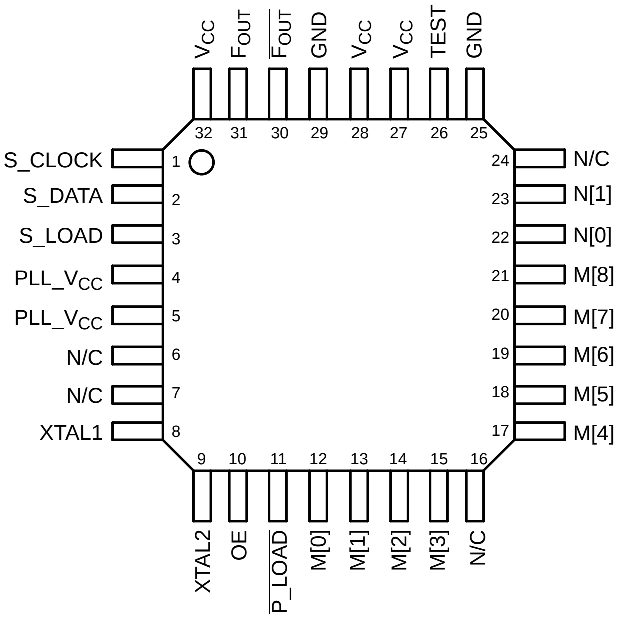


Figure 3. 32-Lead LQFP (Top View)

The following gives a brief description of the functionality of the NBC12429 Inputs and Outputs. Unless explicitly stated, all inputs are CMOS/TTL compatible with either pull-up or pulldown resistors. The PECL outputs are capable of driving two series terminated 50 Ω transmission lines on the incident edge.

PIN FUNCTION DESCRIPTION

Pin Name	Function	Description
INPUTS		
XTAL1, XTAL2	Crystal Inputs	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD*	CMOS/TTL Serial Latch Input (Internal Pulldown Resistor)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA*	CMOS/TTL Serial Data Input (Internal Pulldown Resistor)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK*	CMOS/TTL Serial Clock Input (Internal Pulldown Resistor)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$**	CMOS/TTL Parallel Latch Input (Internal Pullup Resistor)	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW; therefore, the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.
M[8:0]**	CMOS/TTL PLL Loop Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB.
N[1:0]**	CMOS/TTL Output Divider Inputs (Internal Pullup Resistor)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$.
OE**	CMOS/TTL Output Enable Input (Internal Pullup Resistor)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the FOUT output.
OUTPUTS		
F_{OUT}, $\overline{F_{OUT}}$	PECL Differential Outputs	These differential, positive-referenced ECL signals (PECL) are the outputs of the synthesizer.
TEST	CMOS/TTL Output	The function of this output is determined by the serial configuration bits T[2:0].
POWER		
V_{CC}	Positive Supply for the Logic	The positive supply for the internal logic and output buffer of the chip, and is connected to +3.3 V or +5.0 V.
PLL_V_{CC}	Positive Supply for the PLL	This is the positive supply for the PLL and is connected to +3.3 V or +5.0 V.
GND	Negative Power Supply	These pins are the negative supply for the chip and are normally all connected to ground.

* When left Open, these inputs will default LOW.
** When left Open, these inputs will default HIGH.

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 1 kV
Moisture Sensitivity (Note 1)		PLCC Level 1 LQFP Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		2035
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Supply	GND = 0 V	-	6	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge	- -	50 100	mA mA
TA	Operating Temperature Range	-	-	0 to +70	°C
T_{stg}	Storage Temperature Range	-	-	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	28 PLCC	22 to 26	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C	-	265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%)

			0°C			25°C			70°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IH} LVCMOS/LVTTL	Input HIGH Voltage	V_{CC} = 3.3 V	2.0	-	-	2.0	-	-	2.0	-	-	V
V_{IL} LVCMOS/LVTTL	Input LOW Voltage	V_{CC} = 3.3 V	-	-	0.8	-	-	0.8	-	-	0.8	V
I_{IN}	Input Current		-	-	1.0	-	-	1.0	-	-	1.0	mA
V_{OH}	Output HIGH Voltage TEST	I_{OH} = -0.8 mA	2.5	-	-	2.5	-	-	2.5	-	-	V
V_{OL}	Output LOW Voltage TEST	I_{OL} = 0.8 mA	-	-	0.4	-	-	0.4	-	-	0.4	V
V_{OH} PECL	Output HIGH Voltage F_{OUT} $\overline{F_{OUT}}$	V_{CC} = 3.3 V (Notes 3, 4)	2.155	-	2.405	2.155	-	2.405	2.155	-	2.405	V
V_{OL} PECL	Output LOW Voltage F_{OUT} $\overline{F_{OUT}}$	V_{CC} = 3.3 V (Notes 3, 4)	1.355	-	1.605	1.355	-	1.605	1.355	-	1.605	V
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		48 18	56 22	70 26	48 18	58 22	70 26	48 18	61 22	70 26	mA mA

3. $F_{OUT}/\overline{F_{OUT}}$ output levels will vary 1:1 with V_{CC} variation.
4. F_{OUT}/F_{OUT} outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.

DC CHARACTERISTICS (V_{CC} = 5.0 V ± 5%)

			0°C			25°C			70°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IH} CMOS/TTL	Input HIGH Voltage	V_{CC} = 5.0 V	2.0	-	-	2.0	-	-	2.0	-	-	V
V_{IL} CMOS/TTL	Input LOW Voltage	V_{CC} = 5.0 V	-	-	0.8	-	-	0.8	-	-	0.8	V
I_{IN}	Input Current		-	-	1.0	-	-	1.0	-	-	1.0	mA
V_{OH}	Output HIGH Voltage TEST	I_{OH} = -0.8 mA	2.5	-	-	2.5	-	-	2.5	-	-	V
V_{OL}	Output LOW Voltage TEST	I_{OL} = 0.8 mA	-	-	0.4	-	-	0.4	-	-	0.4	V
V_{OH} PECL	Output HIGH Voltage F_{OUT} $\overline{F_{OUT}}$	V_{CC} = 5.0 V (Notes 5, 6)	3.855	-	4.105	3.855	-	4.105	3.855	-	4.105	V
V_{OL} PECL	Output LOW Voltage F_{OUT} $\overline{F_{OUT}}$	V_{CC} = 5.0 V (Notes 5, 6)	3.055	-	3.305	3.055	-	3.305	3.055	-	3.305	V
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		50 19	58 23	75 27	50 19	60 23	75 27	50 19	65 23	75 27	mA mA

5. $F_{OUT}/\overline{F_{OUT}}$ output levels will vary 1:1 with V_{CC} variation.
6. F_{OUT}/F_{OUT} outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 volts.

AC CHARACTERISTICS (V_{CC} = 3.125 V to 5.25 V ± 5%; T_A = 0° to 70°C) (Note 8)

Symbol	Characteristic	Condition	Min	Max	Unit
F_{MAXI}	Maximum Input Frequency S_CLOCK Xtal Oscillator	(Note 7)	- 10	10 20	MHz
F_{MAXO}	Maximum Output Frequency VCO (Internal) F_{OUT}		200 25	400 400	MHz
t_{LOCK}	Maximum PLL Lock Time		-	10	ms
t_{jitter}	Cycle-to-Cycle Jitter (1 σ)	See Applications Section	-	± 20	ps
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$		20 20 20	- - -	ns
t_h	Hold Time S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$		20 20	- -	ns
t_{pwMIN}	Minimum Pulse Width S_LOAD $\overline{\text{P\_LOAD}}$		50 50	- -	ns
DCO	Output Duty Cycle		47.5	52.5	%
t_r, t_f	Output Rise/Fall F_{OUT}	20%-80%	175	425	ps

7. 10 MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
8. $F_{OUT}/\overline{F_{OUT}}$ outputs are terminated through a 50 Ω resistor to V_{CC} - 2.0 V.

FUNCTIONAL DESCRIPTION

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 1 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, Table 1, any crystal in the 10-20 MHz range can be used, Table 3.

The VCO within the PLL operates over a range of 200 to 400 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated into 50 Ω to V_{CC}-2.0 V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface logic is implemented with a fourteen bit shift register scheme. The register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. With P_LOAD held high, the configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

Table 1. Programming VCO Frequency Function Table

VCO Frequency (MHz)	M Count*	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
200	200	0	1	1	0	0	1	0	0	0
201	201	0	1	1	0	0	1	0	0	1
202	202	0	1	1	0	0	1	0	1	0
203	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
397	397	1	1	0	0	0	1	1	0	1
398	398	1	1	0	0	0	1	1	1	0
399	399	1	1	0	0	0	1	1	1	1
400	400	1	1	0	0	1	0	0	0	0

*With 16 MHz crystal.

PROGRAMMING INTERFACE

Programming the NBC12429 is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \div N \qquad \text{(eq. 1)}$$

where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16 MHz input reference.

Assuming that a 16 MHz reference frequency is used the above equation reduces to:

$$FOUT = M \div N \qquad \text{(eq. 2)}$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 2. Programmable Output Divider Function Table

N1	N0	N Divider	F_{OUT}	Output Frequency Range (MHz)*
0	0	÷1	M	200-400
0	1	÷2	M ÷ 2	100-200
1	0	÷4	M ÷ 4	50-100
1	1	÷8	M ÷ 8	25-50

*For crystal frequency of 16 MHz.

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 200-400 MHz, 100-200 MHz, 50-100 MHz and 25-50 MHz, respectively. From these ranges, the user will establish the value of N required. The value of M can then be calculated based on equation 1. For example, if an output frequency of 131 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 131 MHz falls within the frequency range set by an N value of 2; thus, N [1:0] = 01. For N = 2, $F_{OUT} = M \div 2$ and $M = 2 \times F_{OUT}$. Therefore, M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure, a user can generate any whole frequency desired between 25 and 400 MHz. Note that for N > 2, fractional values of F_{OUT} can be realized. The size of the programmable frequency steps (and thus, the indicator of the fractional output frequencies achievable) will be equal to $F_{XTAL} \div 16 \div N$.

For input reference frequencies other than 16 MHz, see Table 3, which shows the usable VCO frequency and M divider range.

The input frequency and the selection of the feedback divider M is limited by the VCO frequency range and F_{XTAL}. M must be configured to match the VCO frequency range of 200 to 400 MHz in order to achieve stable PLL operation.

$$M_{min} = f_{VCOmin} \div (f_{XTAL} \div 16) \text{ and} \qquad \text{(eq. 3)}$$

$$M_{max} = f_{VCOmax} \div (f_{XTAL} \div 16) \qquad \text{(eq. 4)}$$

The value for M falls within the constraints set for PLL stability. If the value for M fell outside of the valid range, a different N value would be selected to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the $\overline{\text{P\_LOAD}}$ signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the $\overline{\text{P\_LOAD}}$ signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the F_{OUT} output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the $\overline{\text{P\_LOAD}}$ signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final nine bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1, and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figures 4 and 5 illustrate the timing diagram for both a parallel and a serial load of the NBC12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1, and T0 control bits are preset to ‘000’ when $\overline{\text{P\_LOAD}}$ is LOW so that the PECL F_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Table 3. NBC12429 Frequency Operating Range

VCO Frequency Range for a Crystal Frequency of:								Output Frequency for F_{XTAL} = 16 MHz and for N =			
M	**M[8:0]**	**10**	**12**	**14**	**16**	**18**	**20**	**1**	**2**	**4**	**8**
160	010100000						200				
170	010101010						212.5				
180	010110100					202.5	225				
190	010111110					213.75	237.5				
200	011001000				200	225	250	200	100	50	25
210	011010010				210	236.25	262.5	210	105	52.5	26.25
220	011011100				220	247.5	275	220	110	55	27.5
230	011100110			201.25	230	258.75	287.5	230	115	57.5	28.75
240	011110000			210	240	270	300	240	120	60	30
250	011111010			218.75	250	281.25	312.5	250	125	62.5	31.25
260	100000100			227.5	260	292.5	325	260	130	65	32.5
270	100001110		202.5	236.25	270	303.75	337.5	270	135	67.5	33.75
280	100011000		210	245	280	315	350	280	140	70	35
290	100100010		217.5	253.75	290	326.25	362.5	290	145	72.5	36.25
300	100101100		225	262.5	300	337.5	375	300	150	75	37.5
310	100110110		232.5	271.25	310	348.75	387.5	310	155	77.5	38.75
320	101000000	200	240	280	320	360	400	320	160	80	40
330	101001010	206.25	247.5	288.75	330	371.25		330	165	82.5	41.25
340	101010100	212.5	255	297.5	340	382.5		340	170	85	42.5
350	101011110	218.75	262.5	306.25	350	393.75		350	175	87.5	43.75
360	101101000	225	270	315	360			360	180	90	45
370	101110010	231.25	277.5	323.75	370			370	185	92.5	46.25
380	101111100	237.5	285	332.5	380			380	190	95	47.5
390	110000110	243.75	292.5	341.25	390			390	195	97.5	48.75
400	110010000	250	300	350	400			400	200	100	50
410	110011010	256.25	307.5	358.75							
420	110100100	262.5	315	367.5							
430	110101110	268.75	322.5	376.25							
440	110111000	275	330	385							
450	111000010	281.25	337.5	393.75							
460	111001100	287.5	345								
470	111010110	293.75	352.5								
480	111100000	300	360								
490	111101010	306.25	367.5								
500	111110100	312.5	375								
510	111111110	318.75	382.5								

Most of the signals available on the TEST output pin are useful only for performance verification of the NBC12429 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the NBC12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Figure 6 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250 MHz or less. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	**T1**	**T0**	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	F_{REF}
0	1	1	M COUNTER OUT
1	0	0	F_{OUT}
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	F_{OUT} ÷ 4

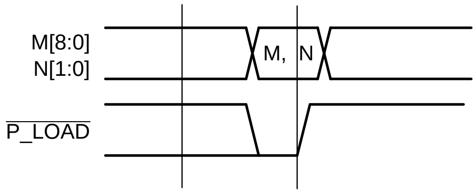


Figure 4. Parallel Interface Timing Diagram

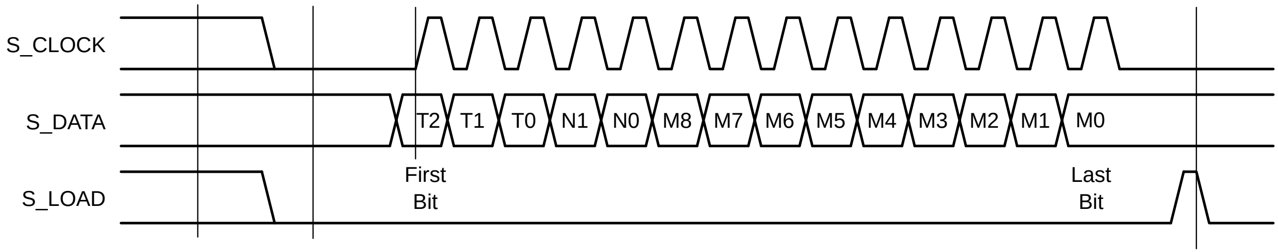
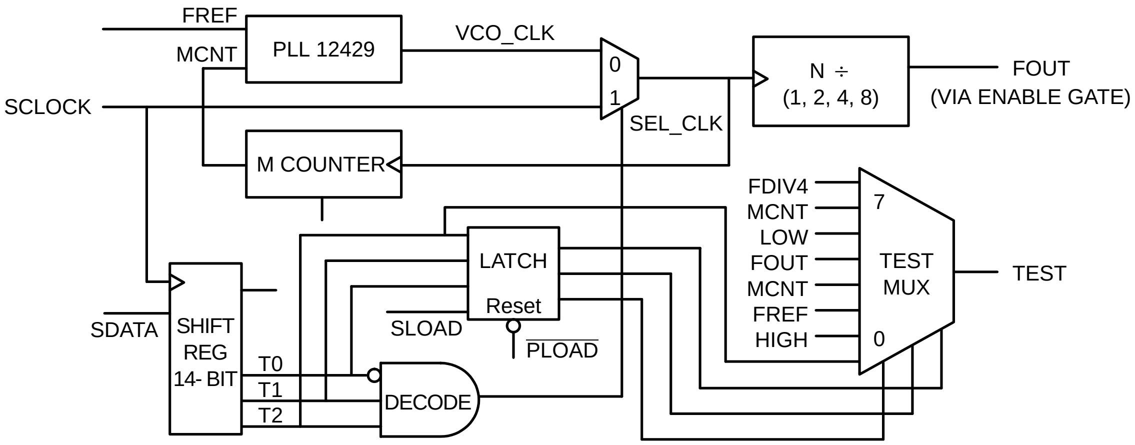


Figure 5. Serial Interface Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK ÷ N is on FOUT pin.

$\overline{\text{PLOAD}}$ acts as reset for test pin latch. When latch reset, T2 data is shifted out TEST pin.

Figure 6. Serial Test Clock Block Diagram

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The NBC12429 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NBC12429 as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the crystal terminals, loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance, it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required, it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 Ω and 1 KΩ.

The oscillator circuit is a series resonant circuit and thus, for optimum performance, a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the NBC12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified (a few hundred ppm translates to kHz inaccuracies). In a general computer application, this level of inaccuracy is immaterial. Table 4 below specifies the performance requirements of the crystals to be used with the NBC12429.

Table 4. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5 ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The NBC12429 is a mixed analog/digital product and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The NBC12429 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_V_{CC}) of the device. The purpose of this design technique is to try and isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_V_{CC} pin for the NBC12429.

Figure 7 illustrates a typical power supply filter scheme. The NBC12429 is most susceptible to noise with spectral content in the 1 KHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_V_{CC} pin of the NBC12429. From the data sheet, the PLL_V_{CC} current (the current sourced through the PLL_V_{CC} pin) is typically 23 mA (27 mA maximum). Assuming that a minimum of 2.8 V must be maintained on the PLL_V_{CC} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 7 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 KHz. As the noise frequency crosses the series resonant point of an individual capacitor, it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

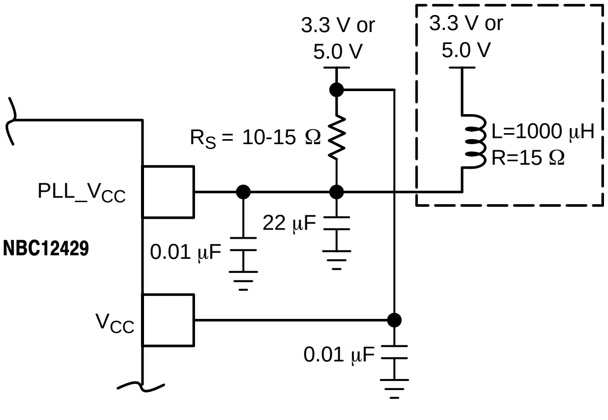


Figure 7. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 7 shows a 1000 μH choke. This value choke will show a significant impedance at 10 KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_V_{CC} pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement, and provide an adequate level of supply filtering.

The NBC12429 provides sub-nanosecond output edge rates and therefore a good power supply bypassing scheme is a must. Figure 8 shows a representative board layout for the NBC12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 8 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the NBC12429 outputs. It is imperative that low inductance chip capacitors are used. It is equally important that the board layout not introduce any of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

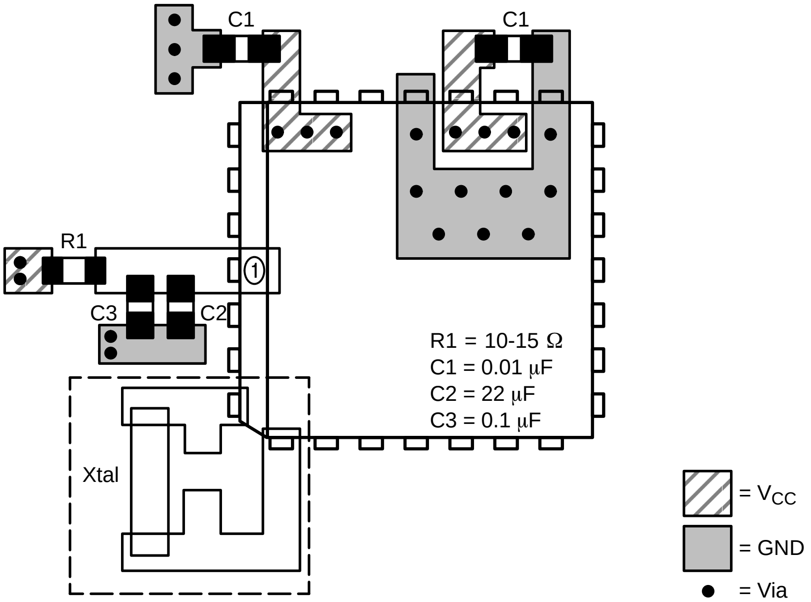


Figure 8. PCB Board Layout for NBC12429 (28 PLCC)

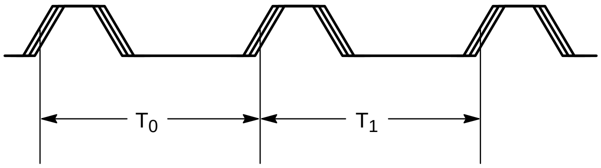
Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the NBC12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise-related problems in most designs.

Jitter Performance of the NBC12429

Jitter is a common parameter associated with clock generation and distribution. Clock jitter can be defined as the deviation in a clock's output transition from its ideal position.

Cycle-to-Cycle Jitter (short-term) is the period variation between two adjacent cycles over a defined number of observed cycles. The number of cycles observed is application dependent but the JEDEC specification is 1000 cycles.



$$T_{JITTER(cycle-cycle)} = T_1 - T_0$$

Figure 9. Cycle-to-Cycle Jitter

Peak-to-Peak Jitter is the difference between the highest and lowest acquired value and is represented as the width of the Gaussian base.

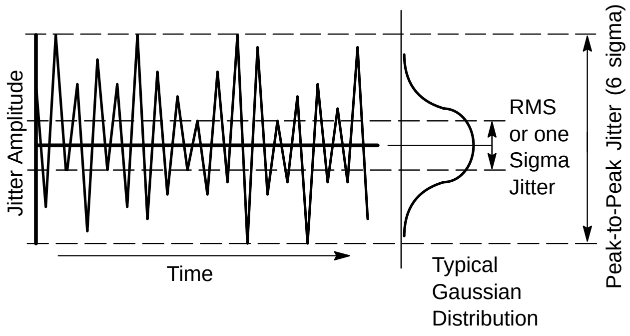


Figure 10. Peak-to-Peak Jitter

There are different ways to measure jitter and often they are confused with one another. The typical method of measuring jitter is to look at the timing signal with an oscilloscope and observe the variations in period-to-period or cycle-to-cycle. If the scope is set up to trigger on every rising or falling edge, set to infinite persistence mode and allowed to trace sufficient cycles, it is possible to determine the maximum and minimum periods of the timing signal. Digital scopes can accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. These scopes can also store a finite number of period durations and post-processing software can analyze the data to find the maximum and minimum periods.

Recent hardware and software developments have resulted in advanced jitter measurement techniques. The Tektronix TDS-series oscilloscopes have superb jitter analysis capabilities on non-contiguous clocks with their histogram and statistics capabilities. The Tektronix TDSJIT2/3 Jitter Analysis software provides many key timing parameter measurements and will extend that capability by making jitter measurements on contiguous clock and data cycles from single-shot acquisitions.

M1 by Amherst was used as well and both test methods correlated.

This test process can be correlated to earlier test methods and is more accurate. All of the jitter data reported on the NBC12429 was collected in this manner. Figure 11 shows the jitter as a function of the output frequency. The graph shows that for output frequencies from 25 to 400 MHz the jitter falls within the ±20 ps peak-to-peak specification. The general trend is that as the output frequency is increased, the output edge jitter will decrease.

Figure 12 illustrates the RMS jitter performance of the NBC12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency. However, the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter.

Long-Term Period Jitter is the maximum jitter observed at the end of a period's edge when compared to the position of the perfect reference clock's edge and is specified by the number of cycles over which the jitter is measured. The number of cycles used to look for the maximum jitter varies by application but the JEDEC spec is 10,000 observed cycles.

The NBC12429 exhibits long term and cycle-to-cycle jitter, which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility associated with a synthesizer over a fixed frequency oscillator. The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

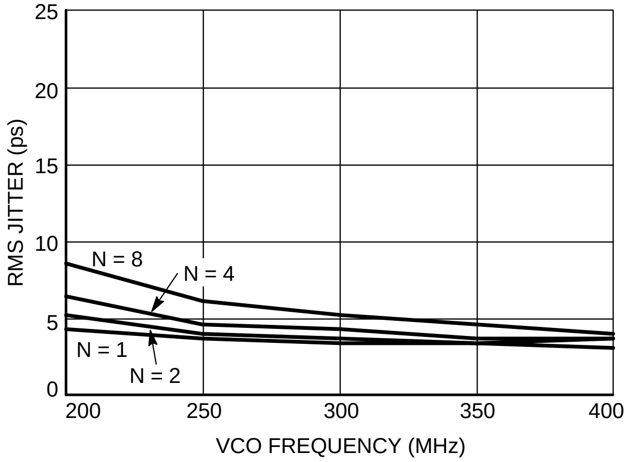


Figure 11. RMS Jitter vs. VCO Frequency

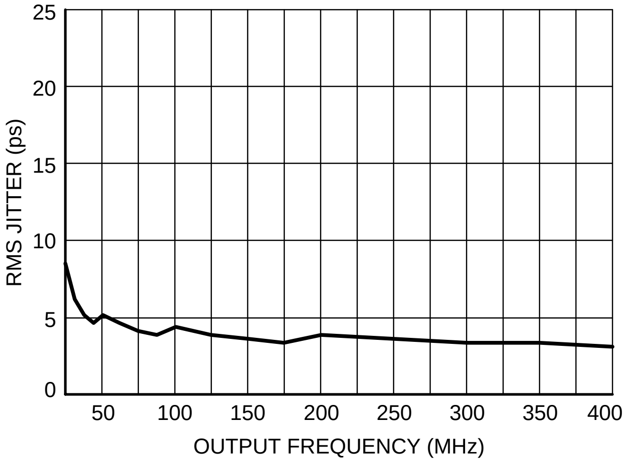


Figure 12. RMS Jitter vs. Output Frequency

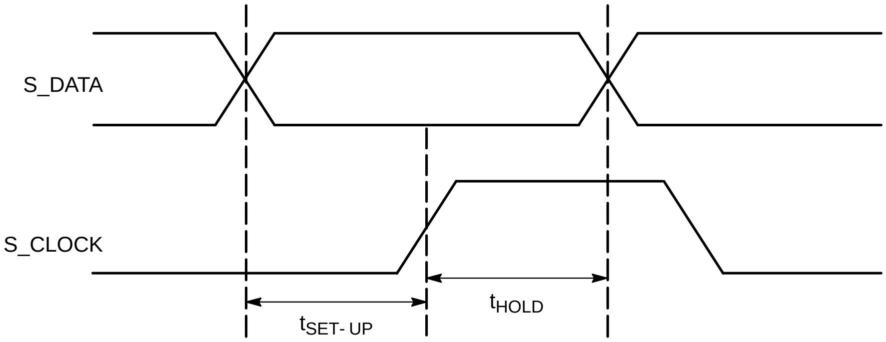


Figure 13. Set-Up and Hold

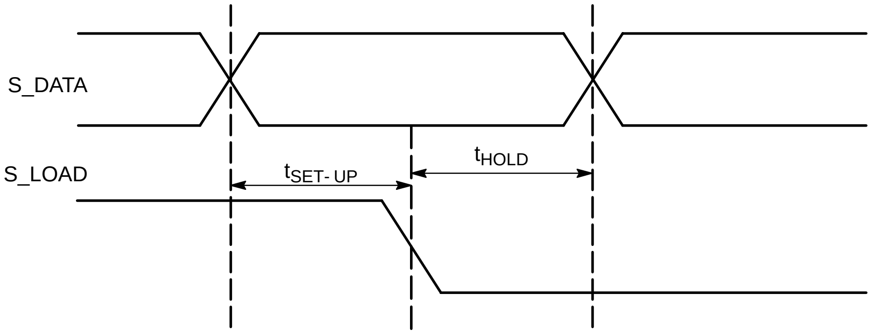


Figure 14. Set-Up and Hold

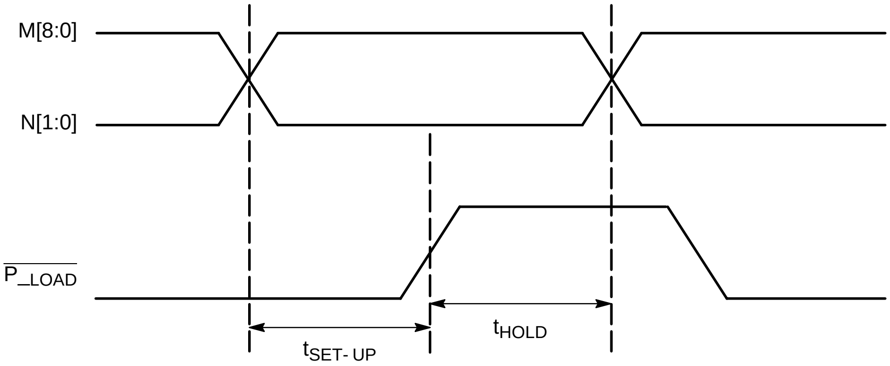
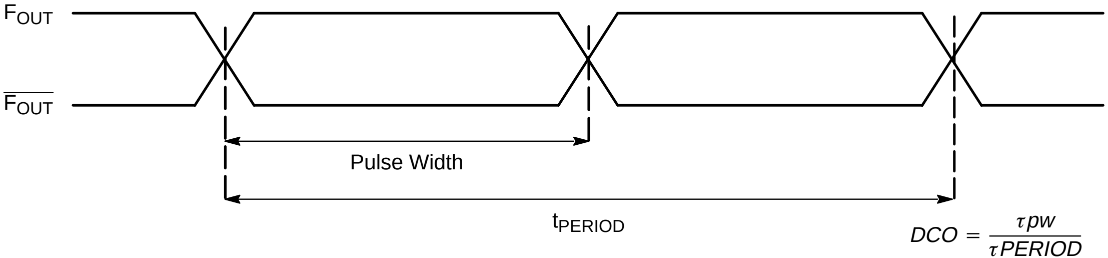


Figure 15. Set-Up and Hold



$$DCO = \frac{\tau pw}{\tau PERIOD}$$

Figure 16. Output Duty Cycle

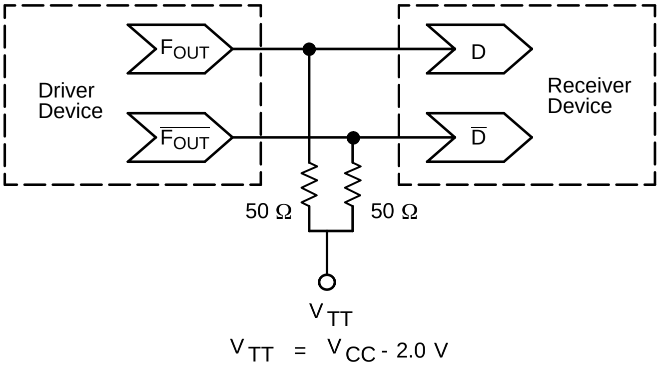
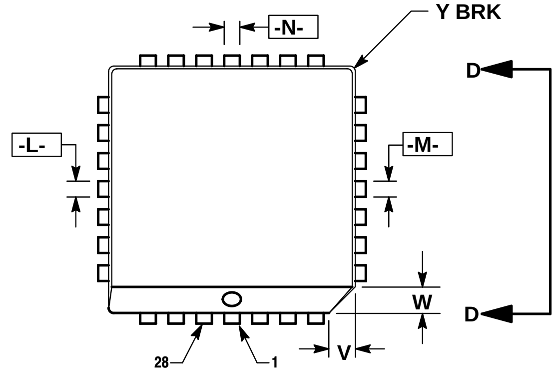


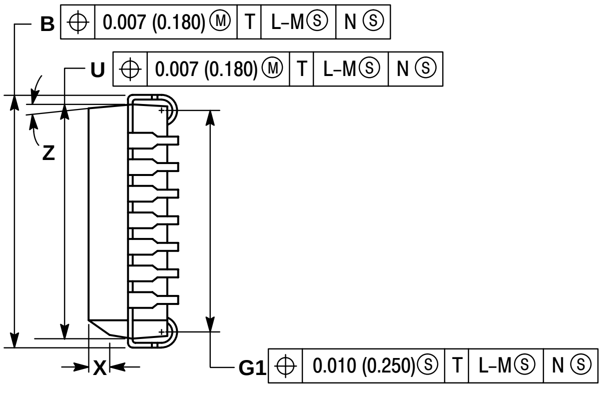
Figure 17. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 - Termination of ECL Logic Devices.)

PACKAGE DIMENSIONS

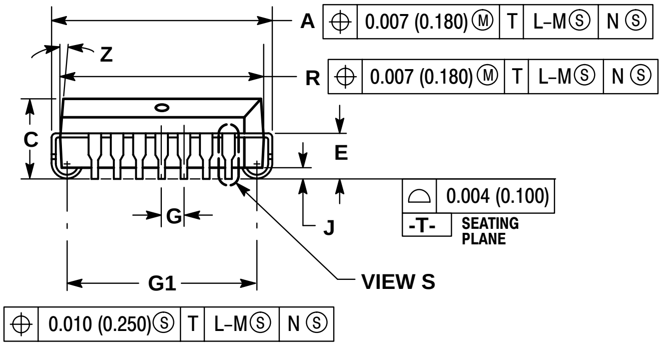
PLCC-28
FN SUFFIX

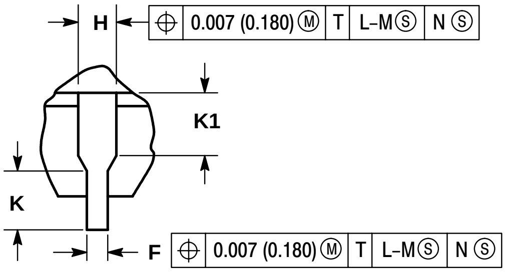
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E





VIEW D-D





VIEW S

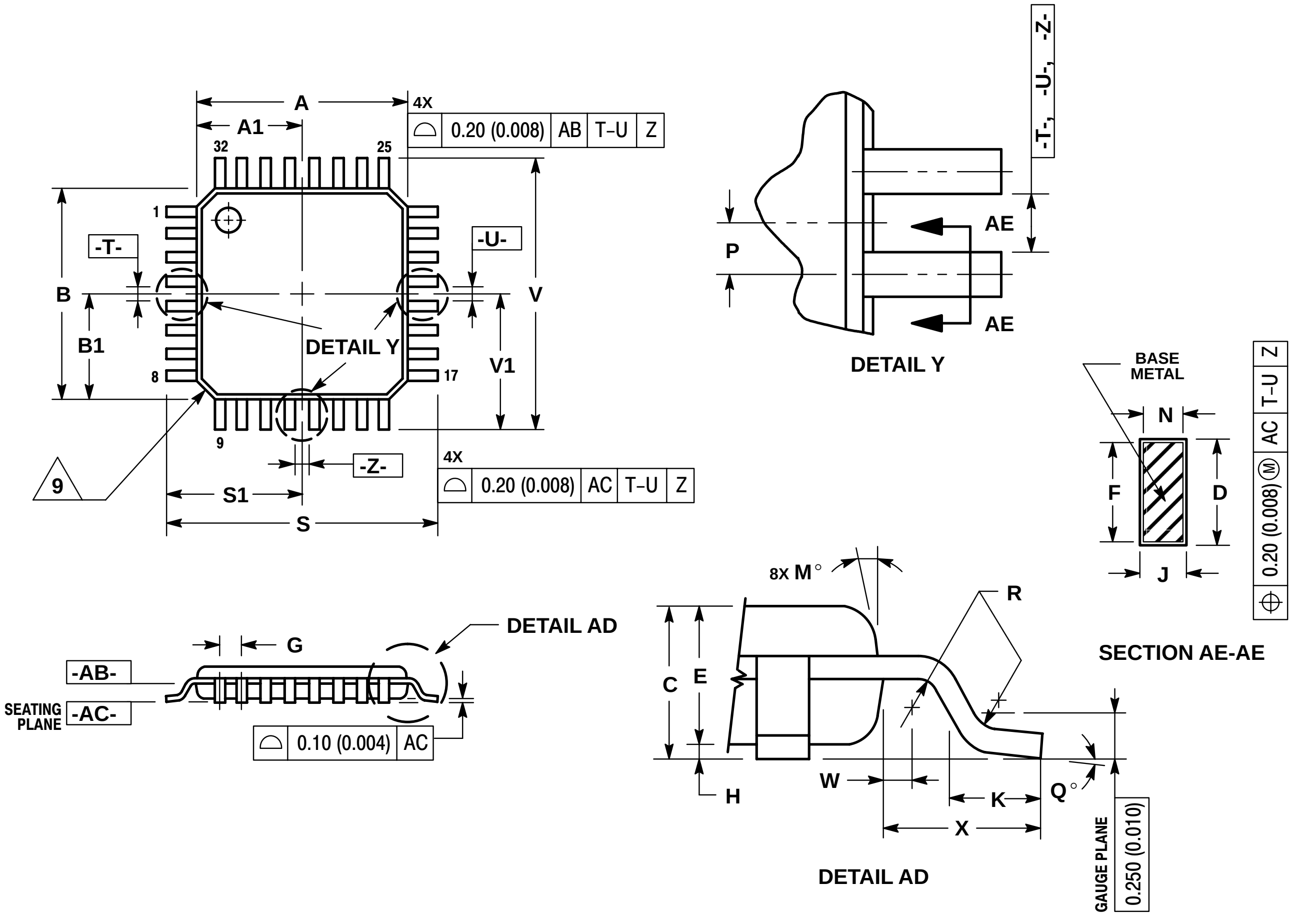
NOTES:

1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

PACKAGE DIMENSIONS

LQFP-32
FA SUFFIX
PLASTIC LQFP PACKAGE
CASE 873A-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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