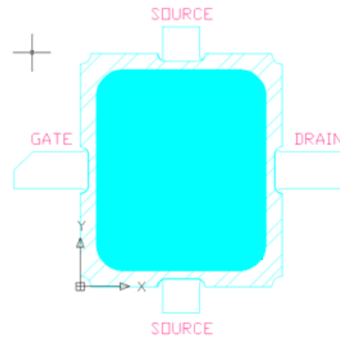
Filtronic

FPD4000AS

2.5W PACKAGED POWER pHEMT

- PERFORMANCE (1.8 GHz)
  - ♦ 34.5 dBm Output Power (P_{1dB})
  - ♦ 12 dB Power Gain (G_{1dB})
  - ♦ 45 dBm Output IP3
  - ♦ 8V Operation
  - ♦ 50% Power-Added Efficiency
  - ♦ Evaluation Boards Available
  - ♦ Design Data Available on Website
  - ♦ Suitable for applications to 5 GHz



SEE PACKAGE OUTLINE FOR MARKING CODE

- DESCRIPTION AND APPLICATIONS

The FPD4000AS is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), optimized for power applications in L-Band. The surface-mount package has been optimized for low parasitics.

Typical applications include drivers or output stages in PCS/Cellular base station transmitter amplifiers, as well as other power applications in WLL/WLAN amplifiers.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT *f* = 1.8 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 8V; I_{DQ} = 700 mA Γ_S and Γ_L tuned for Optimum IP3	33.5	34.5		dBm
Power Gain at dB Gain Compression	G_{1dB}	V_{DS} = 8V; I_{DQ} = 700 mA Γ_S and Γ_L tuned for Optimum IP3	10.5	12		
Maximum Stable Gain S_{21}/S_{12}	MSG	V_{DS} = 8V; I_{DQ} = 700 mA P_{IN} = 0dBm, 50Ω system		18		dB
Power-Added Efficiency at 1dB Gain Compression	PAE	V_{DS} = 8V; I_{DQ} = 700 mA Γ_S and Γ_L tuned for Optimum IP3		50		%
3rd-Order Intermodulation Distortion Γ_S and Γ_L tuned for Optimum IP3	IM3	V_{DS} = 8V; I_{DQ} = 700 mA P_{OUT} = 23 dBm (single-tone level)		-46		dBc
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	1.9	2.3	2.65	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		3.6		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		2.4		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -3 V		70	170	μA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 8 mA	0.7	0.9	1.4	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 8 mA	6	10		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 8 mA	20	22		V
Thermal Resistivity (channel-to-case)	Θ_{CC}	See Note on following page		16		°C/W

- RECOMMENDED OPERATING BIAS CONDITIONS

  Drain-Source Voltage: From 5V to 8V

  Quiescent Current: From 400 mA to 750 mA

- ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	-3V < V_{GS} < +0V		12	V
Gate-Source Voltage	V_{GS}	0V < V_{DS} < +8V		-3	V
Drain-Source Current	I_{DS}	For V_{DS} > 2V		I_{DSS}	mA
Gate Current	I_G	Forward / Reverse current		+20/-20	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		575	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		9.0	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1]$T_{Ambient}$ = 22°C unless otherwise noted [2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1

[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:

  P_{DC}: DC Bias Power

  P_{IN}: RF Input Power

  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:

  P_{TOT}= 9.0 - (0.0625W/°C) x T_{PACK}

  where T_{PACK} = *source tab lead temperature above 22°C*

  (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 55°C source lead temperature: P_{TOT} = 9.0 - (0.0625 x (55 – 22)) = 6.94W

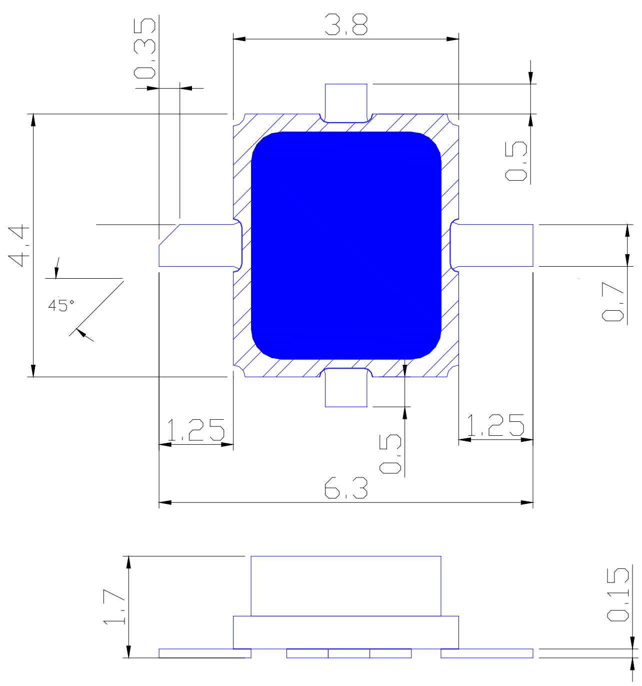
- **For optimum heatsinking, metal-filled through (Source) via holes should be used directly below the central metallized ground pad on the bottom of the package.**
- *Note on Thermal Resistivity:* The nominal value of 16°C/W is measured with the package mounted on a large heatsink with thermal compound to ensure adequate (unsoldered) contact. The package temperature is referred to the Source leads.

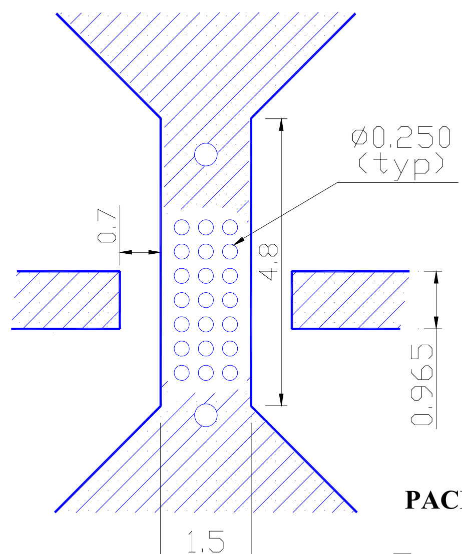
- HANDLING PRECAUTIONS

  To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. This product has be tested to Class 1A (> 250V but < 500V) using JESD22 A114, Human Body Model, and to Class A, (< 200V) using JESD22 A115, Machine Model.

- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD1000AS.
  - Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 3.25 Ω for the recommended 200mA operating point.
  - The recommended 200mA bias point is nominally a Class AB mode. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point.

- PACKAGE OUTLINE AND RECOMMENDED PC BOARD LAYOUT
  (dimensions in millimeters – mm)





PACKAGE MARKING CODE

Example:

***f*1ZD**
P1F

***f* = Filtronic**
1ZD = Lot / Date Code
P1F = Status, Part Code, Part Type

All information and specifications subject to change without notice.