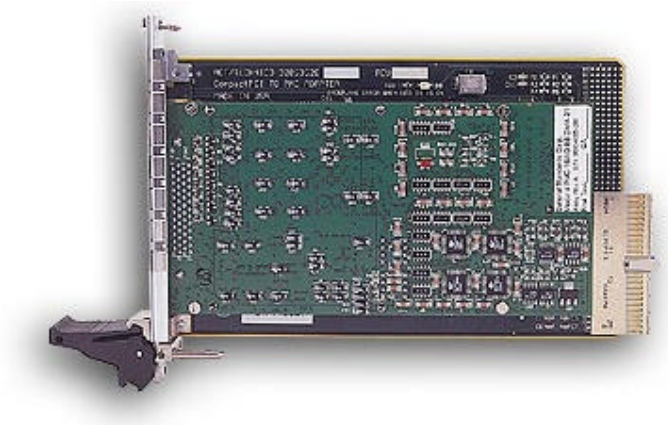
General Standards Corporation

High Performance Bus Interface Solutions

CPCI-16AIO-88

16-Channel 16-Bit Analog I/O CPCI Board

With 8 Input Channels, 8 Output Channels, and Auto calibration



Features Include:

- 8 Analog Output Channels with a 16-Bit D/A Converter per Channel
- 16-Bit Scanning ADC for 8 Single-Ended or 4 Differential Analog Input Channels
- Input and Output Ranges available as ±10V, ±5V or ±2.5V
- Input and Output FIFO Buffers; 32K-Sample Input, 16K-Sample Output Capacity
- Aggregate Analog Output Data Rates to 250K Channels per Second
- Simultaneous Updating of Outputs with Hardware or Software Strobe
- A/D Inputs Scanned at up to 73 KSPS Aggregate Rate; 9.5-16.2 KSPS per Channel
- Continuous or Burst Input Scanning Modes; Hardware and Software Triggering
- Programmable Rate Generator Supports Both Inputs and Outputs
- Autocalibration Trimming Implemented in Hardware, without Host Intervention
- Supports DMA Transfers as Bus Master
- Loopback Feature for Built-in-Test Support (BITE) and Periodic Autocalibration
- Integral Shield Assures Minimum Susceptibility to Radiated Noise in CPCI Environments
- VxWorks™ Driver available for both PowerPC™ and Pentium™

Applications Include:

✓ Data Acquisition Systems	✓ Precision Voltage Sources	✓ Automatic Test Equipment
✓ Industrial Robotics	✓ Function Generation	✓ Research Instrumentation

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Overview:

The 16-channel CPCI-16AIO-88 analog I/O board provides high-resolution 16-bit analog input and output resources in a high-density single-width CPCI module. Eight analog output channels can be updated either synchronously or asynchronously and can be used to perform waveform generation. Analog inputs are software-configurable either as eight single-ended or as four differential input channels, and can be scanned either continuously or in burst-mode. Inputs and outputs have a factory-configured range of ±10V, ±5V or ±2.5V, and are accessed through two FIFO buffers.

Internal Auto calibration networks permit periodic calibration to be performed without removing the board or host from the system. All input and output channels are calibrated against a single internal voltage reference. This feature produces the optimum calibration situation, in which the accuracy of the board is adjusted in its actual operating environment. Software-controlled test configurations include a loopback mode for monitoring all analog output channels.

Functional Description:

The CPCI-16AIO-88 board contains eight 16-Bit D/A converters, an 8-channel 16-bit scanning A/D converter, and all supporting functions necessary for adding flexible analog I/O capability to a CPCI host. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.1, and supports the "plug-n-play" system initialization concept. Designed for minimum off-line maintenance, the CPCI-16AIO-88 board includes internal monitoring and loopback features that eliminate the need for disconnecting or removing the module from the system for calibration. A shared programmable rate generator provides a time base for controlling either output clocking or input scanning, or permits input scanning be synchronized to the output clock. All system analog input and output connections are made through a single 50-pin subminiature-D front-access I/O connector.

Offset and gain trimming of the input and output channels is performed by calibration DAC's 's (Figure 1) that are loaded with channel correction values during initialization. During autocalibration, system analog inputs are replaced with either a precision voltage standard or the eight analog output channels. This arrangement is used to determine the necessary offset and gain correction values for the calibration DAC's. The correction values determined during autocalibration are stored in an EEprom for subsequent transfer to the calibration DAC's during board initialization.

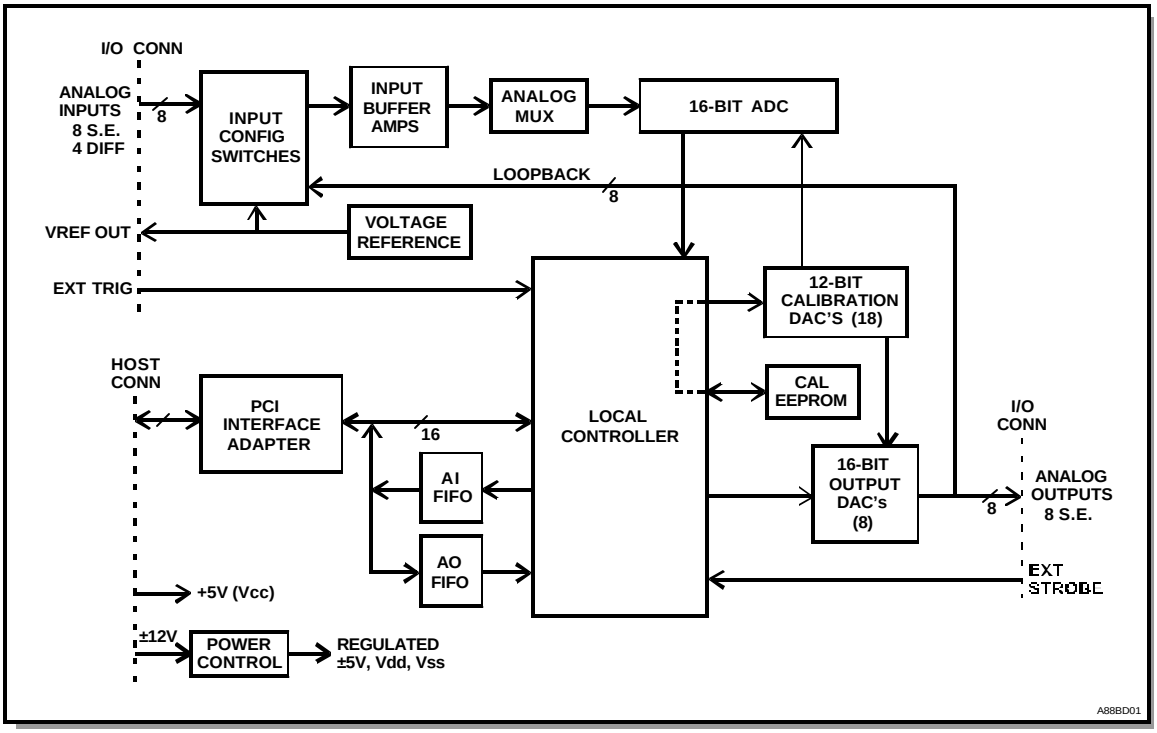

Figure 1. CPCI-16AIO-88 Analog I/O Board, Simplified Functional Diagram

The board receives output data and channel identification values through an analog output (AO) buffer. Analog input conversion values are transferred to the bus through an analog input (AI) FIFO buffer. A PCI Interface Adapter provides communication with the host PCI bus, and furnishes a 16-bit local bus for exchanging information between the FIFO buffers, the adapter, and the Local Controller. The Local Controller manages all internal operations.

ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

ANALOG INPUT CHANNELS

❑ Input Characteristics:

Configuration:	8 single-ended or 4 differential input channels; software selected
Voltage Ranges:	Factory configured as ±10 Volts, ±5 Volts or ±2.5 Volts
Input Impedance:	1.0 Megohms in parallel with 20 pF
Common Mode Rejection:	80 dB minimum, DC-60 Hz (Differential mode)
Common Mode Range:	Input range plus 1.0 Volt; e.g.: ±6V for the ±5V range (Differential mode)
Offset Voltage:	±2.0 millivolts, maximum
Noise:	2 mVRMS, 10Hz-10KHz
Remote Ground Sensing:	All single-ended inputs are measured relative to an external return
Overvoltage Protection:	±30 Volts with power applied; ±15 Volts with power removed

❑ Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Conversion Rate:	73KSPS (thousand samples per second), minimum in single-ended mode, 66KSPS in diferential mode.
Scan Rate:	Fixed at the maximum scan rate unless the rate generator is invoked. The rate generator provides programmable scan rates from 305 scans per second, up to the maximum scan rate.
Maximum Scan Rate:	9,500 scans per second in single-ended mode; 16,200 in differential mode.
Accuracy:	±0.007 percent of reading, ±0.01 percent of Full-Scale-Range, ±2.0 mV. e.g.: ± 3.3 mV, while reading +4 Volts on the ±5V range (10V FSR).
Crosstalk Rejection:	80dB minimum, adjacent channels; 85dB, nonadjacent channels; DC-1000Hz
Integral Nonlinearity:	±0.006 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

❑ **Analog Input Operating Modes and Controls**

Analog Input Modes:	Continuous Scan:	Analog inputs are scanned continuously
	Burst Scan:	A hardware or software trigger initiates a single scan
	Single-Ended:	Eight single-ended analog input channels
	Differential:	Four differential analog input channels
	Loopback:	Monitors a selected output channel with the analog input
	Reference:	Monitors the internal reference with the analog input

Software Burst Trigger:	Initiates an input burst-scan when asserted. Active only in burst-scan modes.
Input Data Buffer:	A 16-bit FIFO buffer provides analog input conversion data to the PCI bus.
Input Buffer Flags:	Input buffer empty or almost-full. Available as interrupt conditions.

ANALOG OUTPUT CHANNELS

❑ **Output Characteristics:**

Configuration:	Eight single-ended output channels
Voltage Ranges:	Factory configured as ±10 Volts, ±5 Volts or ±2.5 Volts
Output Resistance:	1.0 Ohm, maximum
Output protection:	Withstands sustained short-circuiting to ground, and overvoltage transients to ±50 Volts through 80 Ohms for 10 milliseconds.
Load Current:	±5 ma maximum; ±2 ma recommended for minimum crosstalk and line loss
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Noise:	1.2 kHz Filter: 2 mVRMS, 10Hz-10KHz 4 kHz Filter: 4 mVRMS, 10Hz-10KHz No Filter (75 kHz): 10 mVRMS, 10Hz-10KHz

❑ **Transfer Characteristics:**

Resolution:	16 Bits (0.0015 percent of FSR)
Output Sample Rate:	Fixed at the maximum sample rate unless the rate generator is invoked. The rate generator provides an output strobe that updates (samples) all output channels simultaneously. The strobe rate is programmable from 305 strobes per second, up to the maximum scan rate divided by the number of active channels.
Maximum Sample Rate:	250K channels per second, aggregate rate. Host-dependent.
Accuracy (No load):	±0.009 percent of reading, ±0.010 percent of Full-Scale-Range, ±1.5 mV. E.g.: ±2.9 mV, while generating +4 Volts on the ±5V range (10V FSR). Add ±1.0 mV per milliamp of loading.
Settling Time (0.01%):	No output filter: 40 us 4 kHz Filter: 0.40 ms 1.2 kHz Filter: 1.50 ms
Crosstalk Rejection:	75 dB minimum, DC-1000Hz
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

❑ **Analog Output Operating Modes and Controls**

Software Output Strobe:	Transfers data in all output channels to the output DAC's simultaneously
Output Data Buffer:	A 16-bit FIFO buffer receives analog output data and channel. Output channel number is accepted first, followed by the output value.
Buffer Flags:	Buffer-full and almost-empty flags. Available as interrupt conditions.

RATE GENERATOR

A programmable rate generator provides an adjustable internal time base for either the analog inputs or the analog outputs. The generator can be configured to control either the input scan rate, the output strobe rate, or both inputs and outputs simultaneously for input/output synchronization. The generator frequency is programmable from 305 Hz up to either the maximum input scan rate or the maximum output strobe rate.

AUTOCALIBRATION

A single bit in the board control register initiates Autocalibration. During autocalibration, all channels are calibrated to a single precision internal voltage reference, which is adjustable with a single front-panel trimmer. Analog output channels are active during autocalibration, which has a typical duration of three seconds.

PCI INTERFACE

❑ **Compatibility:** Conforms to CPCI Specification 2.1, with D32 read/write transactions.
Supports "plug-n-play" initialization.
Provides one multifunction interrupt.
Supports DMA transfers as bus master.

❑ **Board Control and Data Registers**

Board Control Register: 16-bit register; determines the operating modes of the board.
Data Buffers: 16-bit register; Data path for analog input and output data.
Rate Generator: 16-bit register; Adjusts the rate generator output frequency
Rate Control: 16-bit register; Controls utilization of the rate generator

❑ **Data FIFO Buffers**

Analog input and output values are exchanged with the host PCI bus through two FIFO buffers. Both buffers are 16 bits wide, 32 Kwords deep, and share the same address. The analog input buffer has a capacity of 32K input samples, and the output buffer has a capacity of 16K output values. Data is exchanged through the FIFO buffers in 16-bit offset binary format.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ **Power Requirements**

+5VDC ±0.2 VDC at 1.5 Amp, maximum

Maximum Power Dissipation: 6.5 Watts, Side 1
1.0 Watt, Side 2

❑ **Physical Characteristics**

Height: 106.7 mm
Depth: 74.0 mm
Width: 160.0 mm

❑ **Environmental Specifications**

Ambient Temperature Range: Operating: 0 to +55 degrees Celsius
Storage: -40 to +85 degrees Celsius

Relative Humidity: Operating: 0 to 80%, non-condensing
Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

Cooling: Conventional convection cooling

❑ **System Connector:** Standard 50-pin 0.050" D-Subminiature male connector, AMP#1-750913-5 or equivalent

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-AB", as indicated below. For example, model number CPCI-16AIO-88-32 describes a card with ±10 Volt input/output ranges and 1.2 kHz output filters.

Optional Parameter	Value	Specify Option As:
Input/output Range	±2.5 Volts	A = 1
	±5 Volts	A = 2
	±10 Volts	A = 3
Output Lowpass Filter	No output Filter *	B = 1
	1.2 kHz Output Filter	B = 2
	4 kHz Output Filter	B = 3

* Output frequency response with no output filter is approximately 75 kHz.

Note: This CPCI product consists of a PMC-16AIO-88 board attached to a standard PCI carrier card.

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